Vanguard Semiconductor

VSE002N03MS-G
30V/120A N-Channel Advanced Power MOSFET

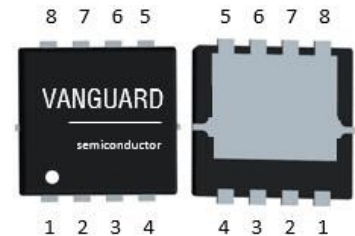|		
V_{DS}	30	V
$R_{DS(on),TYP}$ @ V_{GS}=10V	1.4	mΩ
$R_{DS(on),TYP}$ @ V_{GS}=4.5V	2.2	mΩ
I_D	120	A

Features

- Enhancement mode

- Low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V

- VitoMOS$^®$ Ⅱ Technology

- Fast Switching and High efficiency
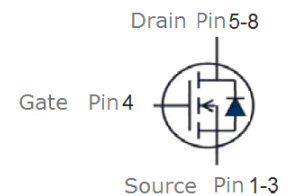
- Pb-free lead plating; RoHS compliant; Halogen free

Pb-Free   RoHS   HF Halogen-Free

PDFN3333

Drain Pin 5-8
Gate Pin 4
Source Pin 1-3

Part ID	Package Type	Marking	Tape and reel information
VSE002N03MS-G	PDFN3333	002N03M	5000pcs/Reel

Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		30	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C=25°C	120	A
I_D	Continuous drain current @V_{GS}=10V	T_C=25°C	120	A
		T_C=100°C	76	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	480	A
I_{DSM}	Continuous drain current @V_{GS}=10V	T_A=25°C	35	A
		T_A=70°C	28	A
EAS	Avalanche energy, single pulsed ②		56	mJ
P_D	Maximum power dissipation	T_C=25°C	42	W
		T_C=100°C	17	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	3.6	W
		T_A=70°C	2.3	W
T_{STG}, T_J	Storage and junction temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{θJC}$	Thermal Resistance, Junction-to-Case	3	3.6	°C/W
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient	35	42	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250µA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=30V,V_{GS}=0V	--	--	1	µA
	Zero Gate Voltage Drain Current(Tj=125℃)	V_{DS}=30V,V_{GS}=0V	--	--	100	µA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250µA	1.2	1.6	2.3	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=20A	--	1.4	1.8	mΩ
		Tj=100℃	--	1.7	2.3	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	V_{GS}=4.5V, I_D=10A	--	2.2	2.9	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=15V,V_{GS}=0V, f=1MHz	2080	2450	2820	pF
C_{oss}	Output Capacitance		980	1155	1330	pF
C_{rss}	Reverse Transfer Capacitance		70	80	90	pF
R_q	Gate Resistance	f=1MHz	1.5	2.1	2.7	Ω
Q_q (10V)	Total Gate Charge	V_{DS}=15V,I_D=20A, V_{GS}=10V	--	45	58	nC
Q_q (4.5V)	Total Gate Charge		--	23	30	nC
Q_{gs}	Gate-Source Charge		--	7.1	--	nC
Q_{gd}	Gate-Drain Charge		--	8.8	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=15V, I_D=20A, R_G=3Ω, V_{GS}=10V	--	8.2	--	ns
t_r	Turn-on Rise Time		--	59	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	--	ns
t_f	Turn-Off Fall Time		--	23	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=0V	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	Tj=25℃,I_{sd}=20A, V_{GS}=0V di/dt=100A/µs	--	35	--	ns
Q_{rr}	Reverse Recovery Charge		--	18	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by TJmax, starting TJ = 25°C, L = 0.5mH, RG = 25Ω, IAS = 15A, VGS =10V. Part not recommended for use above this value

③ The power dissipation PDSM is based on R$_{θJA}$ and the maximum allowed junction temperature of 150°C.

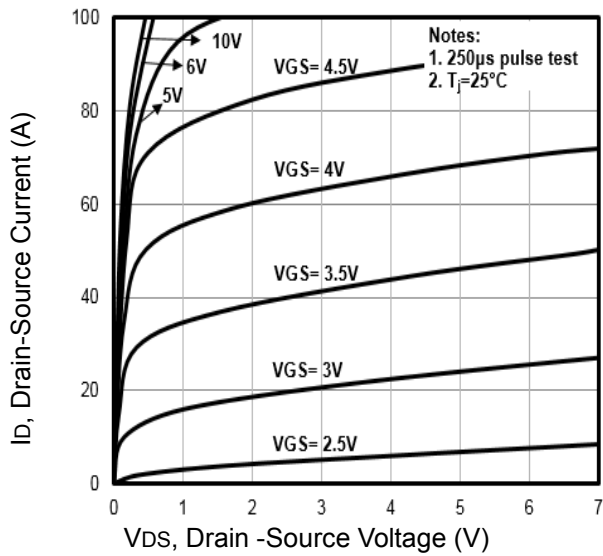④ Pulse width ≤ 380µs; duty cycle≤ 2%.

Typical Characteristics
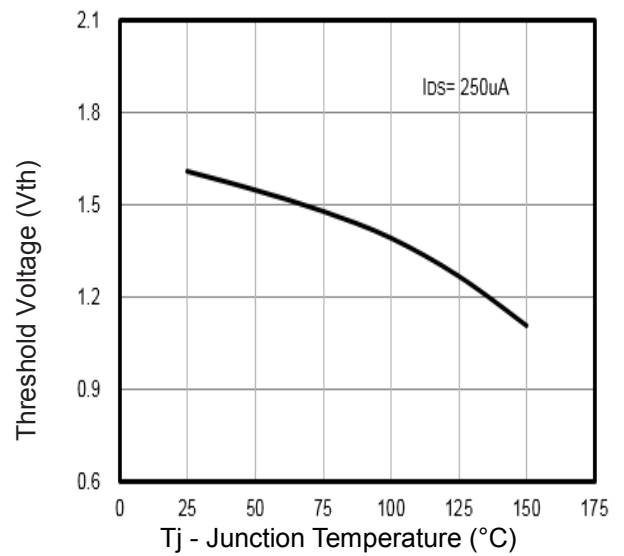
Fig1. Typical Output Characteristics

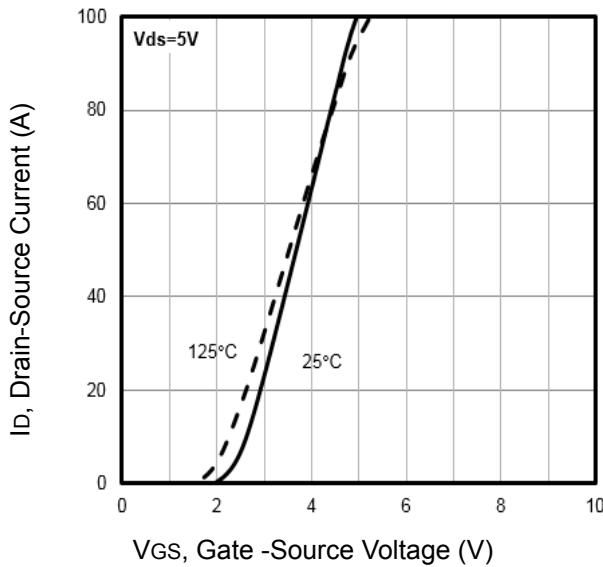**Fig2.** Threshold Voltage Vs. Temperature
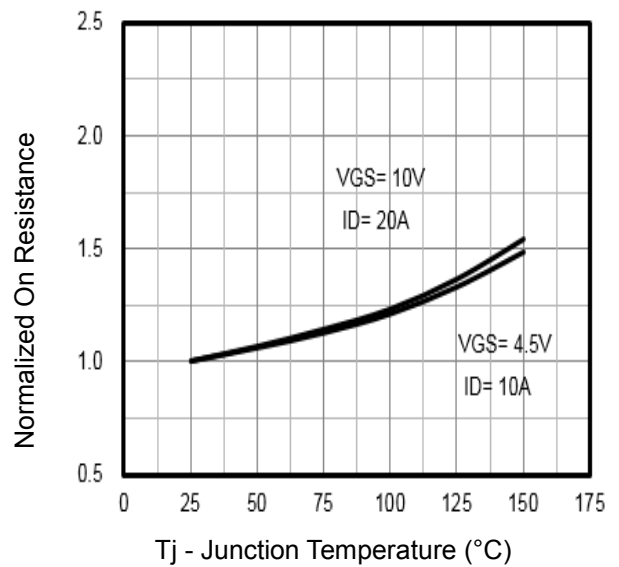
Fig3. Typical Transfer Characteristics

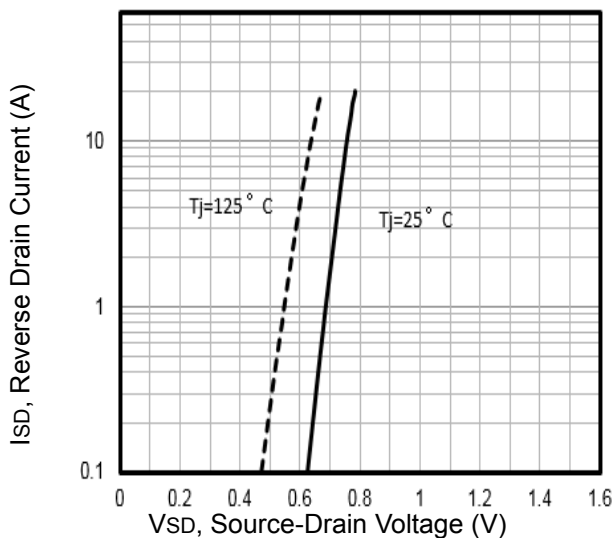**Fig4.** Normalized On-Resistance Vs. Temperature

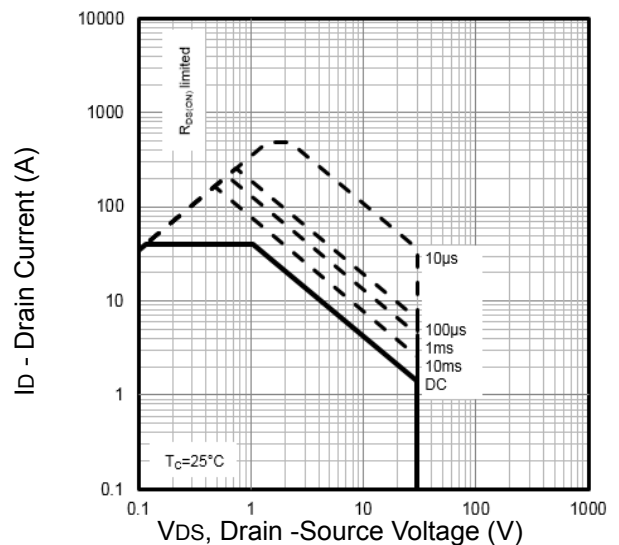**Fig5.** Typical Source-Drain Diode Forward Voltage

Fig6. Maximum Safe Operating Area
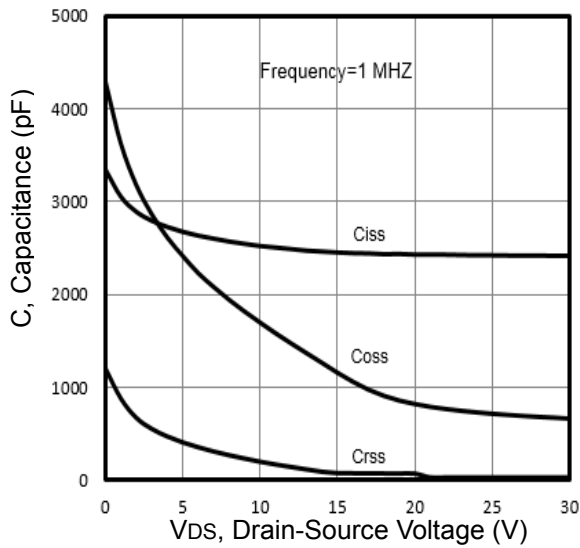
Typical Characteristics
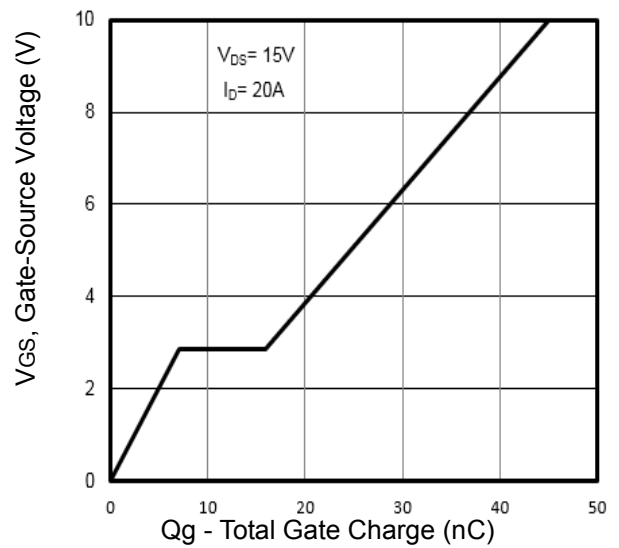

Fig7. Typical Capacitance Vs. Drain-Source Voltage

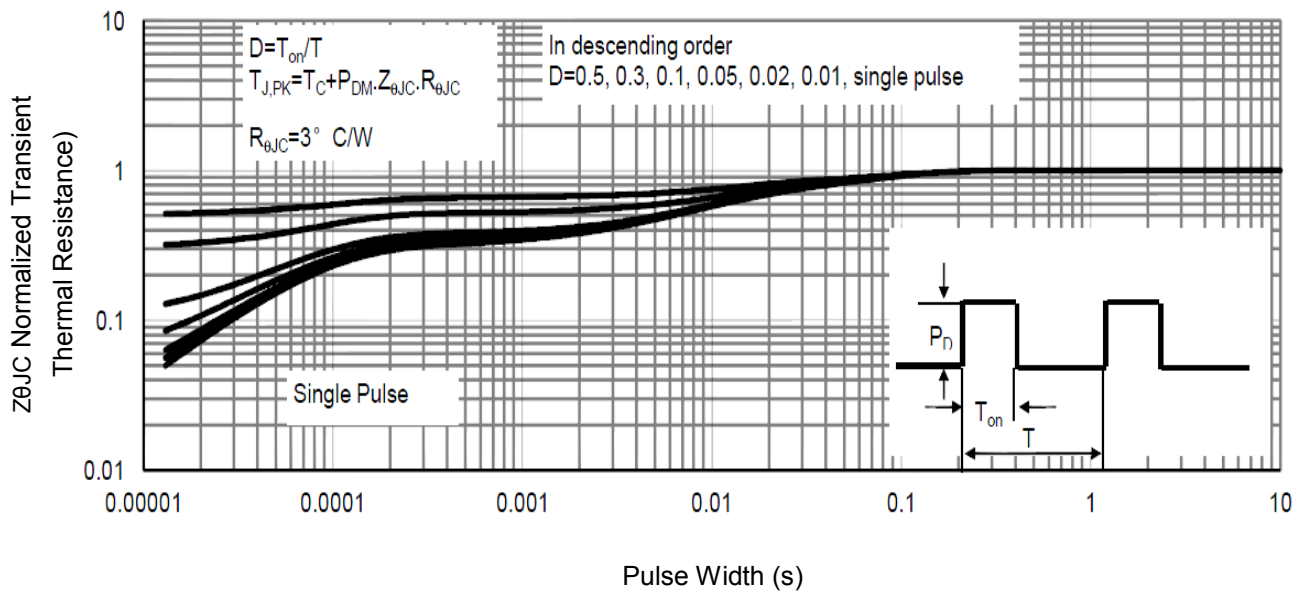**Fig8.** Typical Gate Charge Vs. Gate-Source

Pulse Width (s)

Fig9. Normalized Maximum Transient Thermal Impedance

Fig10. Unclamped Inductive Test Circuit and waveforms

Fig11. Switching Time Test Circuit and waveforms

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Marking Information

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┌─────────────────────┐
│  Vs                 │
│  002N03M            │
│  XXXYWW             │
│  ●                  │
└─────────────────────┘
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1st line：   Vanguard Code（Vs）

2nd line：   Part Number（002N03M）
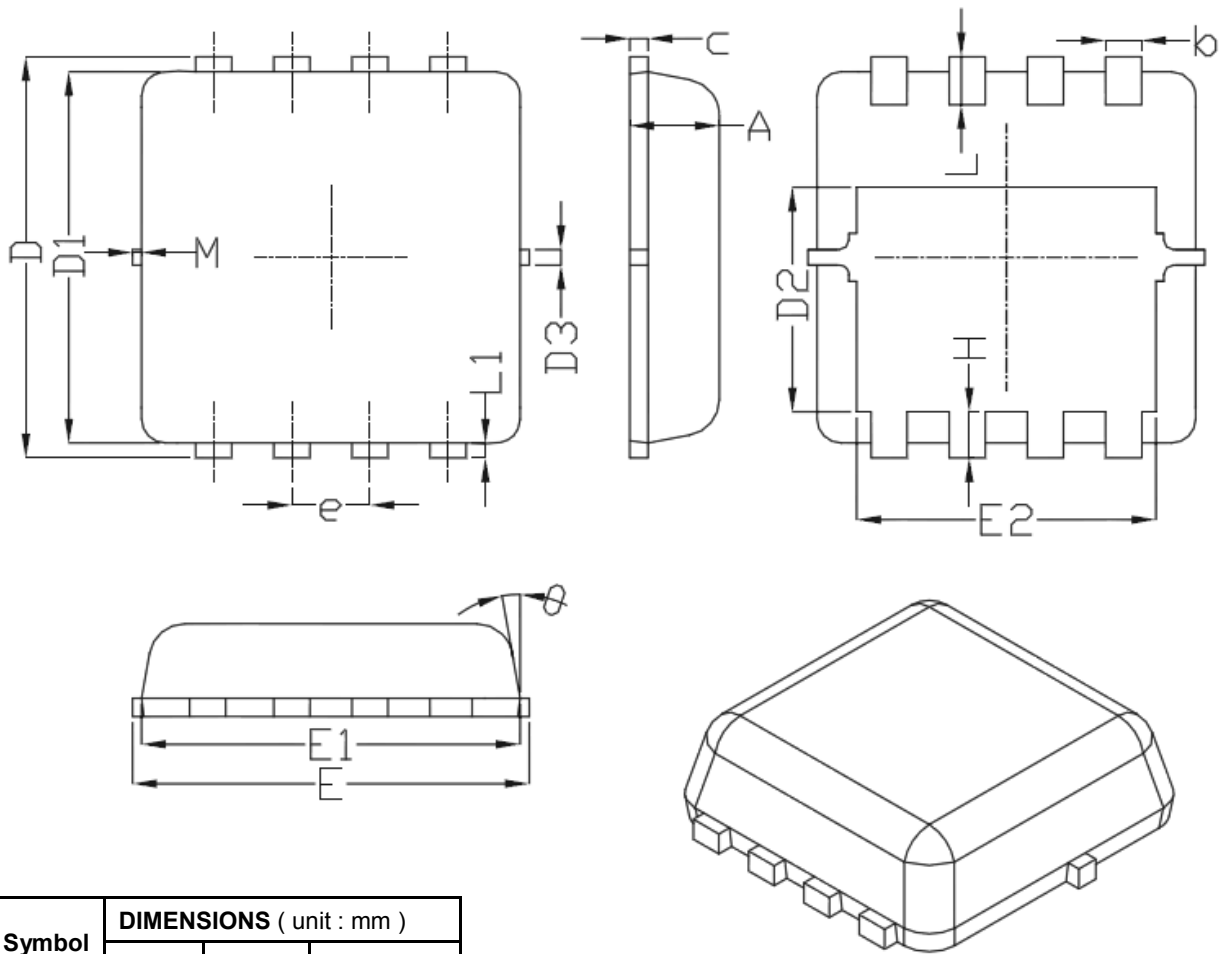
3rd line：   Date code （XXXYWW）

        XXX：   Wafer Lot Number Code , code changed with Lot Number

        Y：   Year Code (e.g. E=2017, F=2018, G=2019, H=2020, etc)

        WW：   Week Code (01 to 53)

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PDFN3333 Package Outline Data

Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15
* Not specified			

Notes:

1. Follow JEDEC MO-240 variation CA.

2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.

3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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单击下面可查看定价，库存，交付和生命周期等信息

>>Vanguard Semiconduct(威兆半导体)