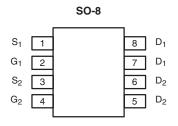


Dual P-Channel 20V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
	0.018 at V _{GS} = - 4.5 V	- 8.9		
- 20	0.022 at V _{GS} = - 2.5 V	- 8.1		
	0.030 at V _{GS} = - 1.8 V	- 3.6		



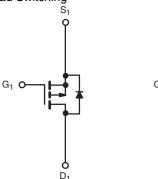
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Advanced High Cell Density Process
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

· Load Switching



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	- 20		V	
Gate-Source Voltage		V _{GS}	± 12			
Continuous Drain Current /T 150 °C\8	T _A = 25 °C	I-	- 8.9 - 6.7	- 6.7		
Continuous Drain Current $(T_J = 150 ^{\circ}C)^a$	T _A = 70 °C	- I _D	- 7.1	- 5.4		
Pulsed Drain Current		I _{DM}	- 30		Α	
Continuous Source Current (Diode Conduction) ^a		I _S	- 1.7	- 0.9		
	T _A = 25 °C	- P _D	2.0	1.1	W	
Maximum Power Dissipation ^a	T _A = 70 °C] ' ['] D	1.3	0.7] **	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manifestory Longition to Austriania	t ≤ 10 s	R_{thJA}	46	62.5	
Maximum Junction-to-Ambient ^a	Steady State	' ¹thJA	80	110	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	24	32	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

1



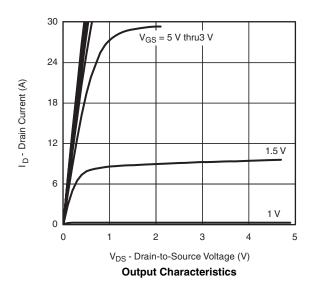
Parameter	Symbol	Test Conditions M		Тур.	Max.	Unit	
Static	<u>'</u>		I.	1	<u>'</u>		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -350 \mu A$	- 0.4		- 1.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Cuvvant	1	V _{DS} = - 20 V, V _{GS} = 0 V			- 1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C	C -5	μΑ			
On-State Drain Current ^a	I _{D(on)}	V _{DS} = - 5 V, V _{GS} = - 4.5 V	- 30			Α	
		V _{GS} = - 4.5 V, I _D = - 8.9 A		0.018			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 8.1 A		0.022		Ω	
		V _{GS} = - 1.8 V, I _D = - 3.6 A	- 1.8 V, I _D = - 3.6 A 0.0	0.030			
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 8.9 A		26		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 1.7 A, V _{GS} = 0 V		- 0.7	- 1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g			34.5	52		
Gate-Source Charge	Q_{gs}	V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_{D} = - 8.9 A		5.1		nC	
Gate-Drain Charge	Q_{gd}			9.6			
Gate Resistance	R_g			9		Ω	
Turn-On Delay Time	t _{d(on)}			25	40		
Rise Time t		V_{DD} = - 10 V, R_L = 6 Ω		46	70		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		230	345	ns	
Fall Time	t _f			155	235		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 1.7 A, dl/dt = 100 A/μs		128	200		

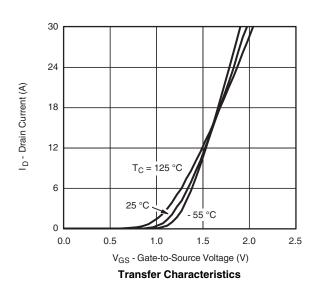
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

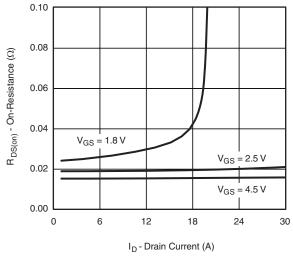
TYPICAL CHARACTERISTICS 25 °C unless otherwise noted



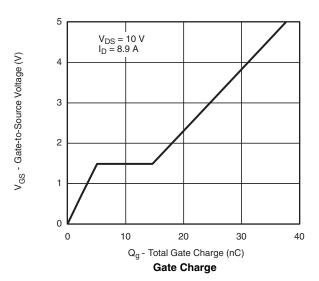


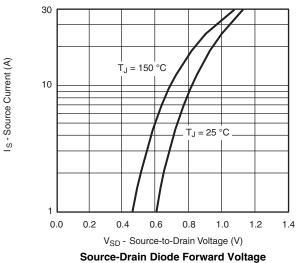


TYPICAL CHARACTERISTICS 25 °C unless otherwise noted



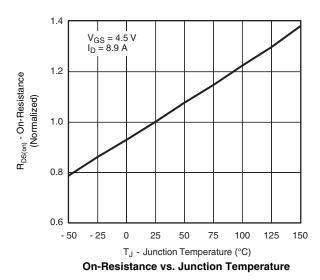
On-Resistance vs. Drain Current

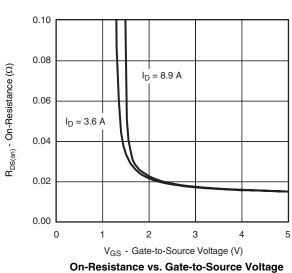




5000 4000 C - Capacitance (pF) C_{iss} 3000 2000 C_{oss} 1000 0 0 2 6 8 10 12 V_{DS} - Drain-to-Source Voltage (V)

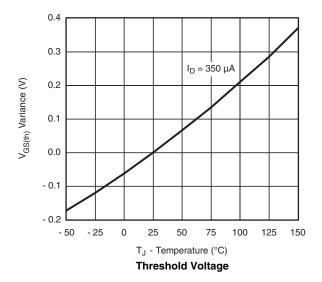
Capacitance

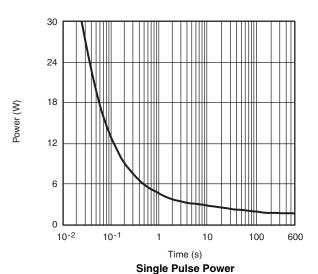


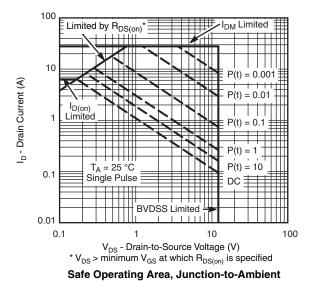


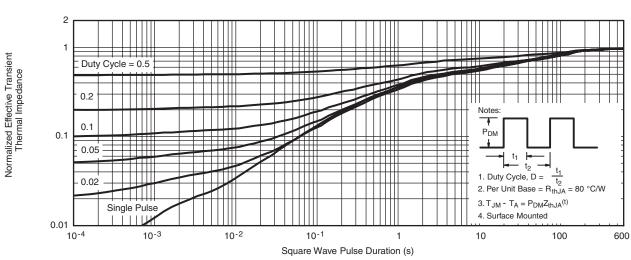


TYPICAL CHARACTERISTICS 25 °C unless otherwise noted





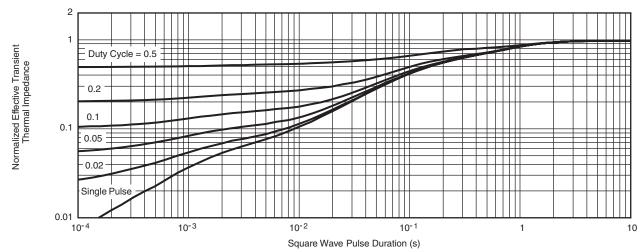




Normalized Thermal Transient Impedance, Junction-to-Ambient



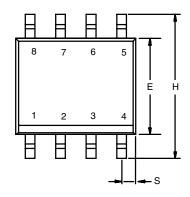
TYPICAL CHARACTERISTICS 25 °C unless otherwise noted

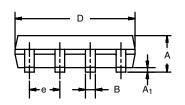


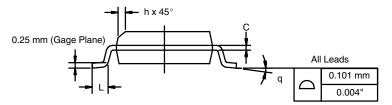
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







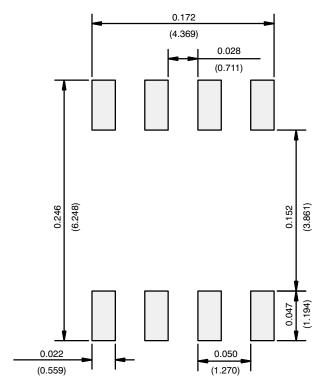
	MILLIM	IETERS	INC	HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C 06527 Pay I 11 San 06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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