N- and P-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
N-Channel	60	0.030 at V_{GS} = 10 V	35	6 nC
		0.033 at V_{GS} = 4.5 V	30	
P-Channel	- 60	0.050 at V_{GS} = - 10 V	- 19	8 nC
		0.060 at V_{GS} = - 4.5 V	- 15	

FEATURES

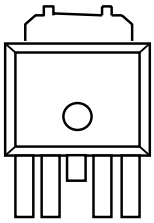
- **Halogen-free According to IEC 61249-2-21 Available**
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

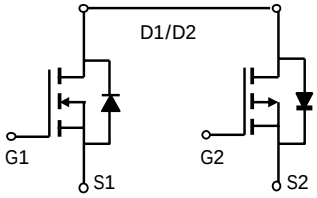
APPLICATIONS

- CCFL Inverter

TO-252
D-PAK



Top View
Drain Connected to Tab



N-channel **P-channel**

ABSOLUTE MAXIMUM RATINGS (TA = 25°C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**Nch Limit**	**Pch Limit**	**Units**
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current [a]	T_C=25°C	I_D	35	-20	A
Pulsed Drain Current [b]		I_{DM}	140	-80	
Continuous Source Current (Diode Conduction) [a]	T_C=25°C	I_S	35	-20	A
Power Dissipation [a]	T_C=25°C	P_D	50	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	T_J, T_{stg}	-55 to 175	°C

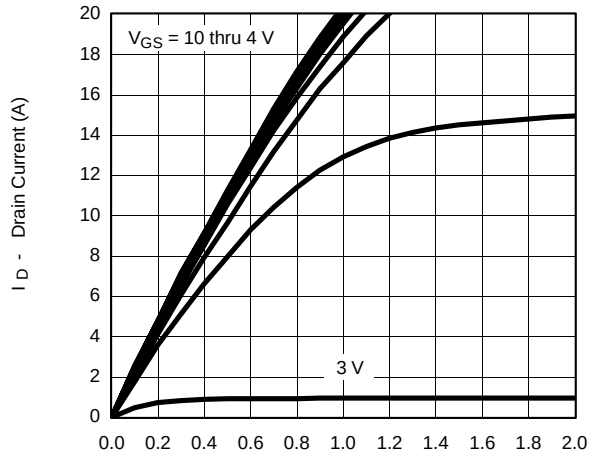
THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient [c]	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3	

Notes

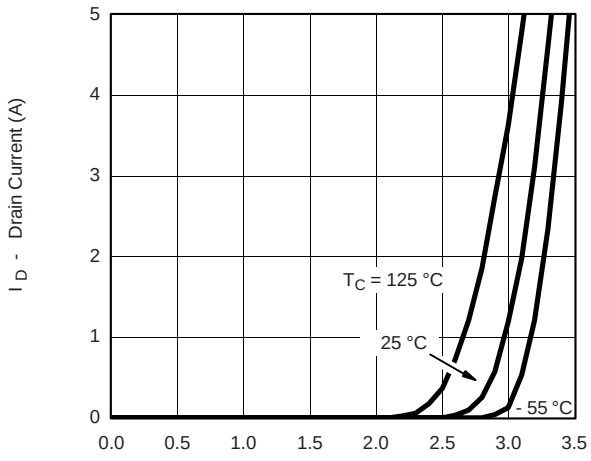
a. Package Limited
b. Pulse width limited by maximum junction temperature
c. Surface Mounted on 1” x 1” FR4 Board.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 uA	1		3	V
		V_{DS} = V_{GS}, I_D = -250 uA	-1		-3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	uA
		V_{DS} = -48 V, V_{GS} = 0 V			-1	
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	45			A
		V_{DS} = -5 V, V_{GS} = -10 V	-25			A
Drain-Source On-Resistance [a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		30		mΩ
		V_{GS} = 4.5 V, I_D = 16 A		33		
		V_{GS} = -10 V, I_D = -10 A		50		mΩ
		V_{GS} = -4.5 V, I_D = -8 A		60		
Forward Transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		15		S
		V_{DS} = -15 V, I_D = -10 A		11		S
Diode Forward Voltage [a]	V_{SD}	I_S = 17 A, V_{GS} = 0 V		0.89		V
		I_S = -10 A, V_{GS} = 0 V		-0.98		V
Dynamic [b]						
Total Gate Charge	Q_g	N - Channel V_{DS} = 30 V, V_{GS} = 4.5 V, I_D = 20 A		9		nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			4		
Turn-On Delay Time	$t_{d(on)}$	N - Channel V_{DS} = 30 V, R_L = 1.5 Ω, I_D = 20 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		5		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			27		
Fall Time	t_f			8		
Input Capacitance	C_{iss}	N - Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1 Mhz		1500		pF
Output Capacitance	C_{oss}			84		
Reverse Transfer Capacitance	C_{rss}			79		
Total Gate Charge	Q_g	P - Channel V_{DS} = -30 V, V_{GS} = 4.5 V, I_D = -10 A		10		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			4		
Turn-On Delay Time	$t_{d(on)}$	P - Channel V_{DS} = -30 V, R_L = 3 Ω, I_D = -10 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		5		ns
Rise Time	t_r			4		
Turn-Off Delay Time	$t_{d(off)}$			30		
Fall Time	t_f			11		
Input Capacitance	C_{iss}	P - Channel V_{DS} = -15 V, V_{GS} = 0 V, f = 1 Mhz		1180		pF
Output Capacitance	C_{oss}			84		
Reverse Transfer Capacitance	C_{rss}			60		

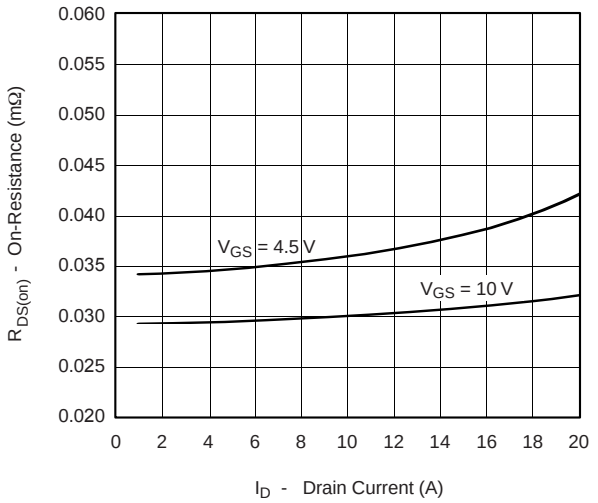
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



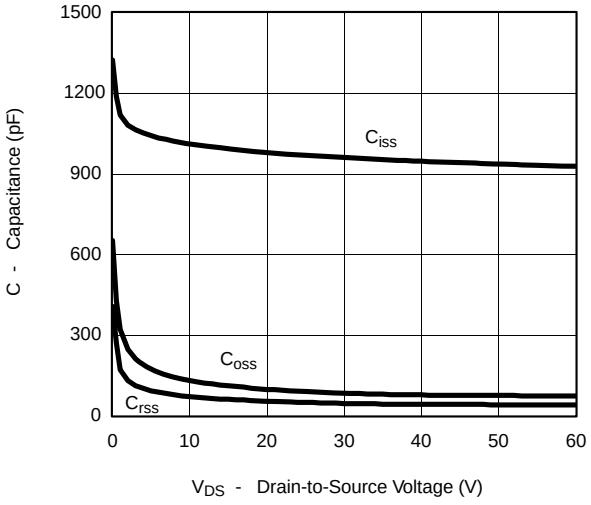
Output Characteristics



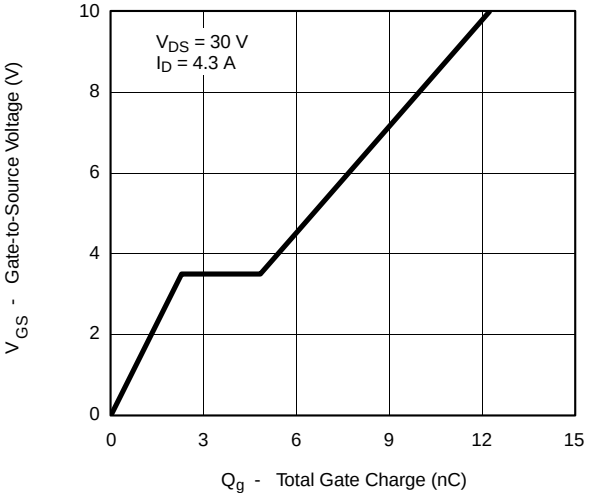
Transfer Characteristics



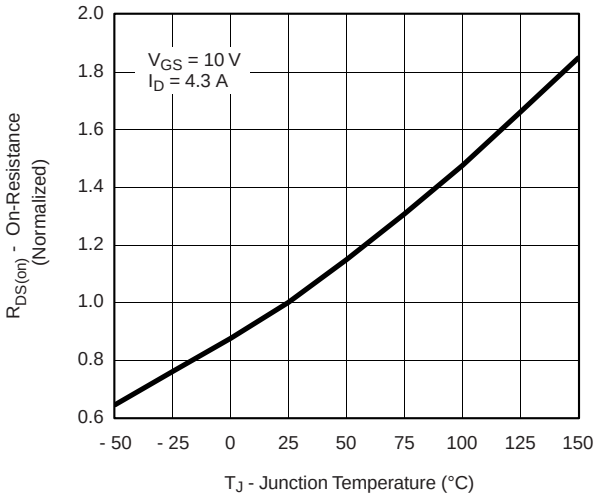
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

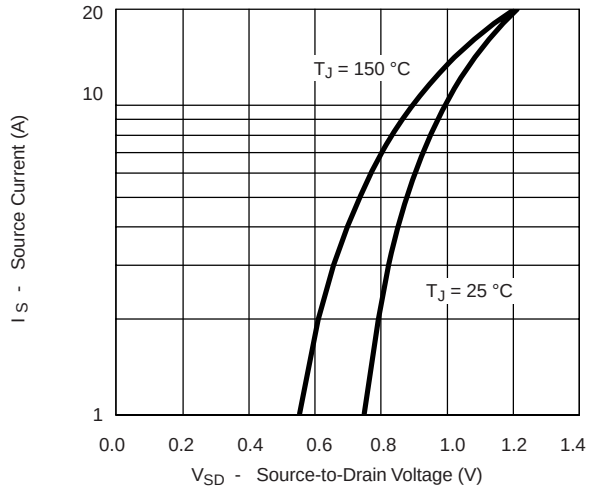


Gate Charge

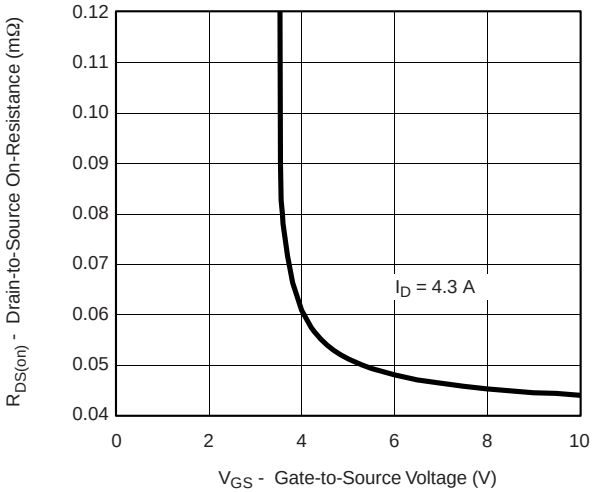


On-Resistance vs. Junction Temperature

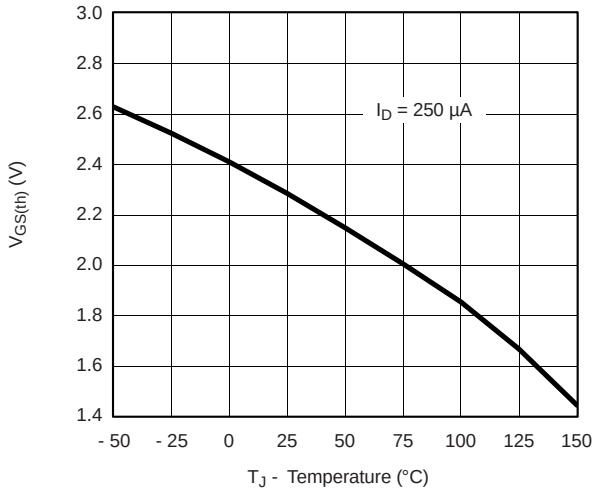
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



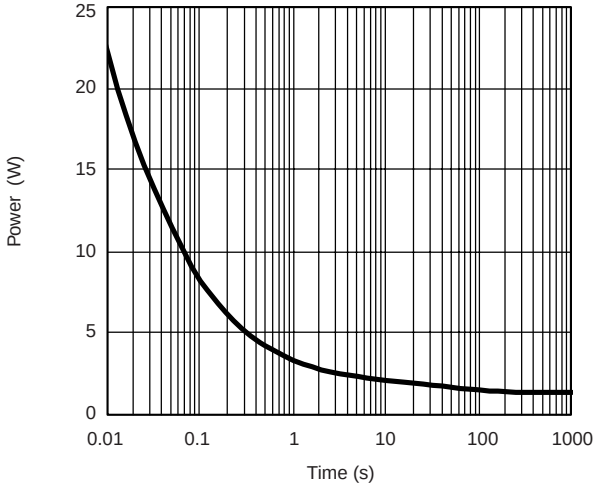
Source-Drain Diode Forward Voltage



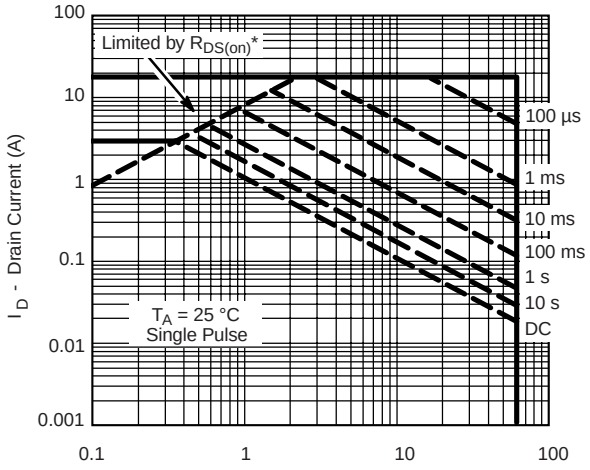
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



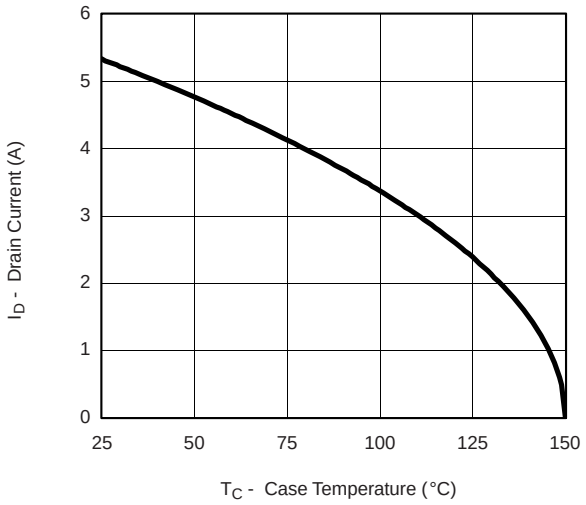
Single Pulse Power, Junction-to-Ambient



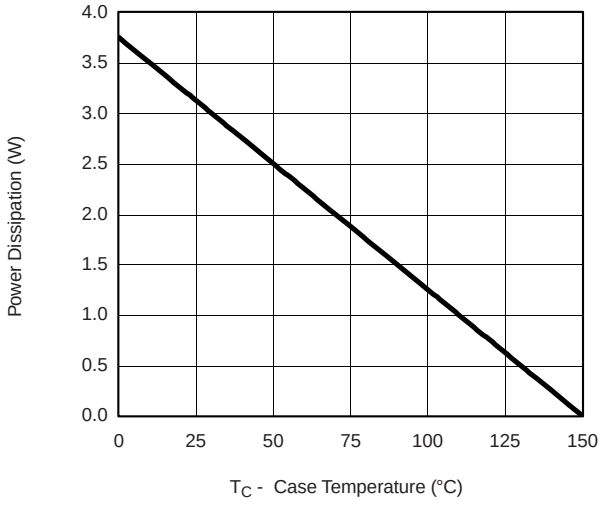
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

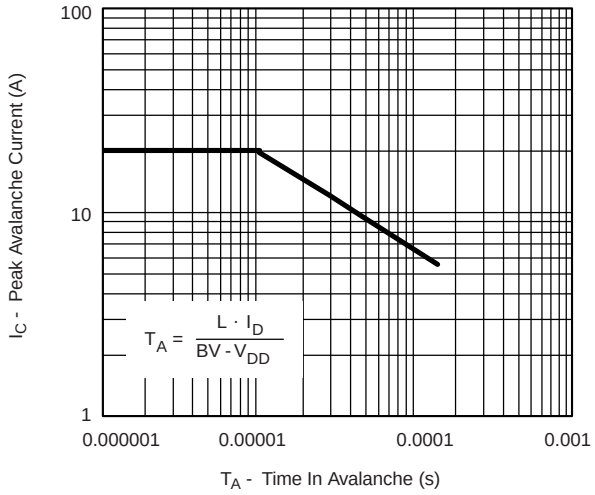
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



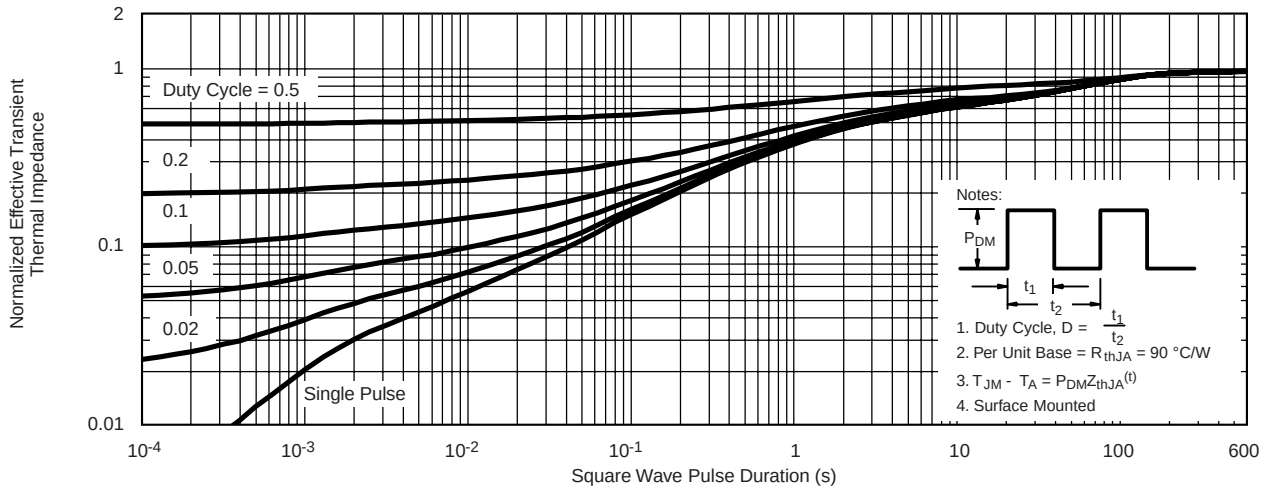
Power Derating



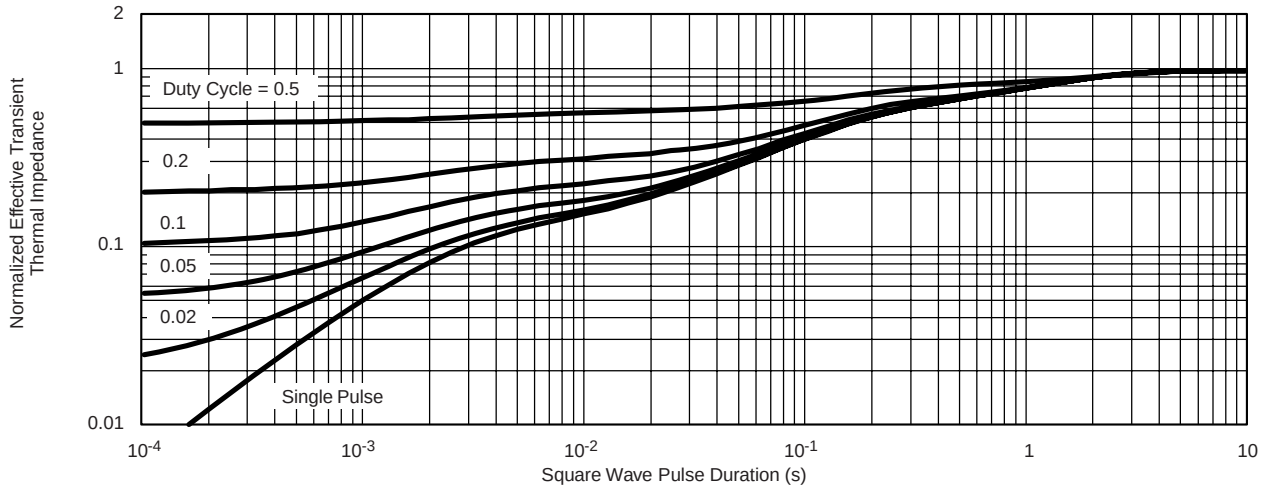
Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

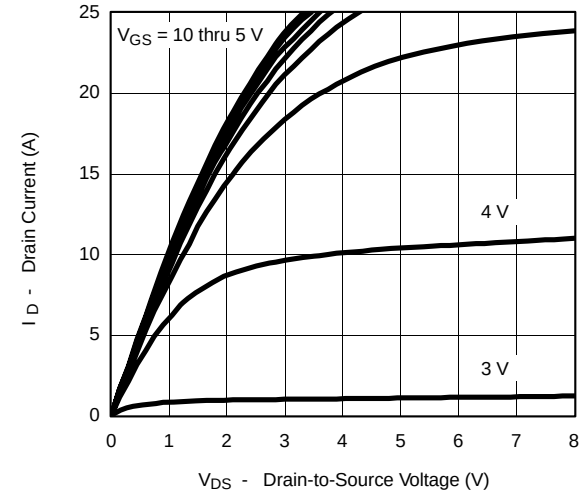


Normalized Thermal Transient Impedance, Junction-to-Ambient

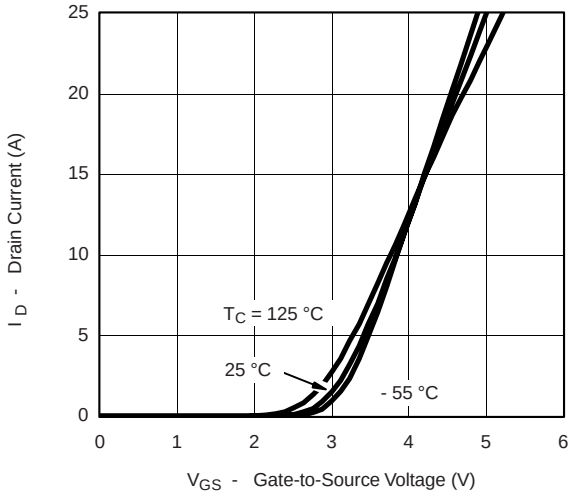


Normalized Thermal Transient Impedance, Junction-to-Case

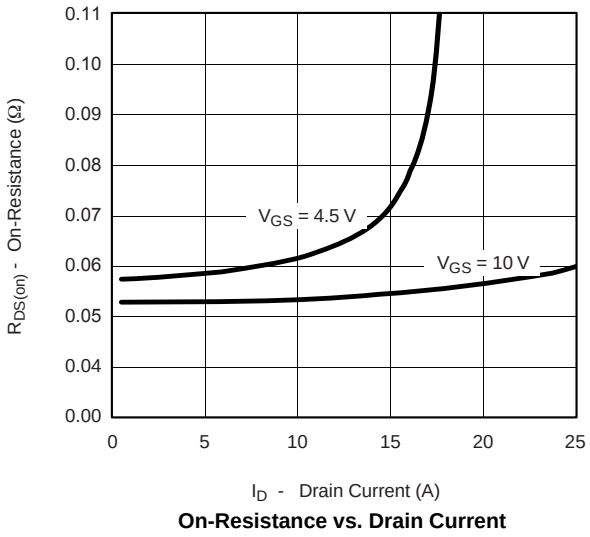
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



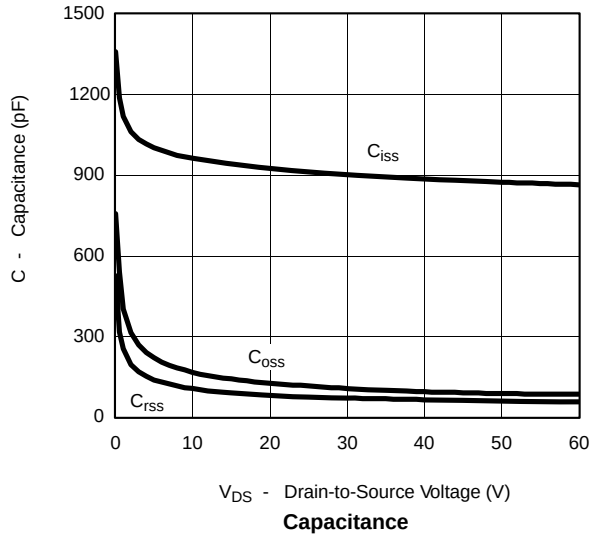
Output Characteristics



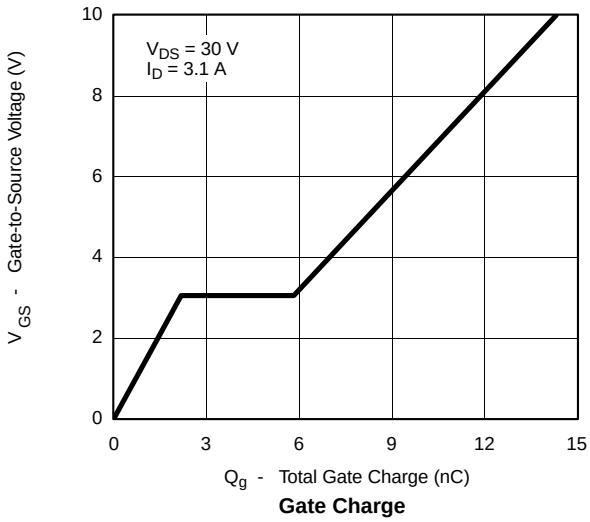
Transfer Characteristics



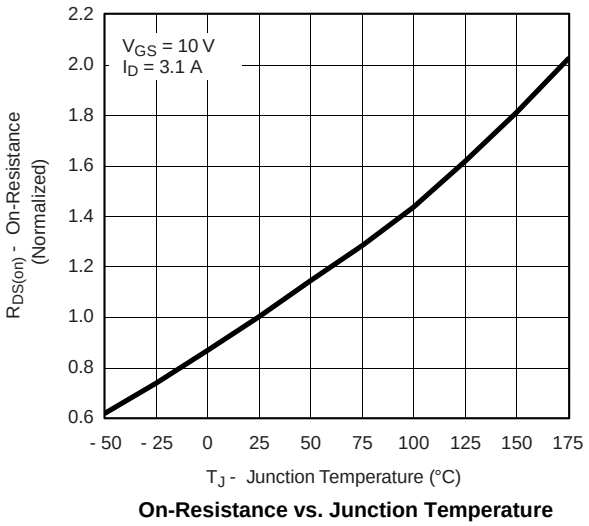
On-Resistance vs. Drain Current



Capacitance

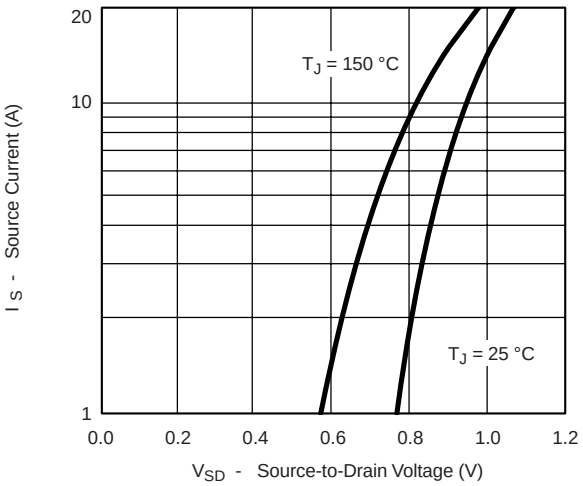


Gate Charge

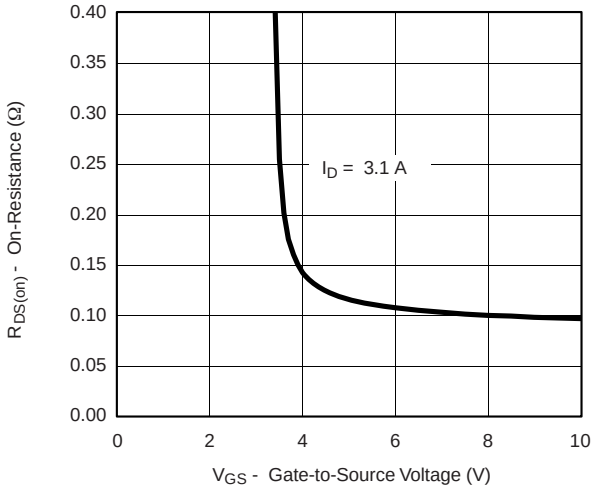


On-Resistance vs. Junction Temperature

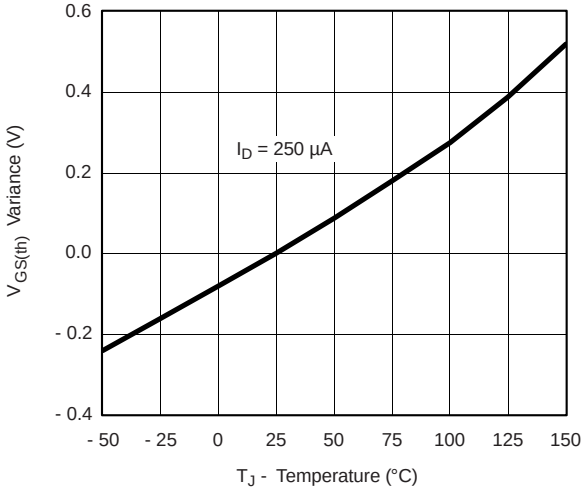
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



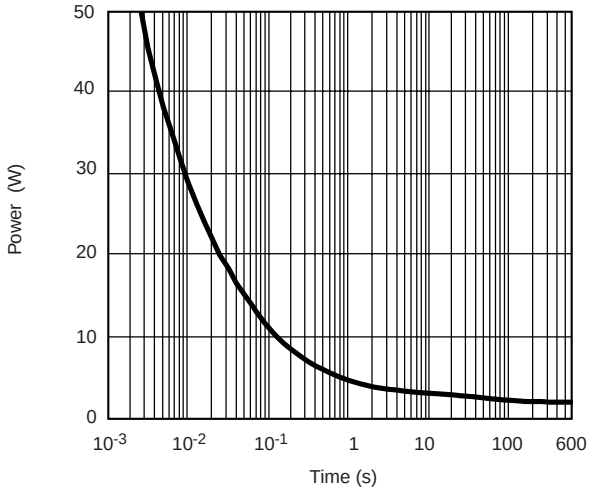
Source-Drain Diode Forward Voltage



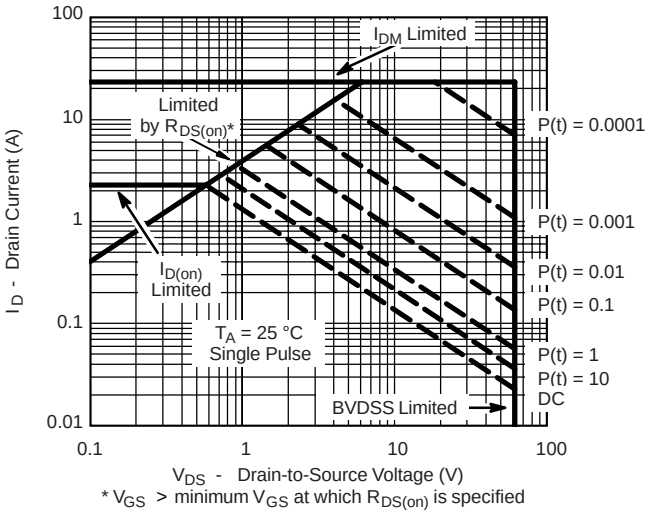
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

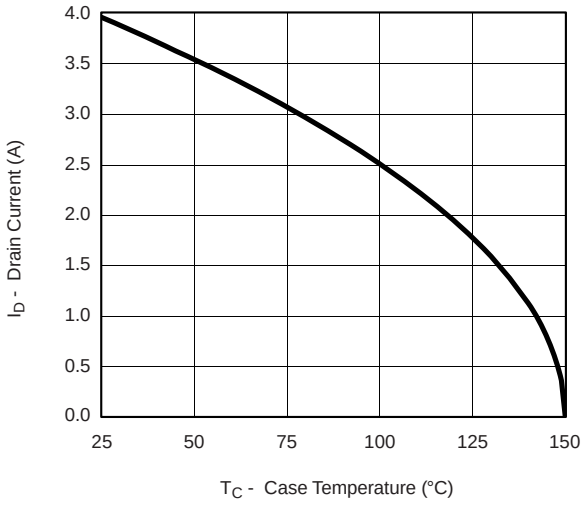


Single Pulse Power

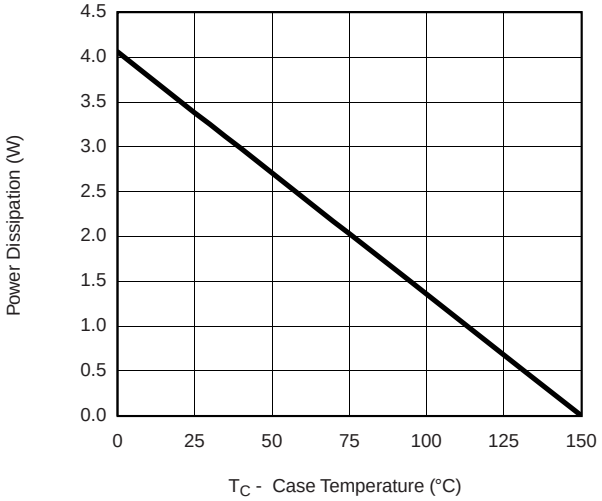


Safe Operating Area, Junction-to-Case

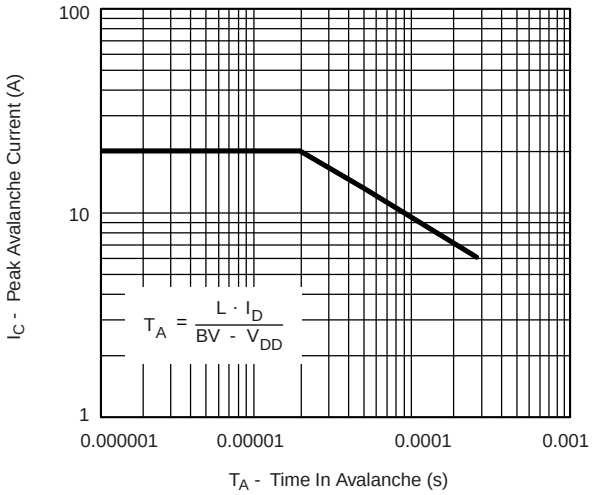
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



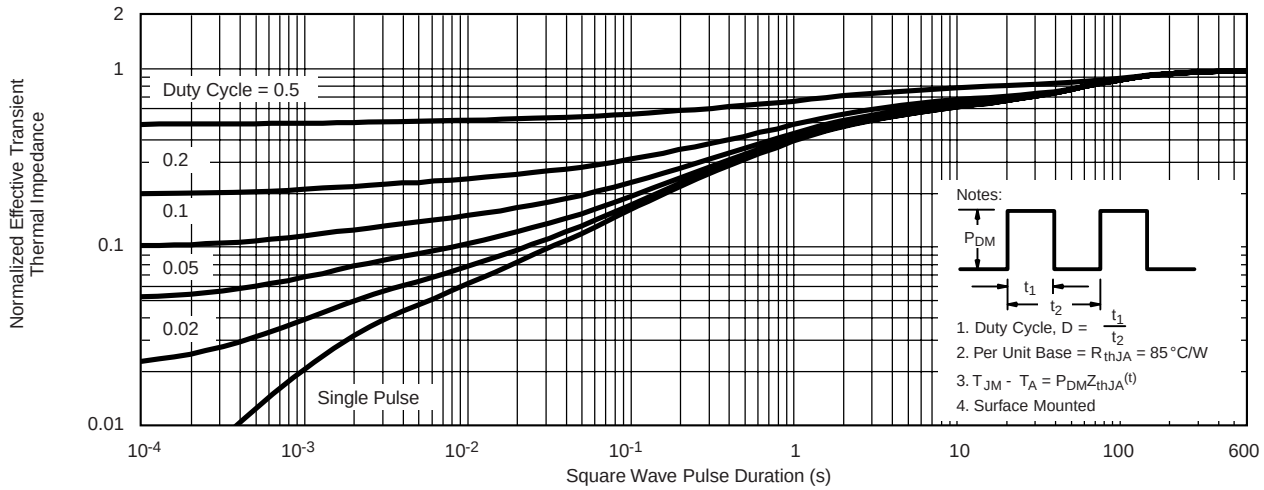
Power Derating, Junction-to-Foot



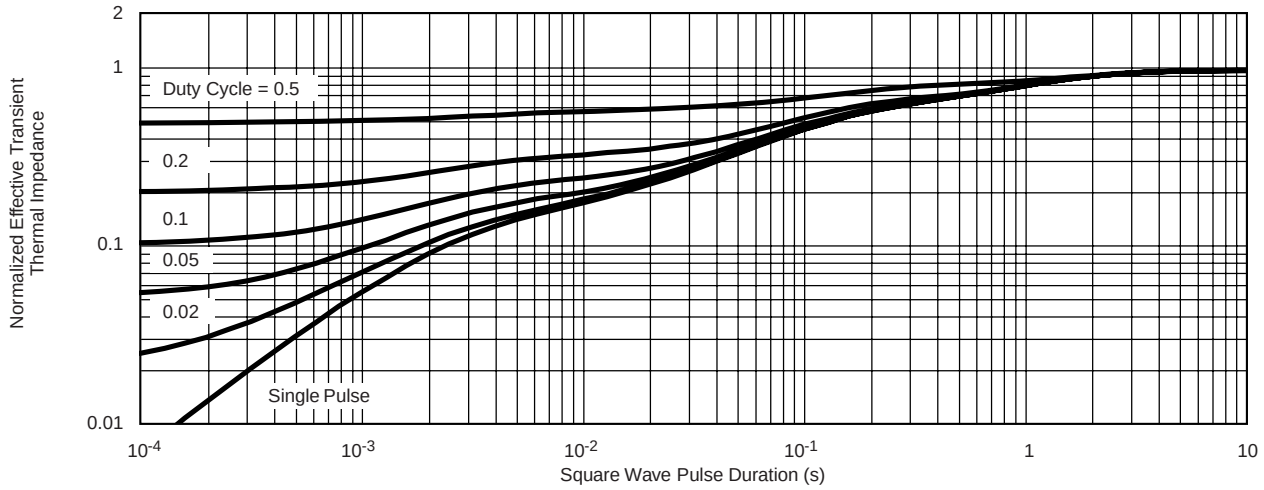
Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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