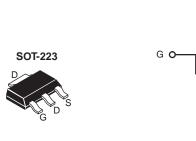


P-Channel 35V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A) ^d	Q _g (Тур.)			
- 35	0.050 at V _{GS} = - 10 V	- 6.2	9.8 nC			
	0.060 at V _{GS} = - 4.5 V	- 5.1	9.0110			



P-Channel MOSFET

D

S

FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Power MOSFET
- 100 % Rg Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Load Switches, Adaptor Switch
 - Notebook PCs

Pb-free
HALOGEN

FREE

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	- 35	V	
Gate-Source Voltage		V _{GS}	GS ± 20		
	T _C = 25 °C		- 6.2		
	T _C = 70 °C	1 . –	- 4.8		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 4.5 ^{a, b}		
	T _A = 70 °C		- 3.4 ^{a, b}		
Pulsed Drain Current	I _{DM}	- 20	Α		
	T _C = 25 °C		- 3.5		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 2.1 ^{a, b}		
Avalanche Current		I _{AS}	- 10		
Single-Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	5	mJ	
	T _C = 25 °C		4.2		
	T _C = 70 °C		2.7		
Maximum Power Dissipation	T _A = 25 °C	P _D	2.5 ^{a, b}	W	
	T _A = 70 °C	1 -	1.6 ^{a, b}		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	40	50	°C/W		
Maximum Junction-to-Foot	Steady State	R _{thJF}	24	30	0/10		

Notes:

a. Surface mounted on 1" x 1" FR4 board.

c. Maximum under steady state conditions is 85 $^{\circ}\text{C/W}.$

d. Based on T_C = 25 °C.

b. t = 10 s.

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static						•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = -250 \mu A$	- 35			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050 A		- 42		m)//00	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		4.6		- mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	- 0.6		- 1.8	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	1	$V_{DS} = -35 V, V_{GS} = 0 V$			- 1	μA	
Zero Gate Voltage Drain Current	IDSS	V_{DS} = - 35 V, V_{GS} = 0 V, T_{J} = 55 °C			- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge$ - 10 V, V_{GS} = - 10 V	- 10			Α	
Drain Courses On Ctota Desistance	Р	V _{GS} = - 10 V, I _D = - 5 A		0.040	0.050		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 4 A		0.048	0.060	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 5 A		14		S	
Dynamic ^b							
Input Capacitance	C _{iss}			970		pF	
Output Capacitance	C _{oss}	V_{DS} = - 20 V, V_{GS} = 0 V, f = 1 MHz		120			
Reverse Transfer Capacitance	C _{rss}			95			
Total Cata Charge	Qg	V_{DS} = - 20 V, V_{GS} = - 10 V, I_D = - 5 A		23	35	nC	
Total Gate Charge				9.8	16		
Gate-Source Charge	Q _{gs}	V_{DS} = - 20 V, V_{GS} = - 4.5 V, I_{D} = - 5 A		3			
Gate-Drain Charge	Q _{gd}			5.2			
Gate Resistance	R _g	f = 1 MHz	1.0	5.5	11	Ω	
Turn-On Delay Time	t _{d(on)}			7	14	_	
Rise Time	t _r	V_{DD} = - 20 V, R_L = 4 Ω		12	24		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 5 Å, V_{GEN} = - 10 V, R_g = 1 Ω		30	60		
Fall Time	t _f			9	18		
Turn-On Delay Time	t _{d(on)}			44	80	ns	
Rise Time	t _r	V_{DD} = - 20 V, R_L = 4 Ω		33	60		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 5 Å, V_{GEN} = - 4.5 V, R_g = 1 Ω		28	55		
Fall Time	t _f			13	25		
Drain-Source Body Diode Characterist	ics			•	•	•	
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 3.5	•	
Pulse Diode Forward Current	I _{SM}				- 20	A	
Body Diode Voltage	V _{SD}	$I_{\rm S}$ = - 2 A, $V_{\rm GS}$ = 0 V		- 0.76	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			27	50	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			19	35	nC	
Reverse Recovery Fall Time	ta	I_F = - 2 A, dl/dt = 100 A/µs, T_J = 25 °C		14			
Reverse Recovery Rise Time		t _b		13		ns	

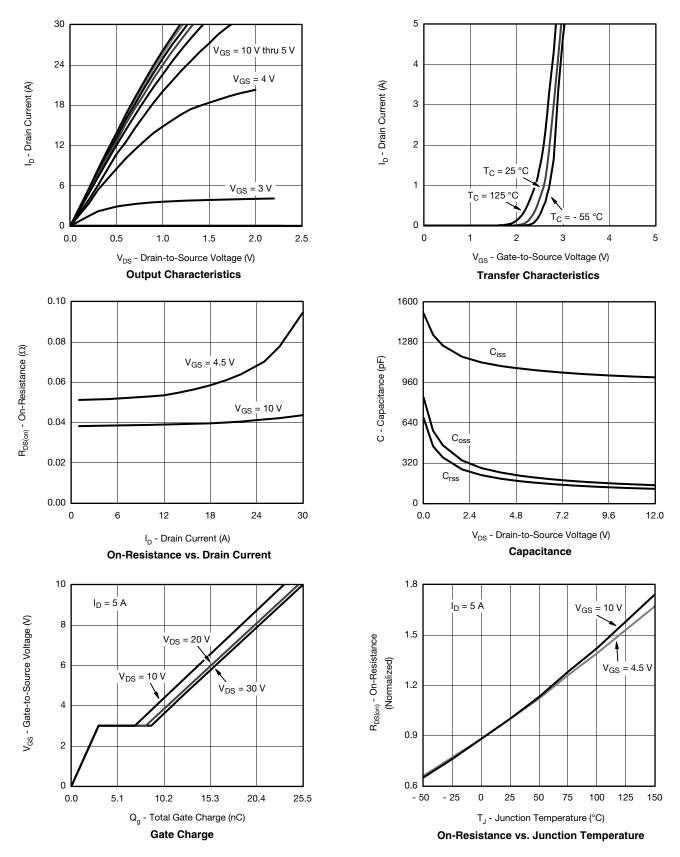
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

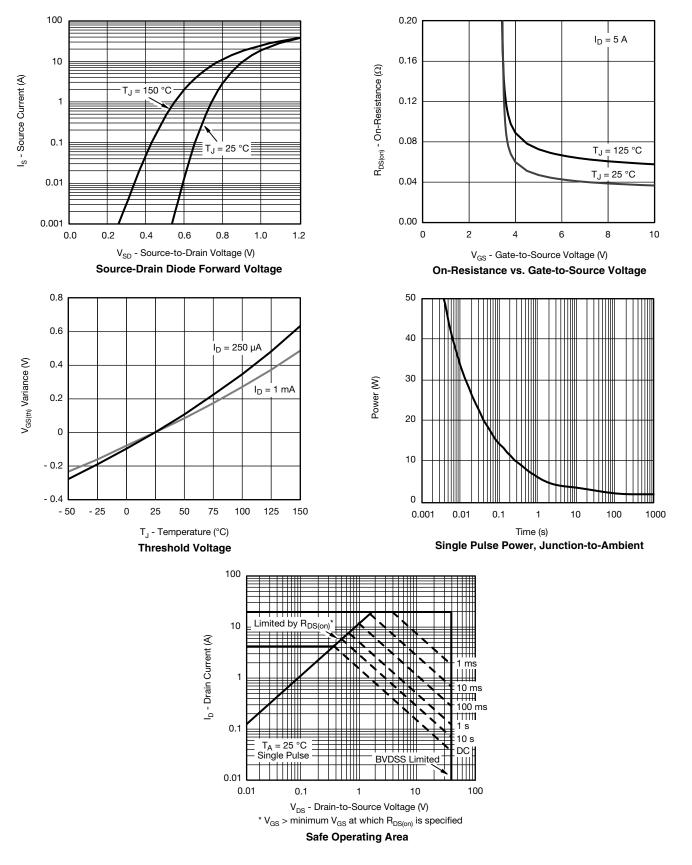
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

emi

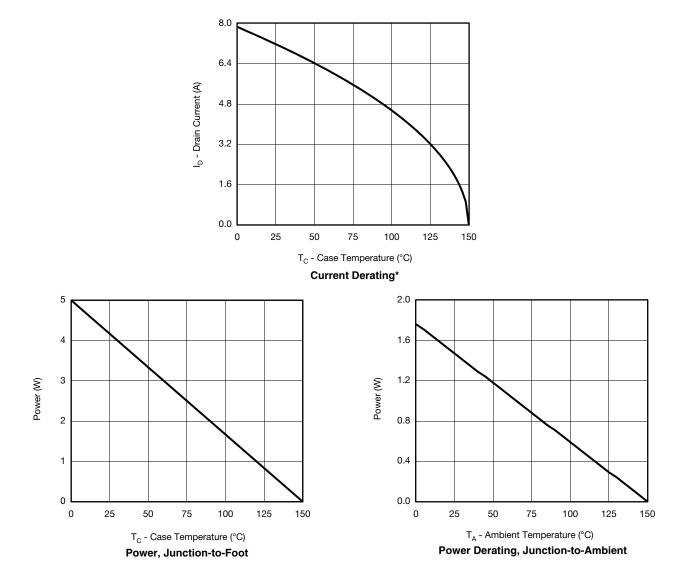






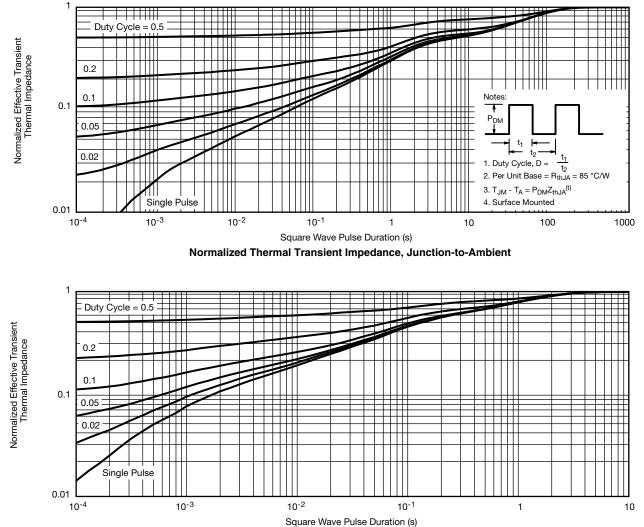






* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

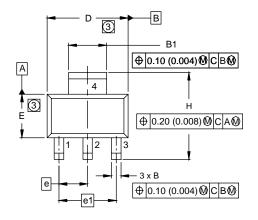


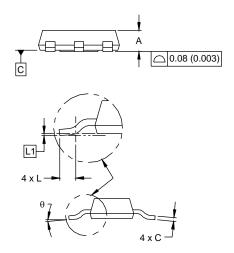


Normalized Thermal Transient Impedance, Junction-to-Foot



SOT-223 (HIGH VOLTAGE)





	MILLIMETERS		INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
A	1.55	1.80	0.061	0.071	
В	0.65	0.85	0.026	0.033	
B1	2.95	3.15	0.116	0.124	
С	0.25	0.35	0.010	0.014	
D	6.30	6.70	0.248	0.264	
E	3.30	3.70	0.130	0.146	
е	2.30 BSC		0.0905 BSC		
e1	4.60 BSC		0.181 BSC		
Н	6.71	7.29	0.264	0.287	
L	0.91	-	0.036	-	
L1	0.061 BSC		0.0024 BSC		
θ	-	10'	-	10'	
ECN: S-82109-Rev. A, 15-S DWG: 5969	Sep-08	•	·	<u>.</u>	

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Dimensions are shown in millimeters (inches).

3. Dimension do not include mold flash.

4. Outline conforms to JEDEC outline TO-261AA.



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