

GUANGDONG VIIYONG ELECTRONIC
TECHNOLOGYCO., LTD.

A104K0603H7R101SKT
(0603, X7R, 0.1 μ F, \pm 10%, 100V)

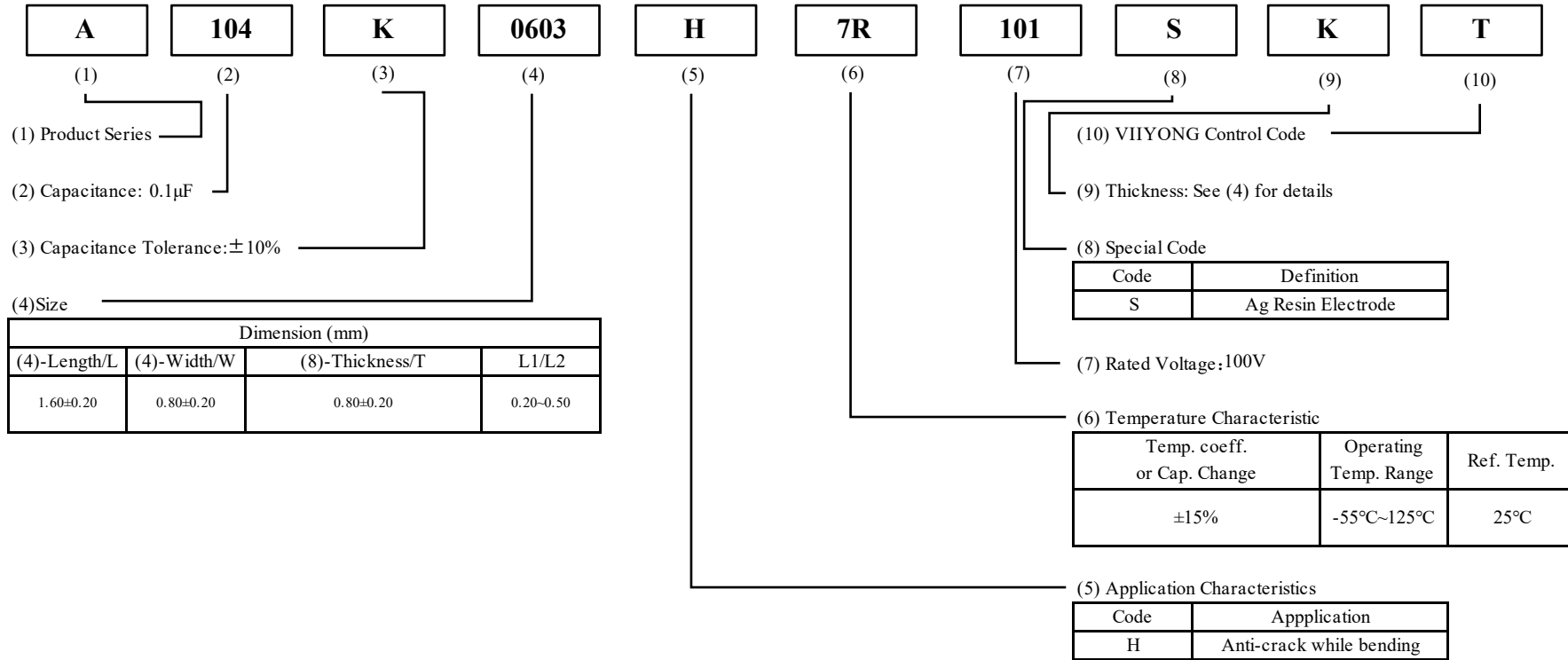
**Product Specification of Automotive Grade Soft Terminal Multi-layer
Ceramic Chip Capacitor for Safety Applications**

The product informations contained in this specification are as of April 1st, 2024, and this specification may be revised or abolished as necessary without notice.
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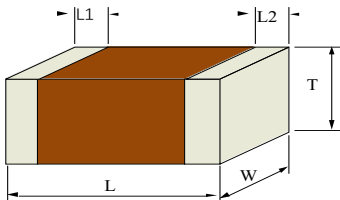
1.Scope

This product specification is applied to Soft Terminal Multi Layer Ceramic Capacitor used for automotive applications such as power train and safety equipment. AEC-Q200 compliant.

2.Part Number System



3.Structure



4.Packaging

Code	Packaging	Quantity
T	7" Reel Paper Tape (W8P4)	4000 pcs./Reel

5.Specifications and Test Methods

NO.	Item	Specification	Test Method (Ref. Standard: AEC-Q200)															
1	Pre-and Post-Stress Electrical Test		It should be tested at 25±5°C.															
2	Heat treatment		Perform a heat treatment at 150+0/-5°C for 1h+/-10min and then let sit for 24+/-2hours at room temperature, then measure.															
3	High Temperature Exposure (Storage)	Appearance: No defects or abnormalities. Capacitance Change: $\leq\pm 10\%$ DF: Within the specified initial value. IR: Within the specified initial value.	Perform per MIL-STD-202 Method108: Solder the capacitor on the test substrate, perform the test under the following conditions. Test Temperature: 150+5/-0°C Duration: 1000hours. Let sit for 24+/-4 hours at room temperature, then measure. Pre-treatment: perform the heat treatment before test.															
4	Temperature Cycling	Appearance: No defects or abnormalities. Capacitance Change: $\leq\pm 10\%$ DF: Within the specified initial value. IR: Within the specified initial value.	Perform per JESD22 Method JA-104: Solder the capacitor on the test substrate, perform the test from step 1 to 4. Cycles:1000. Let sit for 24+/-4 hours at room temperature, then measure. <table border="1" data-bbox="1115 611 1608 767"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> <th>Time(minutes)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>-55+0/-3</td> <td>30+/-3</td> </tr> <tr> <td>2</td> <td>25</td> <td>1</td> </tr> <tr> <td>3</td> <td>125+3/-0</td> <td>30+/-3</td> </tr> <tr> <td>4</td> <td>25</td> <td>1</td> </tr> </tbody> </table> Pre-treatment: perform the heat treatment before test.	Step	Temperature(°C)	Time(minutes)	1	-55+0/-3	30+/-3	2	25	1	3	125+3/-0	30+/-3	4	25	1
Step	Temperature(°C)	Time(minutes)																
1	-55+0/-3	30+/-3																
2	25	1																
3	125+3/-0	30+/-3																
4	25	1																
5	Destructive Physical Analysis	No defects or abnormalities.	Perform visual inspection and sample microscope inspection per ANSI/EIA-469-D-2006.															
6	Moisture Resistance	Appearance: No defects or abnormalities. Capacitance Change: $\leq\pm 12.5\%$ DF: Within the specified initial value. IR: Within the specified initial value.	Perform per MIL-STD-202 Method103: Solder the capacitor on the test substrate, perform the test under the following conditions. Test Temperature: 25°C~65°C Test Humidity: 80%RH~100%RH Duration: Apply the 24h treatment shown in Fig.2, 10 consecutive times. Let sit for 24+/-4 hours at room temperature, then measure. Pre and post-treatment: perform the heat treatment before and after test.															

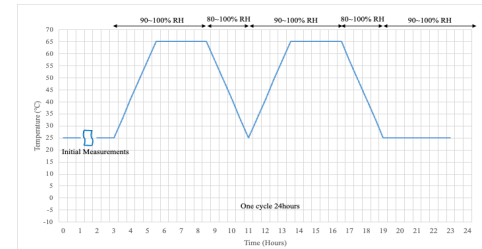


Fig.2 Temperature and Humidity cycle

NO.	Item	Specification	Test Method (Ref. Standard: AEC-Q200)
7	Biased Humidity	Appearance: No defects or abnormalities. Capacitance Change: $\leq \pm 12.5\%$ DF: Within the specified initial value. IR: $\geq 10\%$ of initial value.	Perform per MIL-STD-202 Method103: Solder the capacitor on the test substrate, perform the test under the following conditions. Test Temperature: $85^{\circ}\text{C} \pm 3^{\circ}\text{C}$ Test Humidity: 80%RH~85%RH Test Voltage: The rated voltage and $1.3+0.2/-0\text{Vdc}$ Duration: 1000 ± 12 hours Charge/discharge current: 50mA max. Let sit for 24 ± 4 hours at room temperature, then measure. Pre and post-treatment: perform the heat treatment before and after test.
8	Operational Life	Appearance: No defects or abnormalities. Capacitance Change: $\leq \pm 12.5\%$ DF: Within the specified initial value. IR: $\geq 10\%$ of initial value.	Perform per MIL-STD-202 Method108: Solder the capacitor on the test substrate, perform the test under the following conditions. Test Temperature: Maximum Operating Temperature $\pm 3^{\circ}\text{C}$ Test Voltage: $1.5 \times U_r$ Duration: 1000 ± 12 hours Let sit for 24 ± 4 hours at room temperature, then measure. Pre and post-treatment: perform the heat treatment before and after test.
9	Mechanical Shock	Appearance: No defects or abnormalities. Capacitance Change: Within the specified initial value. DF: Within the specified initial value. IR: Within the specified initial value.	Perform per MIL-STD-202 Method213: Solder the capacitor on the test substrate, perform the test under the following conditions. Wave form: Half-sine Peak Value Velocity: 1500g Duration: 0.5ms Shocks directions and times: Three shocks in each direction should be applied along 3 mutually perpendicular axes of the test specimen (18 shocks).
10	Vibration	Appearance: No defects or abnormalities. Capacitance Change: Within the specified initial value. DF: Within the specified initial value. IR: Within the specified initial value.	Perform per MIL-STD-202 Method204: Solder the capacitor on the test substrate, perform the test under the following conditions. Frequency: 10Hz~2000Hz Peak Value Velocity: 5g Duration: 20minutes Vibration directions and time: This motion should be applied for 12 items in each 3 mutually perpendicular directions (total of 36 times).
11	Resistance to Soldering Heat	Appearance: No defects or abnormalities. Capacitance Change: Within the specified initial value. DF: Within the specified initial value. IR: Within the specified initial value.	Perform per MIL-STD-202 Method210: Preheat the capacitor at 110 to 150°C for 60~120s, then perform the test under the following conditions. Test Method: Solder bath method Soldering Bath Temperature: $260 \pm 5^{\circ}\text{C}$ Duration: 10 ± 1 s Let sit for 24 ± 4 hours at room temperature, then measure. Pre-treatment: perform the heat treatment before test.

NO.	Item	Specification	Test Method (Ref. Standard: AEC-Q200)
12	ESD	Appearance: No defects or abnormalities. Capacitance Change: Within the specified initial value. DF: Within the specified initial value. IR: Within the specified initial value.	Perform per AEC-Q200-002: Test Temperature: 22+/-5°C Test Humidity: 30%RH~60%RH Test Voltage: 2kV(Direct Contact Discharge) Test Method: Two discharges shall be applied to each sample within a sample group, one with a positive polarity and one with a negative polarity. Let sit for 24+/-4 hours at room temperature, then measure. Pre and post-treatment: perform the heat treatment before and after test.
13	Solderability	95% of the terminations is to be soldered evenly and continuously. No cracks are allowed and ceramic exposure $\leq 25\%$.	Perform per J-STD-002: Water Steam: At 100+/-5°C for 4h+/-10min. Aging: 150+/-5°C for 1h+/-10min, cooling time>15min. Immerse the capacitor into a soldering flux consist of 25% rosin ethanol and 75% isopropanol (or ethyl alcohol) for 5s-10s. Test Temperature: Immerse 10mm into a 245°C $\pm 5^\circ$ C Melton tin bath for 5s ± 0.5 s.
14	Appearance	No defects or abnormalities.	Visual inspection under 10x microscope
15	Dimension	Shape and dimension be in accordance Fig.1 and Table 1.	Measuring by gauges with tolerance less than 0.01 mm.
16	Capacitance	Within the specified capacitance and tolerance range.	Temperature: 18~28°C Relative Humidity: $\leq 80\%$ RH Test Frequency: 1kHz $\pm 10\%$ Test Voltage: 1.0 ± 0.2 Vrms
17	DF	DF $\leq 500 \times 10^{-4}$	Temperature: 18~28°C Relative Humidity: $\leq 80\%$ RH Test Frequency: 1kHz $\pm 10\%$ Test Voltage: 1.0 ± 0.2 Vrms
18	Insulation Resistance(IR) (25°C)	Ri $\geq 500\Omega \cdot F/C$	Temperature: 25°C Relative Humidity: $\leq 80\%$ RH Test Voltage: 1.0 \times Ur Duration: 60+/-5s
19	Insulation Resistance(IR) (125°C)	Ri $\geq 10\Omega \cdot F/C$	Temperature: 125°C Test Voltage: 1.0 \times Ur Duration: 60+/-5s

NO.	Item	Specification	Test Method (Ref. Standard: AEC-Q200)												
20	Temperature Characteristics of Capacitance	$\Delta C/C \leq \pm 15\%$	<p>Capacitance should be measured after sit at the temperature for 5 minutes. The reference capacitance is that of Step3 in the following table. Test voltage: $\leq 1.0V_{rms}$ (Refer to the individual data sheet)</p> <table border="1"> <thead> <tr> <th>Step</th> <th>Temp.(°C)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>25±2</td> </tr> <tr> <td>2</td> <td>-55±3</td> </tr> <tr> <td>3</td> <td>25±2</td> </tr> <tr> <td>4</td> <td>125±3</td> </tr> <tr> <td>5</td> <td>25±2</td> </tr> </tbody> </table> <p>Pre-treatment: perform the heat treatment before test.</p>	Step	Temp.(°C)	1	25±2	2	-55±3	3	25±2	4	125±3	5	25±2
Step	Temp.(°C)														
1	25±2														
2	-55±3														
3	25±2														
4	125±3														
5	25±2														
21	Withstanding Voltage	Appearance: No defects or abnormalities.	<p>Perform per IEC 60384-1 / IEC 60384-10 / AEC-Q200: Test Voltage: $2.5 \times U_r$ Duration: 60s Charge/discharge current: 50mA max.</p>												
22	Board Flex	<p>Appearance: No defects or abnormalities. Capacitance Change: $\leq \pm 10\%$ DF: Within the specified initial value. IR: Within the specified initial value.</p>	<p>Perform per AEC-Q200-006: Solder the capacitor on the test substrate (shown in Fig.3), then bend the substrate at 1mm/s to 5mm (shown in Fig.4). Hold for 60+5/-0s, then measure.</p>												
23	Terminal Strength (Adhesion)	<p>Appearance: No defects or abnormalities. Capacitance Change: Within the specified initial value. DF: Within the specified initial value. IR: Within the specified initial value.</p>	<p>Perform per AEC-Q200-006: Solder the capacitor on the test substrate (shown in Fig.3), then apply a push force F (shown in Fig.5). Hold for 60+/-1s, then measure. Adhesion: $F=17.7N$</p>												
24	Ceramic Dielectric strength	Destruction Value: $\geq 20N$	<p>Perform per AEC-Q200-003: Apply a vertical force F (shown in Fig.6), record the force value when the capacitor breaks down.</p>												
25	Temperature shock	<p>Appearance: No defects or abnormalities. Capacitance Change: $\leq \pm 10\%$ DF: Within the specified initial value. IR: Within the specified initial value.</p>	<p>Perform per MIL-STD-202 Method 107: TL: Lower limit temperature TU: Upper limit temperature Resting time at TL or TU: 15min Switch time between TL and TU: Within 20s Cycling: 300</p>												

Board Flex

■ Test substrate

Material: Glass epoxy PCB

Thickness: 0.8mm (0201/0402) or 1.6mm (0603/0805/1206/1210)

■ Land Dimension

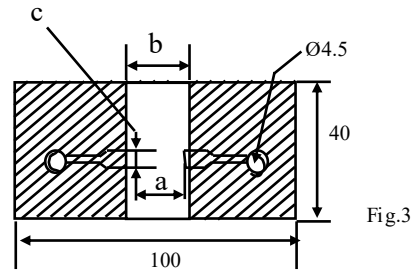


Fig.3

Size	Dimension (mm)		
	a	b	c
0201	0.3	0.9	0.3
0402	0.5	1.5	0.6
0603	0.6	2.2	0.9
0805	0.8	3.0	1.3
1206	2.0	4.4	1.7
1210	2.0	4.4	2.6

■ Pressurization Method

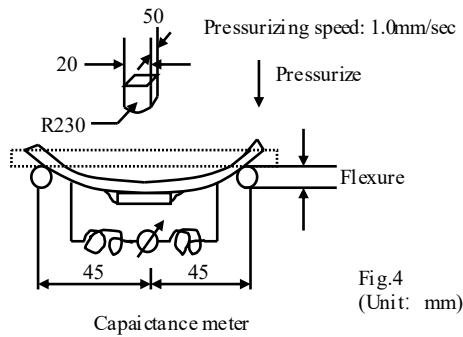


Fig.4
(Unit: mm)

Terminal Strength (Adhesion)

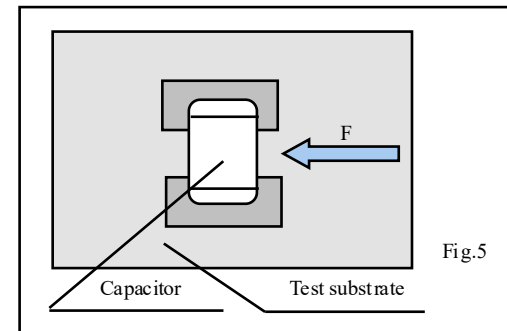


Fig.5

Ceramic Dielectric strength

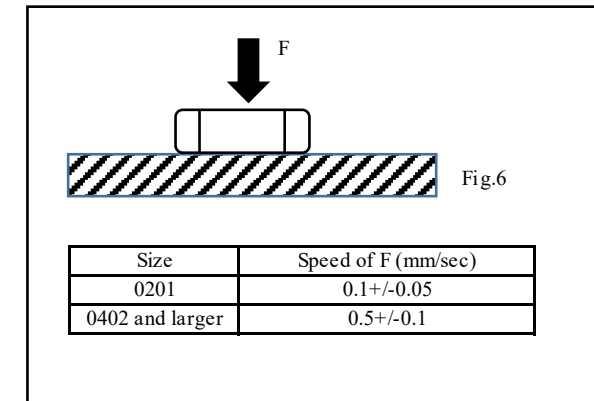
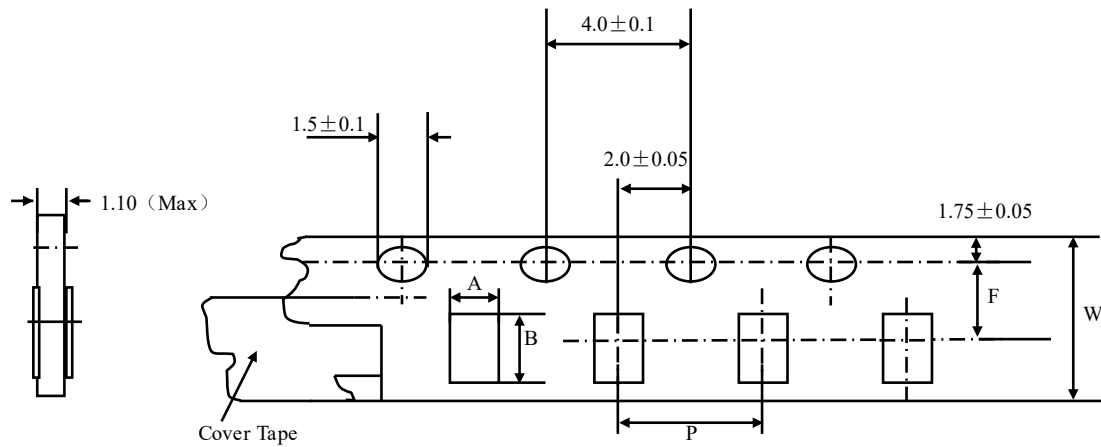


Fig.6

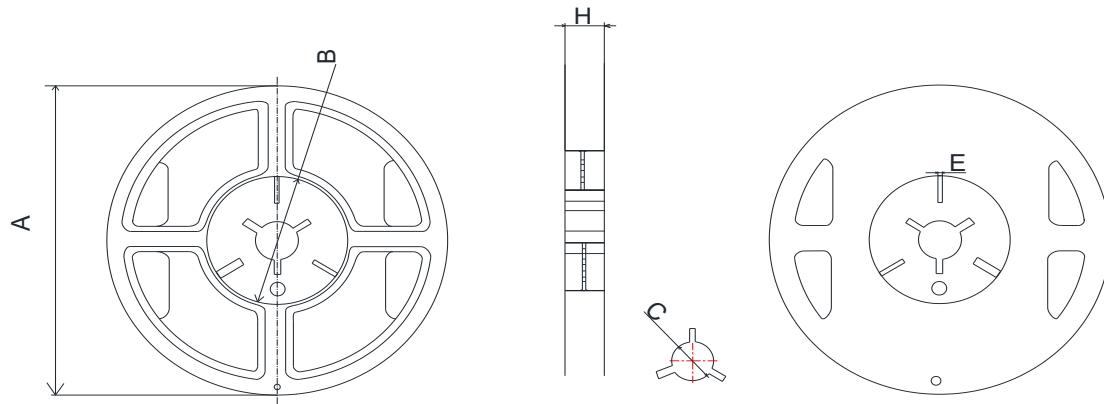
Size	Speed of F (mm/sec)
0201	0.1+/-0.05
0402 and larger	0.5+/-0.1

6. Carrier Tape size



Size	Thickness	Dimension (mm)				
		Width of the square hole /A	Length of the square hole /B	Center distance between positioning hole and square hole /F	Square hole spacing /P	Width of carrier /W
0603	K	1.10±0.10	2.00±0.20	3.50±0.05	4.00±0.10	8.00±0.20

7. Disc size



Disc size	Dimension (mm)				
	A	B	C	E	H
7"	Φ178±2.0	Φ60±2.0	Φ13±1.0	4±1.0	9.5±1.0

■ Storage

1. Storage period: 12 months, otherwise, its solderability must be inspected again.
2. Storage conditions:
 - a. Temperature: lower than 35 °C
 - b. Relative humidity: lower than RH70 %

■ Environmental requirements

All products in this specification comply with the EU RoHS\REACH directive and the relevant requirements of the "VIIYONG Management Guidelines for Restriction of Hazardous Substances".

■ Application

1. Operating Temperature
 - a. Do not use capacitor above the maximum allowable operating temperature.
 - b. Surface temperature including self-heating should be below maximum operating temperature.

2. Operating Voltage

The operating voltage for capacitors must always be lower than their rated voltage.

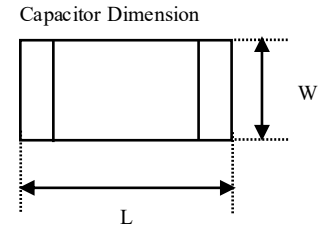
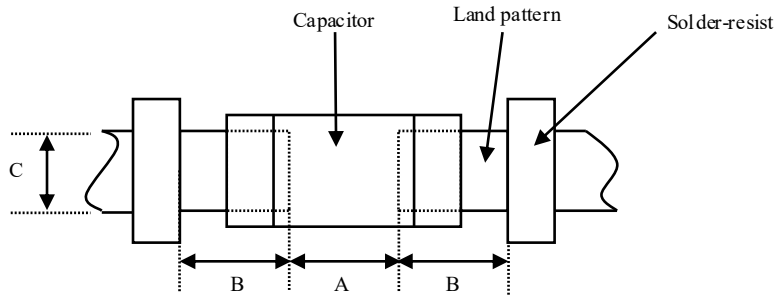
■ PCB Design

1. Design of Land-patterns

When the capacitors are mounted on a PCB, the amount of solder at the terminations has a direct effect on the performance of the capacitors. The greater the amount of solder, the higher the stress on the capacitor. Therefore, when designing land-patterns, it is necessary to consider the appropriate size and configuration of the solder pads.

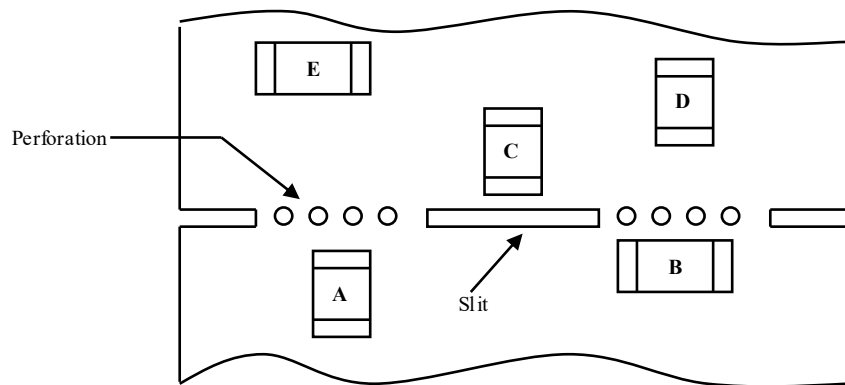
Size and recommended land dimensions for reflow-soldering are shown in the following figure and table. (Unit: mm)

Size	L×W	A	B	C
0201	0.6×0.3	0.20~0.30	0.20~0.35	0.20~0.40
0402	1.0×0.5	0.30~0.50	0.35~0.45	0.45~0.55
0603	1.6×0.8	0.60~0.80	0.60~0.70	0.60~0.80
0805	2.0×1.25	0.80~1.20	0.60~0.70	0.80~1.10
1206	3.2×1.6	2.20~2.40	0.80~0.90	1.00~1.40
1210	3.2×2.5	2.20~2.40	1.00~1.20	1.80~2.30



2. Capacitor Layout on PC Board

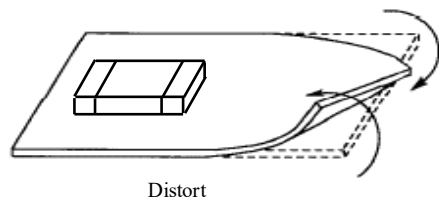
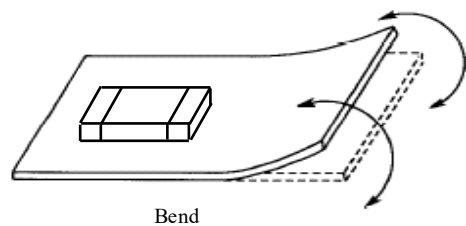
Mechanical stress varies according to the location of capacitors on PC board. The recommendation for better design is as follows:



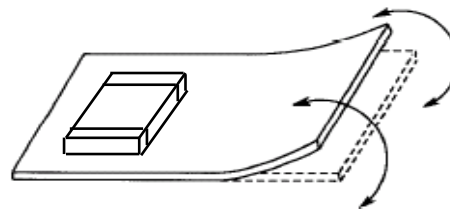
The stress in capacitors is in the following order: $A > B = C > D > E$

Pay attention not to bend or distort the PC board otherwise the capacitor may crack. Please refer to the following examples of good and bad capacitor layout.

a. Not recommended

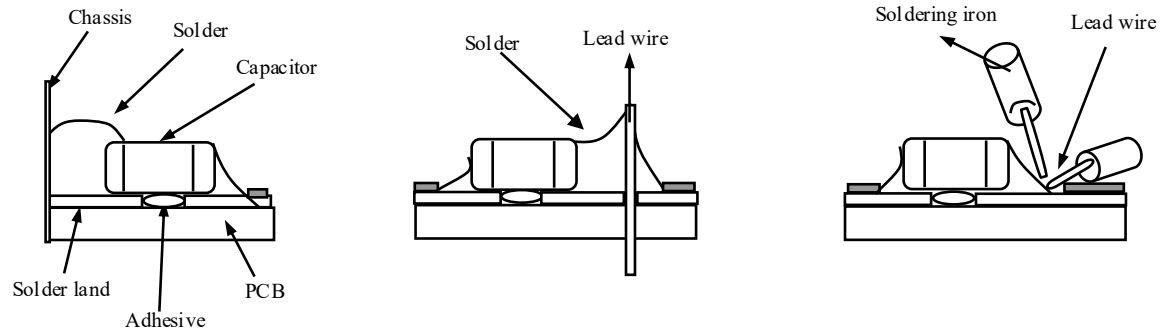


b. Recommended

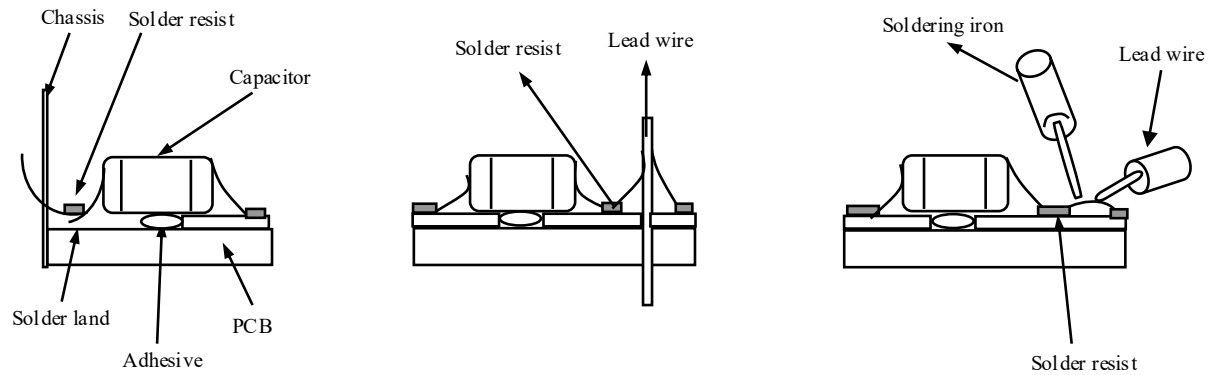


■ Solder Buildup and Soldering Methods

a. Examples of soldering method not recommended



b. Examples of soldering method recommended

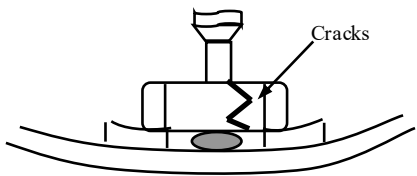
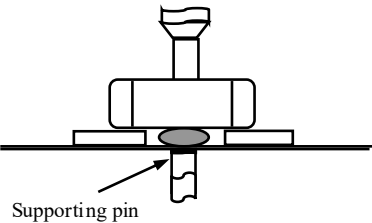
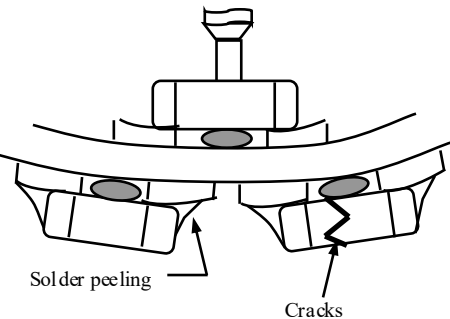
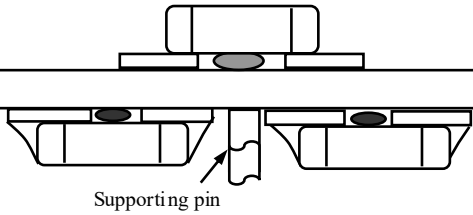


■ Consideration for Automatic Placement

If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitor to result in cracking. Please take following precautions.

- Adjust the bottom dead center of the mounting head to reach on the PC board surface and not press it.
- Adjust the mounting head pressure to be 1 to 3N of static weight .
- To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the PC board.

Please refer to the following samples

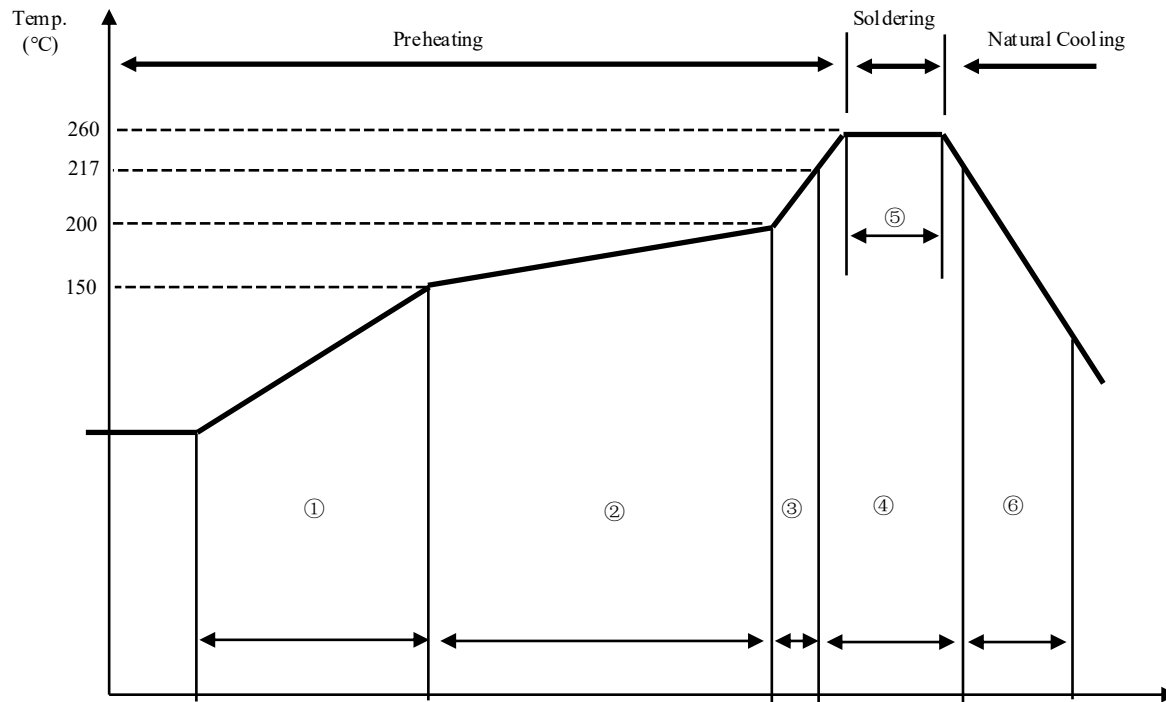
	Not recommended	Recommended
Single-sided	 <p>A cross-sectional diagram showing a chip capacitor being placed on a single-sided PCB. The mounting head is positioned too low, causing the capacitor to be pressed against the board. This results in visible cracks in the capacitor's body, indicated by a jagged line and the label "Cracks".</p>	 <p>A cross-sectional diagram showing a chip capacitor being placed on a single-sided PCB. A supporting pin is inserted from the back of the board to support the capacitor from below. The mounting head is positioned at the correct height, and the capacitor is shown without any damage. The label "Supporting pin" points to the pin.</p>
Double-sided	 <p>A cross-sectional diagram showing a chip capacitor being placed on a double-sided PCB. The mounting head is too low, causing the capacitor to be pressed against the board. This results in visible cracks in the capacitor's body and solder peeling from the board, indicated by jagged lines and the labels "Solder peeling" and "Cracks".</p>	 <p>A cross-sectional diagram showing a chip capacitor being placed on a double-sided PCB. A supporting pin is inserted from the back of the board to support the capacitor from below. The mounting head is positioned at the correct height, and the capacitor is shown without any damage. The label "Supporting pin" points to the pin.</p>

■ Soldering

1. Flux Selection

- It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended.
- Please provide proper amount of flux. Excessive flux must be avoided.
- When water-soluble flux is used, enough washing is necessary.

2. Recommended Soldering Profile



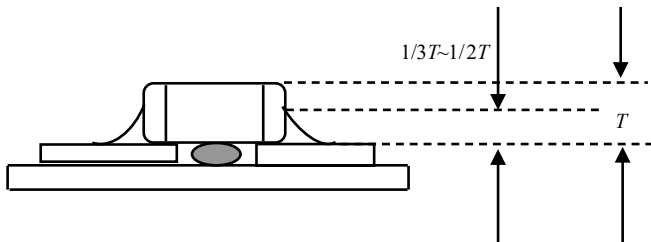
Reflow Soldering Profile

(1) Reflow Soldering Condition

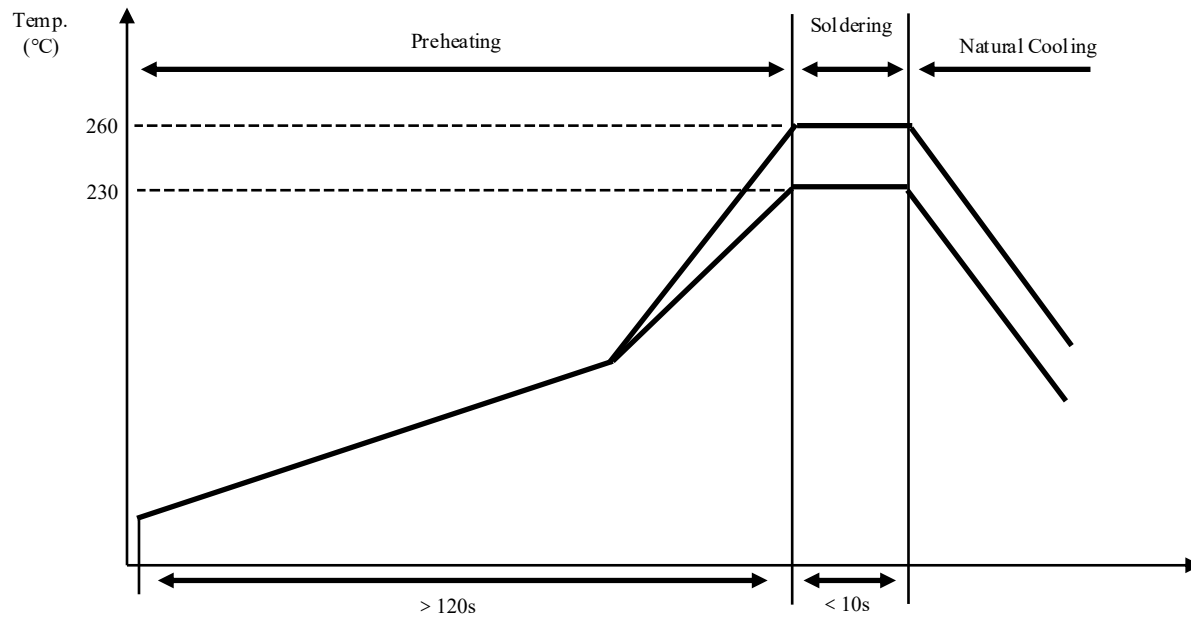
No.	Reflow Soldering zone	Reflow Soldering Condition
①	Preheating 1	Heating rate: $\leq 3^{\circ}\text{C/s}$; Durations: 60s
②	Constant temperature	Heating rate: $\leq 1^{\circ}\text{C/s}$; Durations at $150\sim 200^{\circ}\text{C}$: 60~120s
③	Preheating 2	Heating rate: $1\sim 5^{\circ}\text{C/s}$
④	Soldering 1	Durations at 217°C : 60~150s
⑤	Soldering 2	Durations at $255\sim 260^{\circ}\text{C}$: above 30s
⑥	Natural cooling	Cooling rate: $\leq 6^{\circ}\text{C/s}$

Caution

- a. Excessive solder will induce higher tensile force in chip capacitor when temperature changes and result in cracking. Insufficient solder may detach the capacitor from the PC board. The ideal condition is to have solder mass controlled to $1/2$ to $1/3$ of the thickness of the capacitor.
- b. Soldering duration should be kept as close to recommended times as possible, because excessive duration can detrimentally affect solderability.



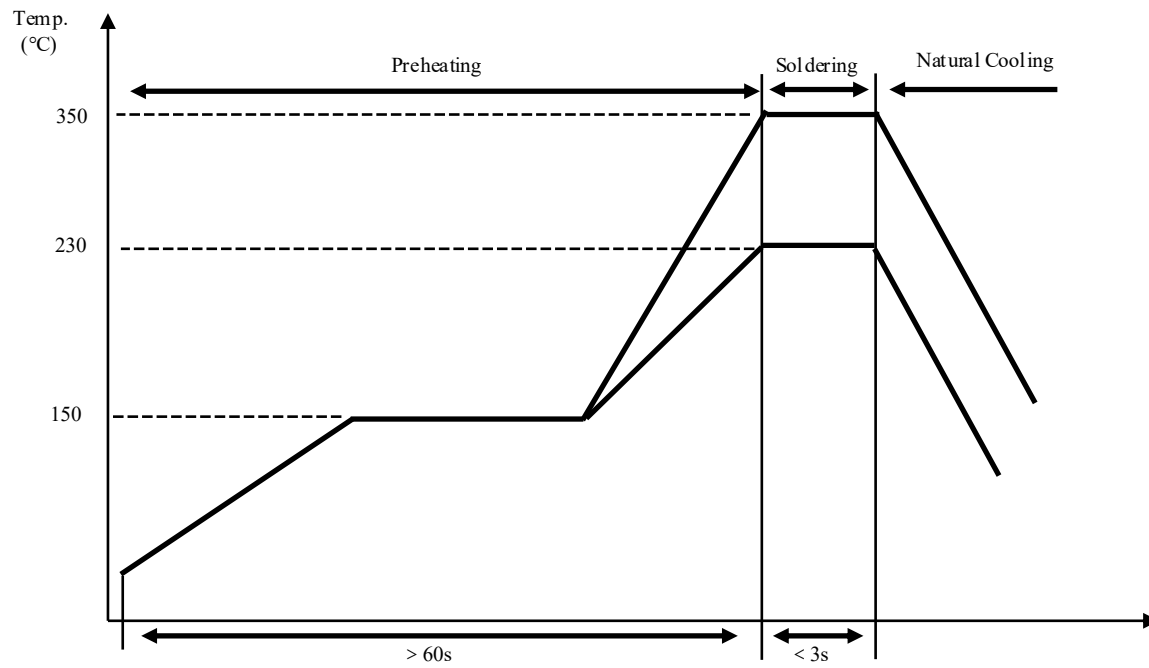
(2) Wave Soldering Condition



Caution :

- a. Make sure the capacitors are preheated sufficiently.
- b. The temperature difference between the capacitor and melted solder should not be greater than 100~130°C.
- c. Wave soldering must not be applied to the capacitors designated as for reflow soldering only

(3) Hand Soldering Condition



Caution:

- a. Use a 20W soldering iron with a maximum tip diameter of 1.0mm.
- b. The soldering iron should not directly touch the capacitor.

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