



Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}$ (Ω)	I _D (A)		
- 20	0.048 at V _{GS} = - 4.5 V	- 6.3		
	0.068 at V _{GS} = - 2.5 V	- 5.3		
	0.090 at V _{GS} = - 1.8 V	- 4.6		

FEATURES

- Halogen-free According to IEC 61249-2-21 **Available**
- TrenchFET® Power MOSFETS: 1.8 V Rated
- ESD Protected: 4500 V
- Ultra Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile

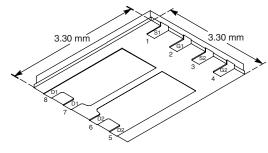




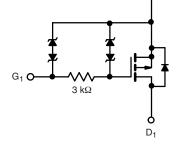
APPLICATIONS

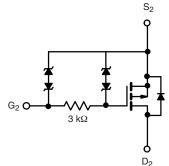
Bidirectional Switch

PowerPAK 1212-8



Bottom View





Ordering Information: Si7901EDN-T1-E3 (Lead (Pb)-free) Si7901EDN-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

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P-Channel MOSFET

ABSOLUTE MAXIMUM RATING	iS $T_A = 25 ^{\circ}C$,	unless otherwis	se noted			
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V_{DS}	- 20		V	
Gate-Source Voltage		V_{GS}	± 12			
Continuous Dunin Courset /T 450 90\2	T _A = 25 °C	l _D	- 6.3	- 4.3	A	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 85 °C		- 4.5	- 3.1		
Pulsed Drain Current		I _{DM}	- 20		А	
Continuous Source Current (Diode Conduction) ^a	I _S	- 2.3	- 1.1		
Maximum Power Dissipation ^a	T _A = 25 °C	- P _D -	2.8	1.3	W	
	T _A = 85 °C		1.5	0.7		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations ^{b,c}		·	260		C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana la disa da Antisa da	t ≤ 10 s	- R _{thJA}	35	44	
Maximum Junction-to-Ambient ^a	Steady State		75	94	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4	5	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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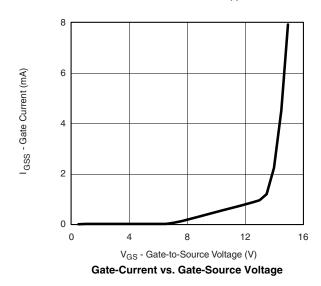
SPECIFICATIONS T _J = 25	°C, unles	s otherwise noted					
Parameter		Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -800 \mu A$	- 0.45		- 1.0	V	
Gate-Body Leakage		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 1.5	νA	
	IGSS	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 10	mA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μΑ	
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 85 °C			- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 20			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 6.3 A		0.041	0.048	Ω	
		V _{GS} = - 2.5 V, I _D = - 5.3 A		0.057	0.068		
		V _{GS} = - 1.8 V, I _D = - 1 A		0.072	0.090		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 6.3 A		14		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 2.3 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Dynamic ^b	•			•			
Total Gate Charge	Qg			12	18		
Gate-Source Charge	Q_{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -6.3 \text{ A}$		2.5		nC	
Gate-Drain Charge	Q _{gd}			2.9			
Turn-On Delay Time	t _{d(on)}			2.5	4		
Rise Time	t _r	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_G = 6 Ω		4	6	μs	
Turn-Off DelayTime	t _{d(off)}			15	23		
Fall Time	t _f			12	18		

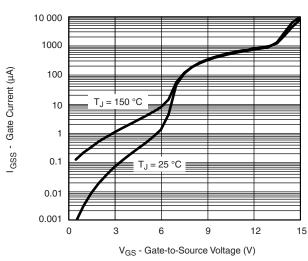
Notes

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25 \, ^{\circ}C$, unless otherwise noted

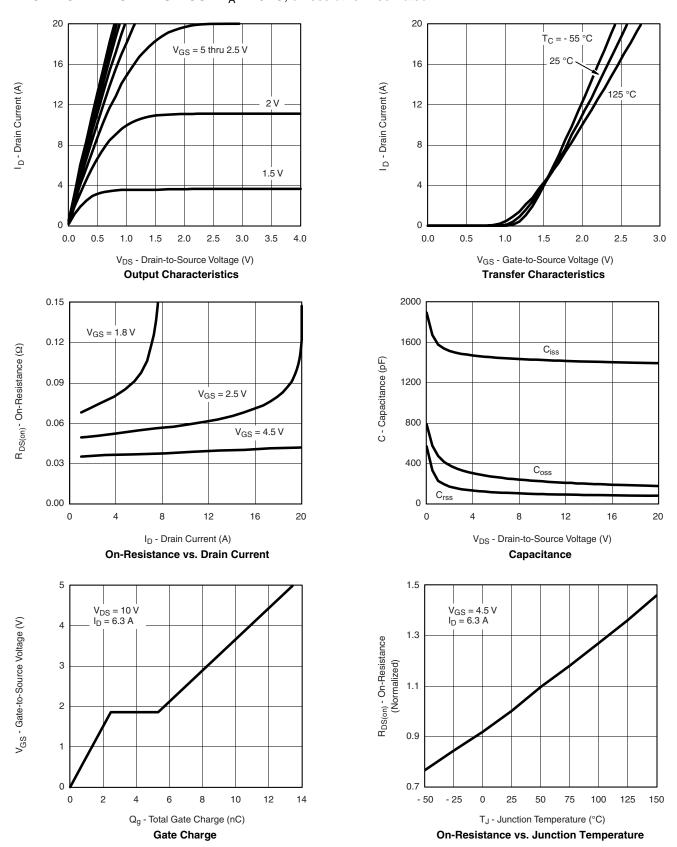




Gate Current vs. Gate-Source Voltage



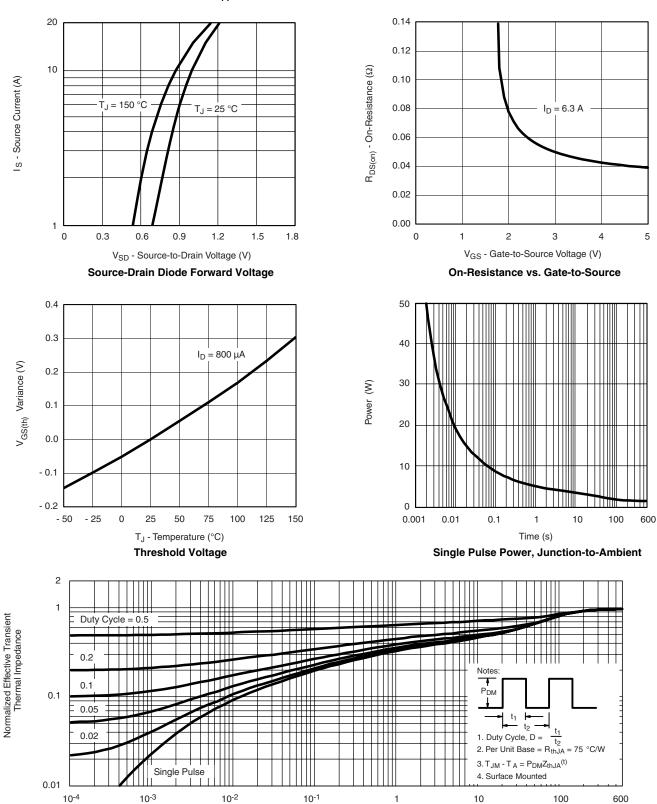
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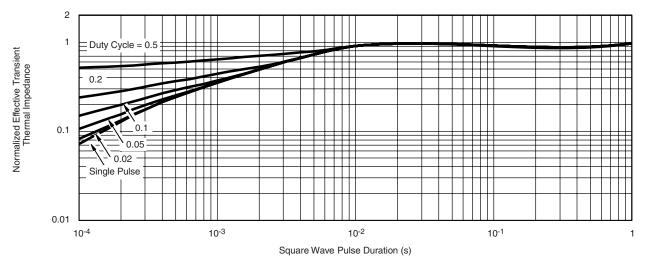
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Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71430.

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