



# **Bi-Directional N-Channel 20-V (D-S) MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
20	0.022 at V <sub>GS</sub> = 4.5 V	10.3			
	0.023 at V <sub>GS</sub> = 4.0 V	10.0	9.1		
	0.026 at V <sub>GS</sub> = 3.1 V	9.4	9.1		
	0.028 at V <sub>GS</sub> = 2.5 V	9.0			

### **FEATURES**

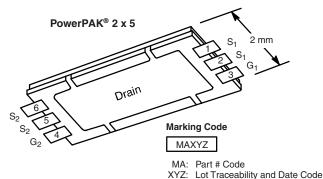
- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET: 2.5 V Rated
- ESD Protected: 4000 V



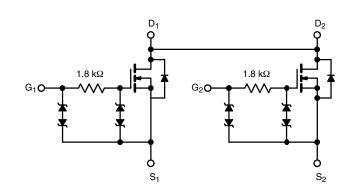
RoHS COMPLIANT

### **APPLICATIONS**

- Battery Protection Circuitry
  - Cell Li-Ion LiB/LiP Battery Packs



Ordering Information: SiF902EDZ-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted						
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	20		٧	
Gate-Source Voltage		V <sub>GS</sub>	± 12			
Continuous Drain Current /T 150 °C\8	T <sub>A</sub> = 25 °C	I <sub>D</sub>	10.3	7.0		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 85 °C		7.4	5.1		
Pulsed Drain Current (V <sub>GS</sub> = 8 V)		I <sub>DM</sub>	40		A	
Continuous Diode Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	3.1	1.5		
Mariana Barra Biraina in a	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5	1.6	W	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 85 °C	] 'D	1.8	0.86	] vv	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 10 s	R <sub>thJA</sub>	30	36	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		61	76		
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	4.8	6.0		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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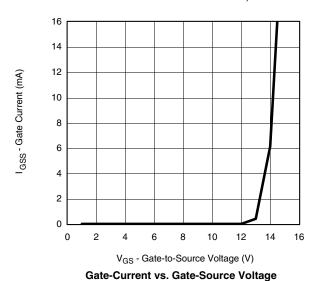
<b>SPECIFICATIONS</b> T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.6		1.5	V	
Gate-Body Leakage	1	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 10		
	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 500		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	μΑ	
	I <sub>DSS</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			5	1	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	40			Α	
		$V_{GS} = 4.5 \text{ V}, I_D = 7.0 \text{ A}$		0.018	0.022	Ω	
	R <sub>DS(on)</sub>	$V_{GS} = 4.0 \text{ V}, I_D = 6.5 \text{ A}$		0.019	0.023		
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = 3.1 \text{ V}, I_D = 4.0 \text{ A}$		0.021	0.026		
		$V_{GS} = 2.5 \text{ V}, I_D = 3.5 \text{ A}$		0.023	0.028		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 7.0 \text{ A}$		38		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 3.1 A, V <sub>GS</sub> = 0 V		0.76	1.1	V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg			9.1	14	nC	
Gate-Source Charge	Q <sub>gs</sub>	$Q_{gs}$ $V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 7.0 \text{ A}$		1.9			
Gate-Drain Charge	Q <sub>gd</sub>			2.7			
Turn-On Delay Time	t <sub>d(on)</sub>			1.7	2.6		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 10 $\Omega$		2.3	3.5		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 1$ A, $V_{GEN}=4.5$ V, $R_g=6~\Omega$		1.1	1.7	μs	
Fall Time	t <sub>f</sub>			4.4	6.6		

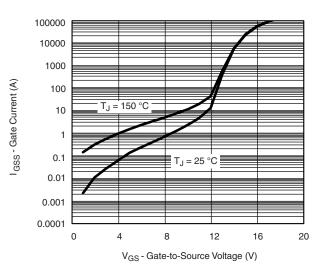
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

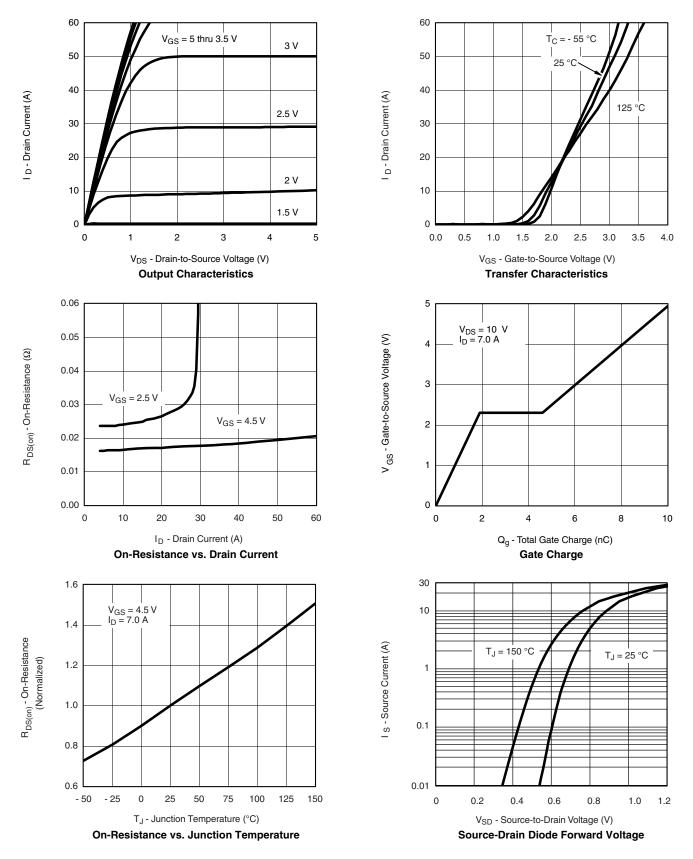




Gate Current vs. Gate-Source Voltage



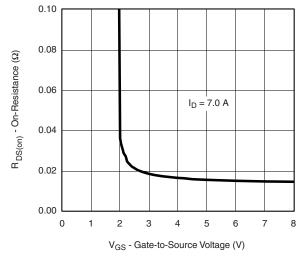
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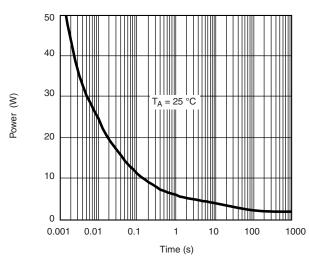
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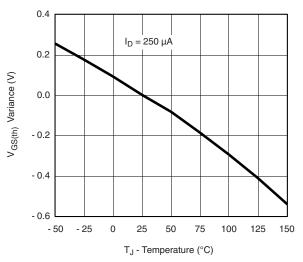
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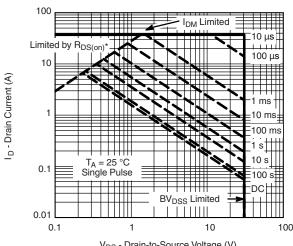
### On-Resistance vs. Gate-to-Source Voltage



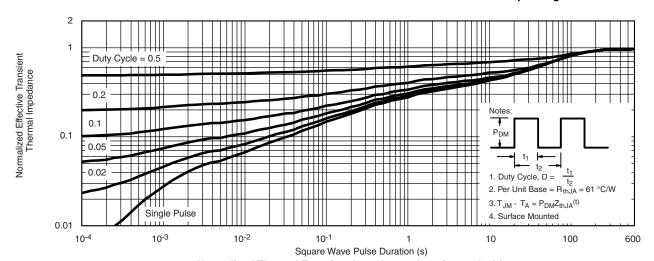
Single Pulse Power, Junction-to-Ambient



### **Threshold Voltage**



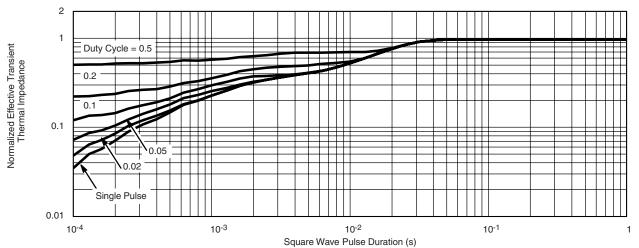
$$\begin{split} &V_{DS}\text{ - Drain-to-Source Voltage (V)}\\ ^*V_{GS}\text{ > minimum }V_{GS}\text{ at which }R_{DS(on)}\text{ is specified}\\ &\textbf{Safe Operating Area} \end{split}$$



Normalized Thermal Transient Impedance, Junction-to-Ambient



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?72987">https://www.vishay.com/ppg?72987</a>.

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