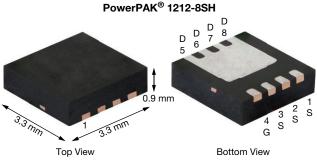
SiSH106DN

www.vishay.com

Vishay Siliconix

N-Channel 20 V (D-S) Fast Switching MOSFET



PRODUCT SUMMARY

 $R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V $R_{DS(on)}$ max. (Ω) at V_{GS} = 2.5 V

V_{DS} (V)

 $I_D(A)$

Q_g typ. (nC)

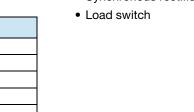
Configuration

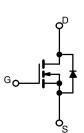
FEATURES

- TrenchFET[®] power MOSFET
- 2.5 V rated R_{DS(on)}
- PWM optimized
- 100 % R_a tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

Synchronous rectification





N-Channel MOSFET

Document Number: 79358

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH106DN-T1-GE3

20 0.0062

0.0098

17.5

19.5

Single

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unle	ss otherwise r	noted)			
PARAMETER		SYMBOL	10 s	STEADY STATE	UNIT	
Drain-source voltage		V _{DS}	20	20	V	
Gate-source voltage		V _{GS}	± 12	± 12		
Continuous drain current (T,I = 150 °C) ^a	T _A = 25 °C		19.5	12.5		
Continuous drain current $(1_j = 150^{-1}C)^{-1}$	T _A = 70 °C	I _D	15.6	10		
Pulsed drain current		I _{DM}	60	60	А	
Continuous source current (diode conduction) a		I _S	3.2	1.3		
Single avalanche current	L = 0.1 mH	I _{AS}	30	30		
Single avalanche energy	L = 0.1 MH	E _{AS}	45	45	mJ	
Maximum neuror dissinction a	T _A = 25 °C	P _D	3.8	1.5	W	
Maximum power dissipation ^a	T _A = 70 °C		2	0.8		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		0°	
Soldering recommendations (peak temperature)	b, c			260	-0	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction to ambient a	t ≤ 10 s	Р	24	33	
Maximum junction-to-ambient ^a	Steady state	R _{thJA}	65	81	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.9	2.4	

Notes

a. Surface mounted on 1" x 1" FR4 board

See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at b. the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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COMPLIANT HALOGEN FREE

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SPECIFICATIONS ($T_J = 25 \circ C$	C, unless otl	herwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	0.6	-	1.5	V	
Gate-body leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$	-	-	± 100	nA	
Zero gate voltage drain current		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA	
Zero gate voltage drain current	IDSS	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	-	-	5	μΑ	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}$	40	-	-	А	
Drain-source on-state resistance ^a	D	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 19.5 \text{ A}$	-	0.0051	0.0062	Ω	
Drain-source on-state resistance "	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 15.5 \text{ A}$	-	0.0081	0.0098	Ω	
Forward transconductance a	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 19.5 \text{ A}$	-	105	-	S	
Diode forward voltage ^a	V _{SD}	$I_{S} = 3.2 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.8	1.2	V	
Dynamic ^b							
Total gate charge	Qg		-	17.5	27		
Gate-source charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 19.5 \text{ A}$ -	6.6	-	nC		
Gate-drain charge	Q _{gd}		-	2.8	-		
Gate resistance	Rg	f = 1 MHz	0.7	1.4	2.1	Ω	
Turn-on delay time	t _{d(on)}		-	25	40		
Rise time	t _r	V_{DD} = 10 V, R_{L} = 10 Ω	-	15	25		
Turn-off delay time	t _{d(off)}	$I_D \cong 1$ Å, $V_{GEN} = 10$ V, $R_g = 6 \Omega$	-	50	75	ns	
Fall time	t _f		-	12	20		
Source-drain reverse recovery time	t _{rr}	I _F = 3.2 A, di/dt = 100 A/μs	-	30	60		

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

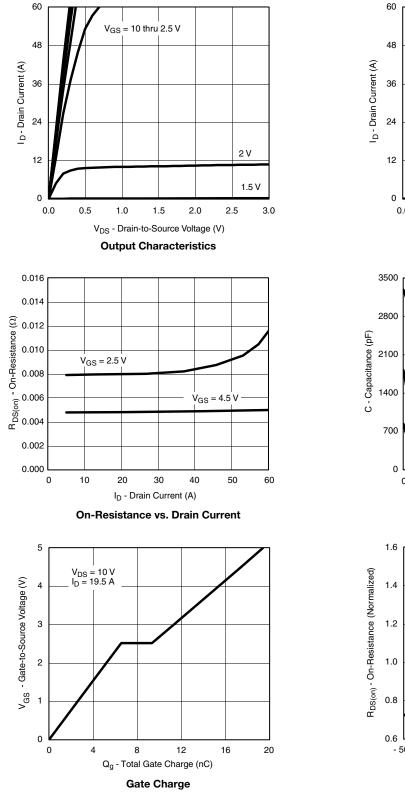
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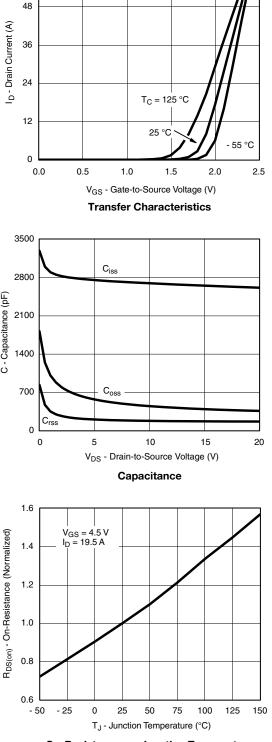


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





On-Resistance vs. Junction Temperature

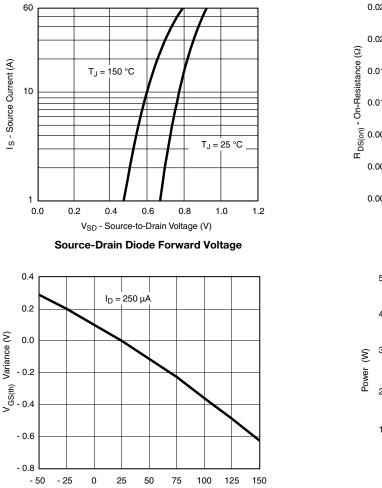
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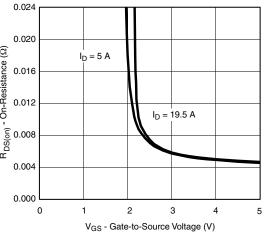
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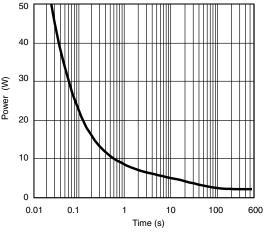
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



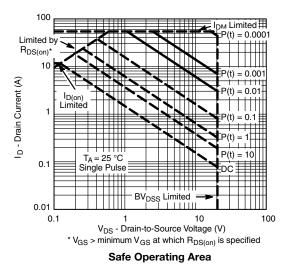




On-Resistance vs. Gate-to-Source Voltage

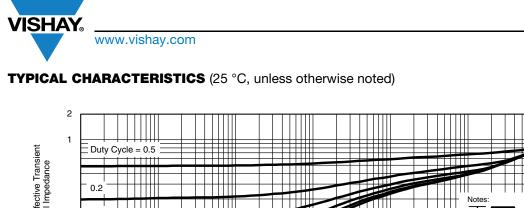


Single Pulse Power, Junction-to-Ambient



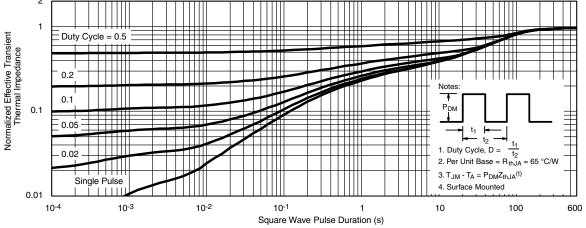
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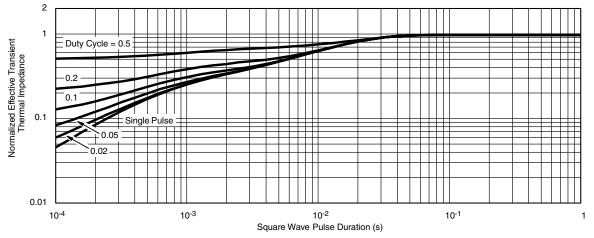




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Normalized Thermal Transient Impedance, Junction-to-Ambient



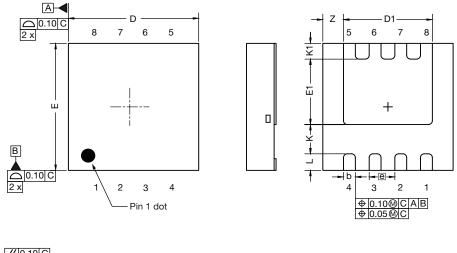
Normalized Thermal Transient Impedance, Junction-to-Case

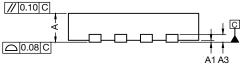
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Case Outline for PowerPAK[®] 1212-SWLH and PowerPAK[®] 1212-8SH

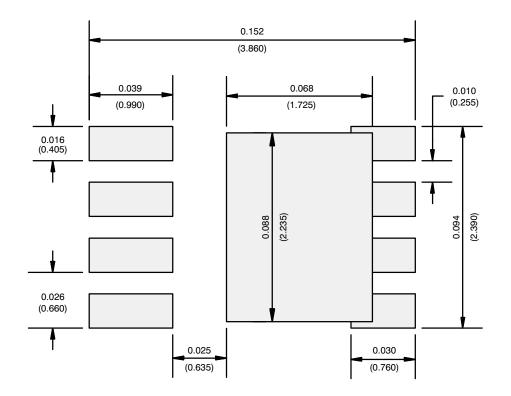




MIN. NOM. 0.032 0.035 0.000 - 0.008 ref. 0.012	MAX. 0.038 0.002		
0.000 - 0.008 ref. 0.010 0.012	0.002		
0.008 ref. 0.010 0.012			
0.010 0.012	0.014		
	0.014		
	0.014		
0.126 0.130	0.134		
0.085 0.089	0.093		
0.126 0.130	0.134		
0.063 0.067	0.071		
0.026 bsc.			
0.030 ref.			
0.016 ref.			
0.013 0.017	0.021		
0.021 ref.			
	0.013 0.017		



RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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