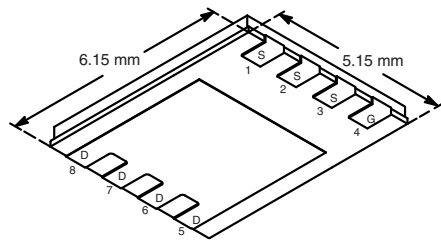




N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
100	0.0305 at $V_{GS} = 10$ V	22	9.5 nC
	0.033 at $V_{GS} = 7.5$ V	21	
	0.043 at $V_{GS} = 4.5$ V	18.5	

PowerPAK® SO-8



Bottom View

Ordering Information: Si7454CDP-T1-GE3 (Lead (Pb)-free and Halogen-free)

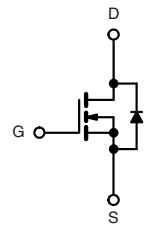
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- DC/DC Primary Side Switch
- Telecom/Server 48 V, Full/Half-Bridge dc-to-dc
- Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	100	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	22	A
		$T_C = 70$ °C	17.6	
		$T_A = 25$ °C	8.1 ^{b, c}	
		$T_A = 70$ °C	6.5 ^{b, c}	
Pulsed Drain Current	I_{DM}	40		
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	22	
		$T_A = 25$ °C	3.7 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	15		
Single Pulse Avalanche Energy	E_{AS}	11.2	mJ	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	29.7	W
		$T_C = 70$ °C	19	
		$T_A = 25$ °C	4.1 ^{b, c}	
		$T_A = 70$ °C	2.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	24	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3.3	4.2	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 10$ s.d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 70 °C/W.

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		47		mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.4			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.2		2.8	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA	
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	20			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.0252	0.0305	Ω	
		$V_{GS} = 7.5\text{ V}$, $I_D = 8\text{ A}$		0.027	0.033		
		$V_{GS} = 4.5\text{ V}$, $I_D = 6\text{ A}$		0.0345	0.043		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 10\text{ A}$		20		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		580		pF	
Output Capacitance	C_{oss}			347			
Reverse Transfer Capacitance	C_{rss}			24			
Total Gate Charge	Q_g	$V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		12.8	19.5	nC	
		$V_{DS} = 50\text{ V}$, $V_{GS} = 7.5\text{ V}$, $I_D = 10\text{ A}$		9.8	15		
Gate-Source Charge	Q_{gs}	$V_{DS} = 50\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$		6.3	9.5		
Gate-Drain Charge	Q_{gd}			1.8			
Gate Resistance	R_g			2.9			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$, $R_L = 5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		0.8	3.8	7.6	Ω
Rise Time	t_r			8	16		
Turn-Off Delay Time	$t_{d(off)}$			12	24		
Fall Time	t_f			16	32		
Turn-On Delay Time	$t_{d(on)}$		$V_{DD} = 50\text{ V}$, $R_L = 5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 7.5\text{ V}$, $R_g = 1\text{ }\Omega$		10	20	
Rise Time	t_r				10	20	
Turn-Off Delay Time	$t_{d(off)}$				12	24	
Fall Time	t_f				17	34	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			22	A	
Pulse Diode Forward Current ^a	I_{SM}				40		
Body Diode Voltage	V_{SD}	$I_S = 4\text{ A}$		0.78	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$		31	62	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			28	56	nC	
Reverse Recovery Fall Time	t_a			15		ns	
Reverse Recovery Rise Time	t_b			16			

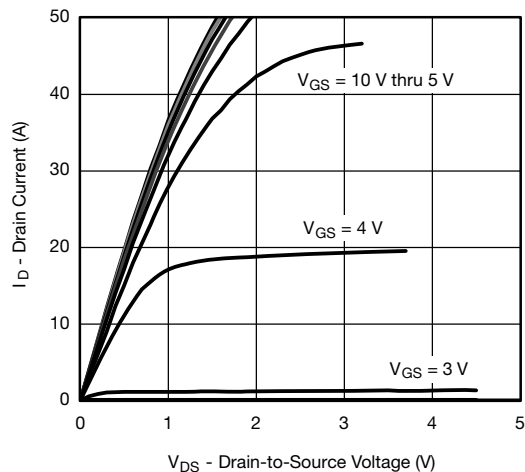
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

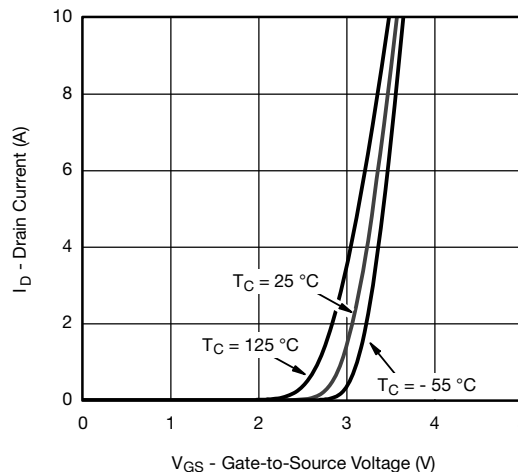
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



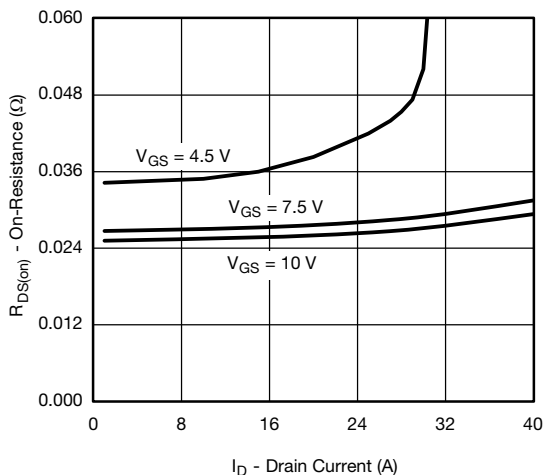
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



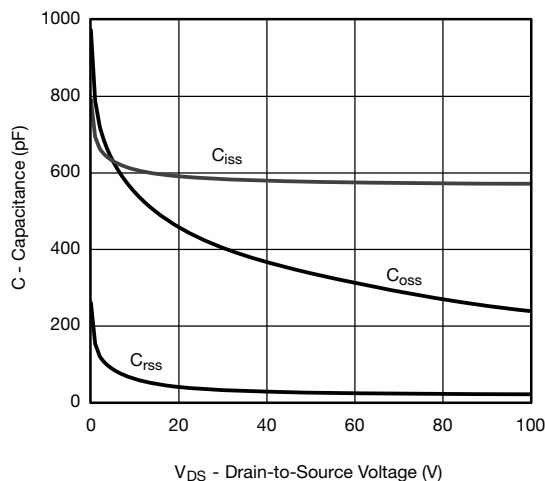
Output Characteristics



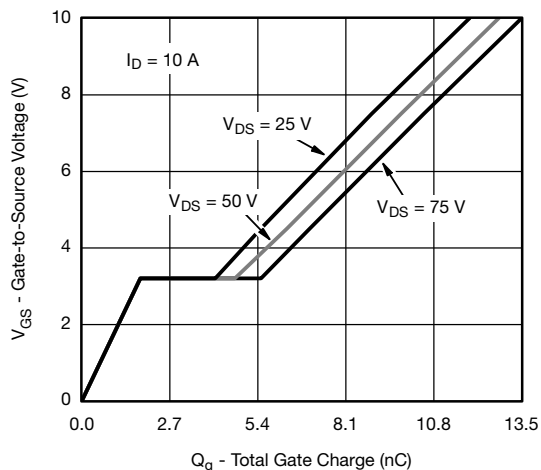
Transfer Characteristics



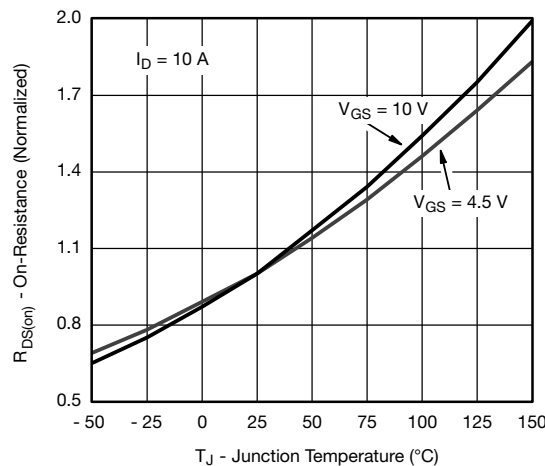
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



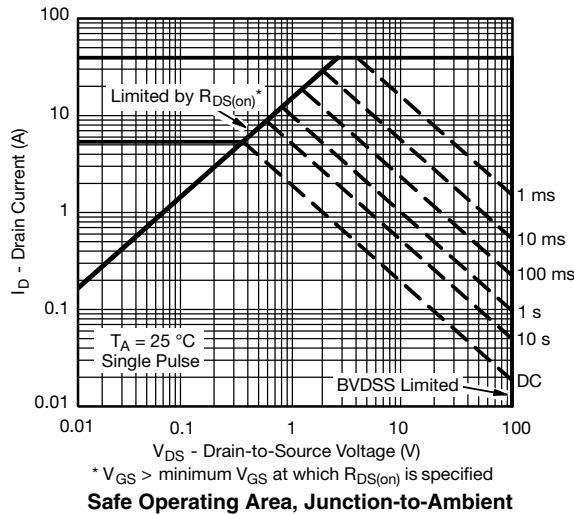
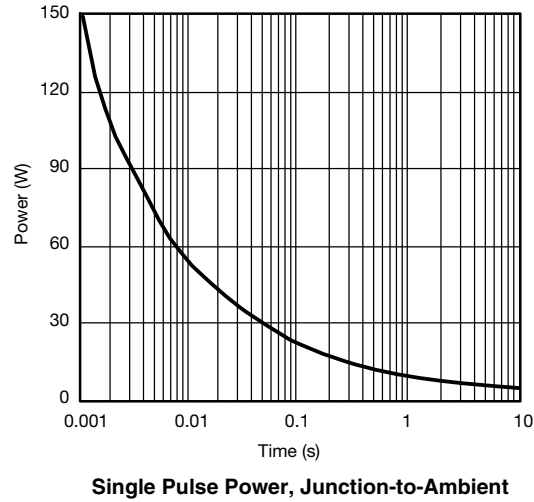
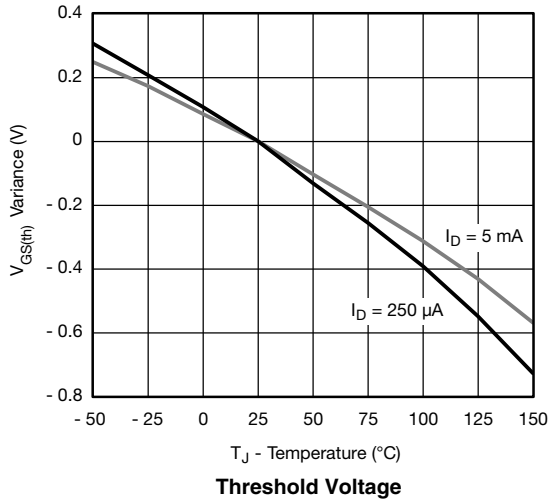
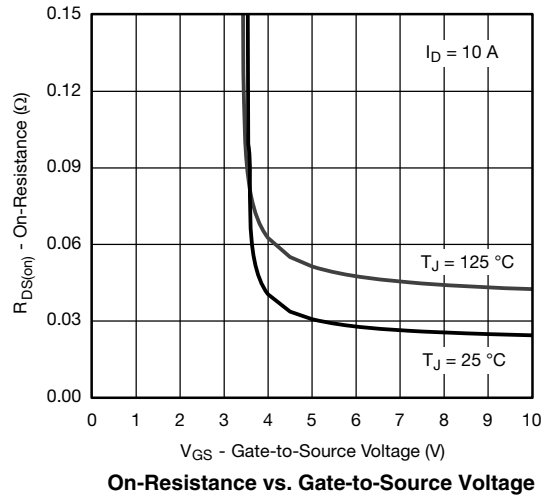
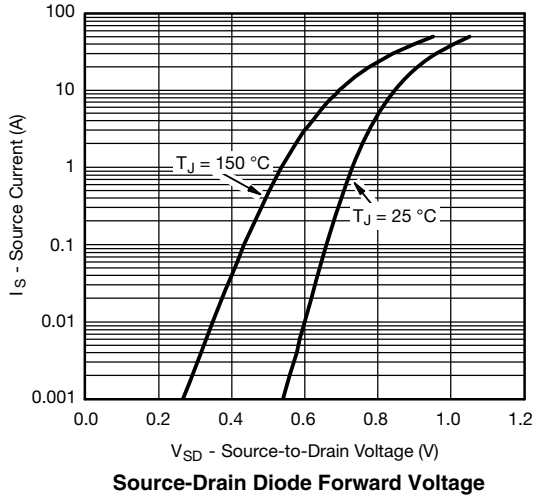
On-Resistance vs. Junction Temperature

Si7454CDP

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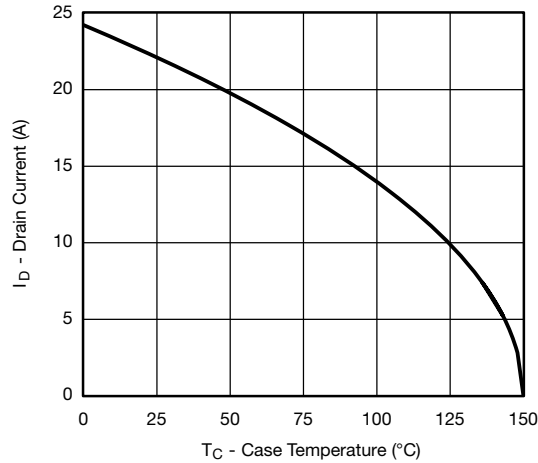


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

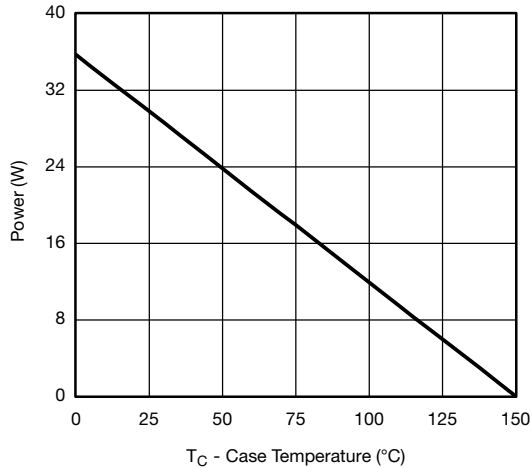




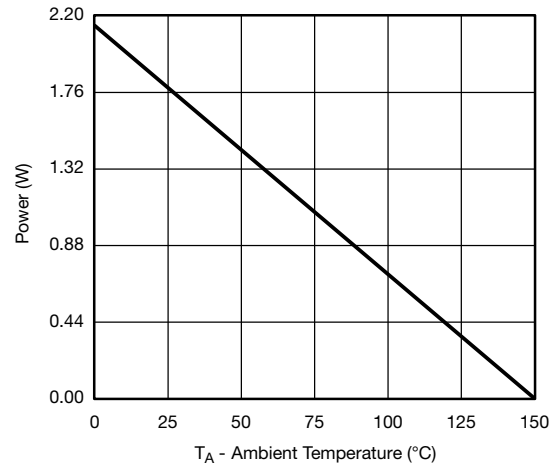
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

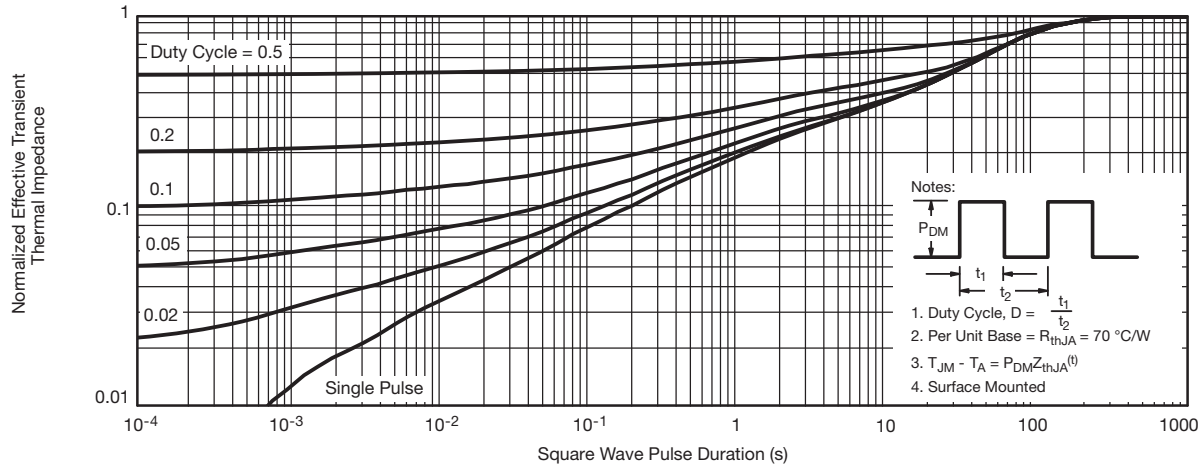
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si7454CDP

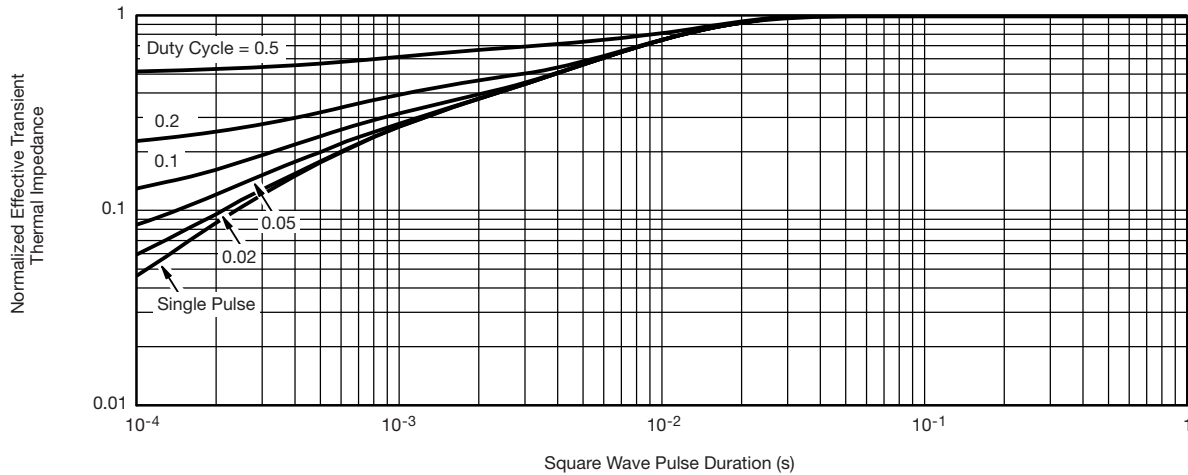
Vishay Siliconix



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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