## SQM40016EM

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AUTOMOTIVE

RoHS

COMPLIANT HALOGEN

FREE

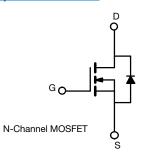
## Automotive N-Channel 40 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY					
V <sub>DS</sub> (V)	40				
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.00100				
I <sub>D</sub> (A)	250				
Configuration	Single				
Package	TO-263-7L				

#### FEATURES

- TrenchFET® power MOSFET
- · Package with low thermal resistance
- 100 %  $R_{\rm q}$  and UIS tested
- AEC-Q101 qualified
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



ABSOLUTE MAXIMUM RATING	<b>S</b> (T <sub>C</sub> = 25 °C, unless	s otherwise noted	)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	40	V
Gate-source voltage	V <sub>GS</sub>	± 20		
Continuous drain current	T <sub>C</sub> = 25 °C <sup>a</sup>	I	250	
	T <sub>C</sub> = 125 °C	l <sub>D</sub>	229	
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	250	А
Pulsed drain current <sup>b</sup>	I <sub>DM</sub>	420		
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	78	
Single pulse avalanche energy		E <sub>AS</sub>	304	mJ
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	PD	300	W
	T <sub>C</sub> = 125 °C	۳D	100	vv
Operating junction and storage temperature	range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	40	°C/W		
Junction-to-case (drain)		R <sub>thJC</sub>	0.5	0/10		

#### Notes

a. Package limited

b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

c. When mounted on 1" square PCB (FR4 material)

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static					•	•		
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$		40	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μΑ	2.5	3.0	3.5	v	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA	
		$V_{GS} = 0 V \qquad \qquad V_{DS} = 40 V$		-	-	1		
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	500	μA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	100	-	-	Α	
		$V_{GS} = 10 V$	I <sub>D</sub> = 40 A	-	0.00081	0.00100		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	I <sub>D</sub> = 40 A, T <sub>J</sub> = 125 °C	-	-	0.00152	Ω	
		$V_{GS} = 10 V$	I <sub>D</sub> = 40 A, T <sub>J</sub> = 175 °C	-	-	0.00184		
Forward transconductance b	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 40 A		-	181	-	S	
Dynamic <sup>b</sup>					-			
Input capacitance	C <sub>iss</sub>			-	10 841	15 000		
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$ $V_{DS} = 25 V$ , f = 1 MHz		-	2928	4000	pF	
Reverse transfer capacitance	C <sub>rss</sub>	-		-	198	270		
Total gate charge <sup>c</sup>	Qg			-	163	245		
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 \text{ V}$ $V_{DS} = 20 \text{ V}, I_D = 100 \text{ A}$		-	46	-	nC	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	36	-		
Gate resistance	Rg	f = 1 MHz		1	2.2	3.4	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	24	40		
Rise time <sup>c</sup>	tr	$\label{eq:VDD} \begin{array}{l} V_{\text{DD}} = 20 \text{ V}, \ R_{\text{L}} = 0.2 \ \Omega \\ I_{\text{D}} \cong 100 \ \text{A}, \ V_{\text{GEN}} = 10 \ \text{V}, \ R_{\text{g}} = 1 \ \Omega \end{array}$		-	215	330	20	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	59	90	ns	
Fall time <sup>c</sup>	t <sub>f</sub>			-	35	55		
Source-Drain Diode Ratings and Chara	cteristics <sup>b</sup>	<u>.</u>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	420	А	
Forward voltage	V <sub>SD</sub>	$I_F = 60 \text{ A}, V_{GS} = 0 \text{ V}$		-	0.8	1.5	V	
Body diode reverse recovery time	t <sub>rr</sub>			-	92	185	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	I <sub>F</sub> = 40 A, di/dt = 100 A/μs		-	198	400	nC	
Reverse recovery fall time	t <sub>a</sub>			-	47	-	-	
Reverse recovery rise time	t <sub>b</sub>			-	45	-	ns	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-4.4	-	А	

#### Notes

a. Pulse test; pulse width  $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%$ 

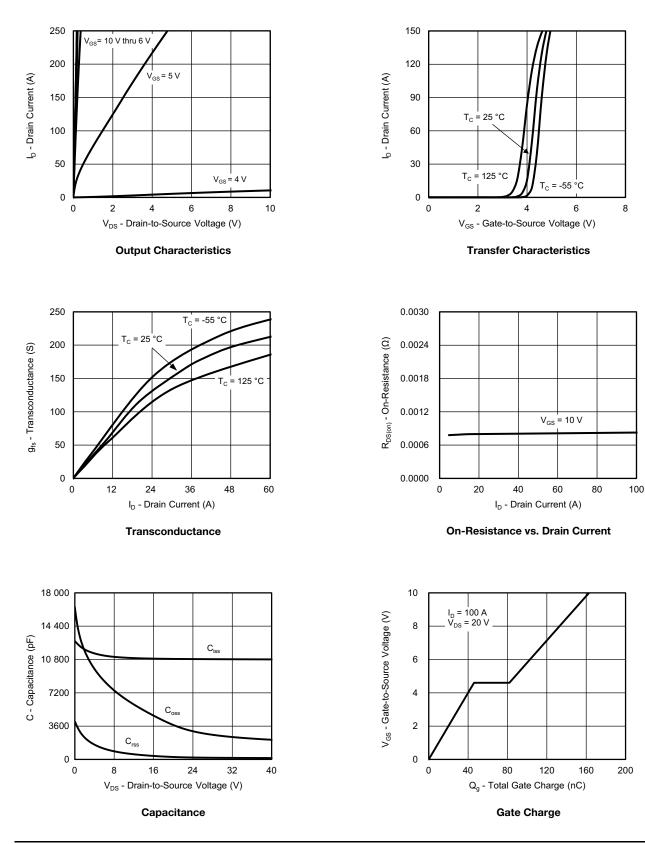
b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



S17-1886-Rev. A, 01-Jan-18

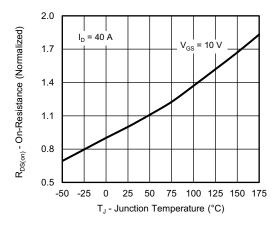
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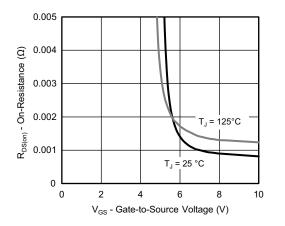
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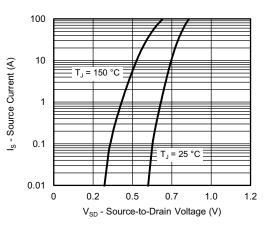
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



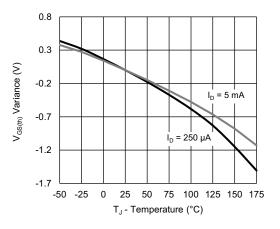
**On-Resistance vs. Junction Temperature** 



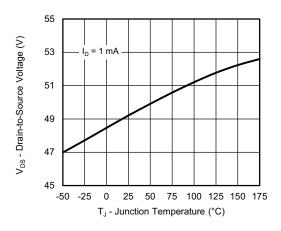
On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage







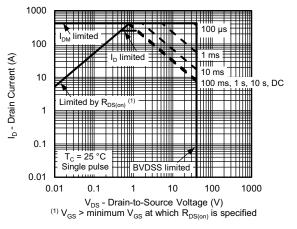
Drain Source Breakdown vs. Junction Temperature

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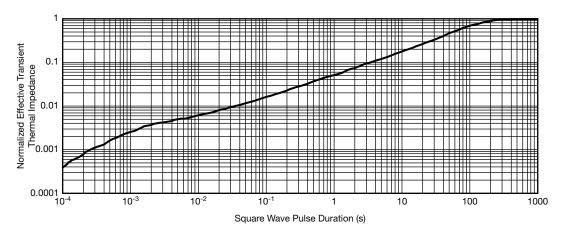
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### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



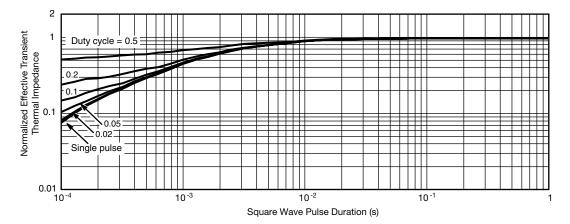
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

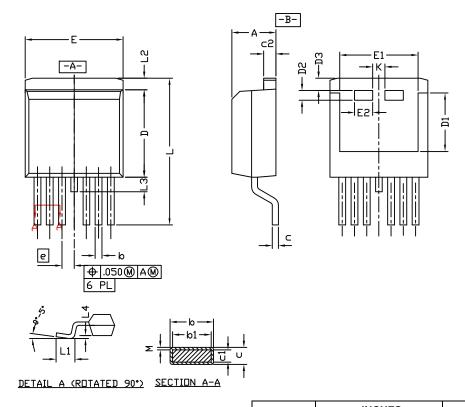
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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## D<sup>2</sup>PAK (TO-263-7L) Case Outline



#### Notes

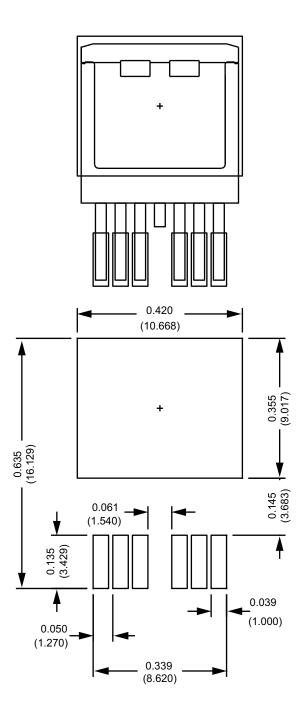
- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin to pin coplanarity max. 4 mils.
- 4. Lead thickness 25 mils.
- 5. For SUM part numbers lead thickness is 24 mils to 29 mils.
- 6. For reference only.
- 7. Use inches as the primary measurement.
- 8. This feature is only for SUM.

	INC	HES	MILLIMETERS		
DIM.	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c* SUB	0.012	0.018	0.305	0.457	
c* SUM	0.022	0.028	0.559	0.711	
c1	0.018	0.025	0.457	0.635	
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.072	0.078	1.829	1.981	
е	0.050 BSC		1.27 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
М	-	0.002	-	0.050	
ECN: T13-0709-Rev. B, 30-Sep-13 DWG: 6006					





# Recommended Land Pattern D<sup>2</sup>PAK (TO-263-7L)





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