



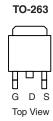
# N-Channel 60-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>(BR)DSS</sub> (V)	$r_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)	
60	$0.0039 \text{ at V}_{GS} = 10 \text{ V}$	110 <sup>a</sup>	200	

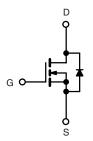
#### **FEATURES**

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- High Threshold Voltage At High Temperature
- 100 % R<sub>g</sub> Tested





Ordering Information: SUM110N06-3m9H-E3 (Lead (Pb)-free)



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25$ °C, unless otherwise noted					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	60	V		
Gate-Source Voltage	V <sub>GS</sub>	± 20	V		
0 D . 0 (T 175.00)	T <sub>C</sub> = 25 °C	I-	110 <sup>a</sup>	Α	
Continuous Drain Current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 125 °C	- I <sub>D</sub>	110 <sup>a</sup>		
Pulsed Drain Current	I <sub>DM</sub>	440			
Single Pulse Avalanche Current	I <sub>AS</sub>	70	]		
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	245	mJ	
Maximum Power Dissipation <sup>b</sup>	$T_C = 25  ^{\circ}C$	В	375 <sup>c</sup>	W	
	T <sub>A</sub> = 25 °C <sup>d</sup>	- P <sub>D</sub>	3.75		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Limit	Unit	
Junction-to-Ambient	PCB Mount <sup>d</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.4	- C/VV	

#### Notes:

- a. Package limited.
- b. Duty cycle  $\leq$  1 %.
- c. See SOA curve for voltage derating.
- d. When mounted on 1" square PCB (FR-4 material).

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<b>SPECIFICATIONS</b> $T_J = 25$	°C, unless o	otherwise noted					
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V, } I_D = 250  \mu\text{A}$	60			V	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.4		4.5		
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			100	nA	
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	μΑ	
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		0.00325	0.0039	Ω	
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C			0.0063		
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C			0.0082		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	30			S	
Dynamic <sup>b</sup>	•			•			
Input Capacitance	C <sub>iss</sub>			15 800		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		1050			
Reverse Transfer Capacitance	C <sub>rss</sub>			600			
Gate Resistance	$R_{g}$	f = 1 MHz	0.6	1.2	1.8	Ω	
Total Gate Charge <sup>c</sup>	Qg			200	300	nC	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 110 A		80			
Gate-Drain Charge <sup>c</sup>	$Q_{\mathrm{gd}}$			45			
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			45	70	ns	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_{L} = 0.27 \Omega$		160	240		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 110 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		75	115		
Fall Time <sup>c</sup>	t <sub>f</sub>			14	25		
Source-Drain Diode Ratings and Cha	aracteristics	(T <sub>C</sub> = 25 °C) <sup>b</sup>		I	l l		
Continuous Current	I <sub>S</sub>				110	Α	
Pulsed Current	I <sub>SM</sub>				240		
Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>F</sub> = 85 A, V <sub>GS</sub> = 0 V		1.1	1.5	٧	
Reverse Recovery Time	t <sub>rr</sub>			65	100	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 85 A, di/dt = 100 A/μs		4.4	6.6	Α	
Reverse Recovery Charge	Q <sub>rr</sub>			143	330	nC	

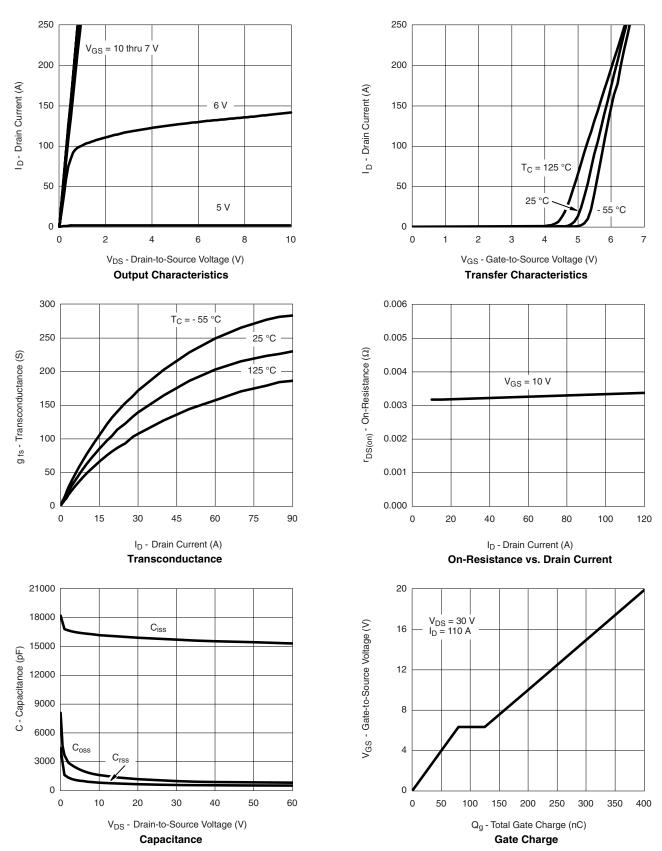
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

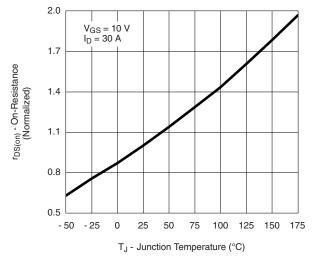


Document Number: 73236 S-70534-Rev. C, 26-Mar-07

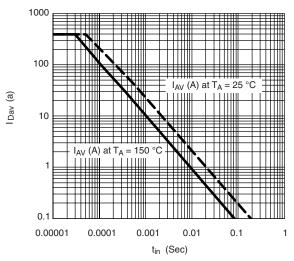
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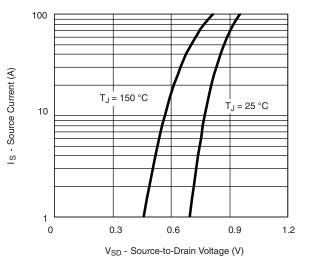
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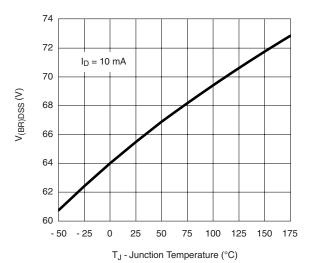
On-Resistance vs. Junction Temperature



**Avalanche Current vs. Time** 



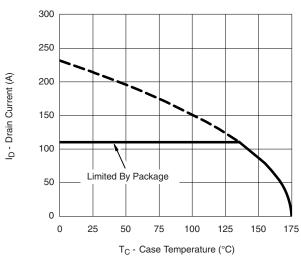
Source-Drain Diode Forward Voltage

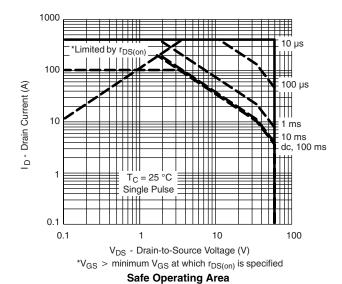


Drain Source Breakdown vs. Junction Temperature

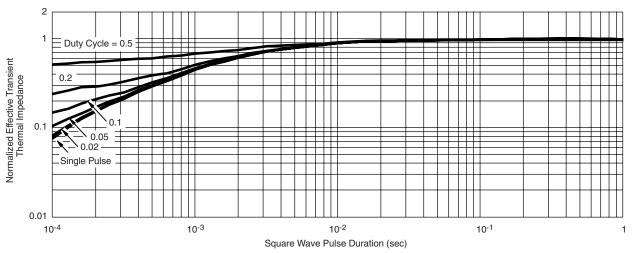


#### THERMAL RATINGS





Maximum Avalanche and Drain Current vs. Case Temperature



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?73236">http://www.vishay.com/ppg?73236</a>.

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Document Number: 91000
Revision: 18-Jul-08
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