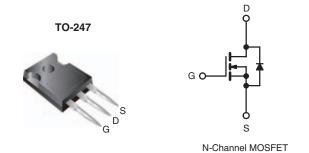


Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	50	500		
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	V _{GS} = 10 V 0.40		
Q _g (Max.) (nC)	150	150		
Q _{gs} (nC)	20	20		
Q _{gd} (nC)	80	80		
Configuration	Sing	Single		



FEATURES

- · Dynamic dV/dt Rating
- · Repetitive Avalanche Rated
- · Isolated Central Mounting Hole
- Fast Switching
- · Ease of Paralleling
- · Simple Drive Requirements
- Lead (Pb)-free Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION		
Package	TO-247	
Lead (Pb)-free	IRFP450PbF	
Leau (FD)-liee	SiHFP450-E3	
SnPb	IRFP450	
SIFD	SiHFP450	

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 20	v
Continuous Drain Current	V _{GS} at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	1-	14	
Continuous Diain Current	V _{GS} at 10 V	T _C = 100 °C	ID	8.7	Α
Pulsed Drain Current ^a			I _{DM}	56	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	760	mJ
Repetitive Avalanche Current ^a			I _{AR}	8.7	Α
Repetitive Avalanche Energy ^a			E _{AR}	19	mJ
Maximum Power Dissipation	T _C =	25 °C	P_{D}	190	W
Peak Diode Recovery dV/dtc			dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) for 10 s			300 ^d		
Mounting Torque	6.22.04.1	0.00 140		10	lbf ⋅ in
Mounting Torque	6-32 or M3 screw			1.1	N · m

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 7.0 mH, R_G = 25 Ω , I_{AS} = 14 A (see fig. 12).
- c. $I_{SD} \leq$ 14 A, $dI/dt \leq$ 130 A/µs, $V_{DD} \leq V_{DS}, \, T_{J} \leq$ 150 °C.
- d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	40	
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24	-	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.65	

SPECIFICATIONS $T_J = 25 ^{\circ}C$,	unless otherv	vise noted					
PARAMETER	SYMBOL	TEST	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						•	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0	V, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	to 25 °C, I _D = 1 mA	-	0.63	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	_{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _G	_S = ± 20 V	-	-	± 100	nA
Zana Oata Wallana Busin Oamani		V _{DS} = 50	00 V, V _{GS} = 0 V	-	-	25	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 V, V	/ _{GS} = 0 V, T _J = 125 °C	-	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 8.4 A ^b	-	-	0.40	Ω
Forward Transconductance	9 _{fs}	V _{DS} = 5	0 V, I _D = 8.4 A ^b	9.3	-	-	S
Dynamic				l e			
Input Capacitance	C _{iss}	\ <u>\</u>	_{GS} = 0 V,	-	2600	-	
Output Capacitance	C _{oss}	Vr	$_{0S} = 25 \text{ V},$	-	720	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	340	-	1
Total Gate Charge	Qg			-	-	150	
Gate-Source Charge	Q_{gs}	V _{GS} = 10 V	$I_D = 14 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13^b	-	-	20	nC
Gate-Drain Charge	Q _{gd}		See fig. 6 and 16	-	-	80	
Turn-On Delay Time	t _{d(on)}			-	17	-	
Rise Time	t _r	V 2	50 V, I _D = 14 A,	-	47	-	
Turn-Off Delay Time	t _{d(off)}	$R_{G} = 6.2 \Omega$, $R_{D} = 17 \Omega$, see fig. 10^{b}		-	92	-	ns
Fall Time	t _f			-	44	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") fro	m ,	-	5.0	-	
Internal Source Inductance	L _S	package and cer die contact	nter of	-	13	-	- nH
Drain-Source Body Diode Characteristic	s			l e			
Continuous Source-Drain Diode Current	I _S	MOSFET symbo	ol Control	-	-	14	
Pulsed Diode Forward Current ^a	I _{SM}	integral reverse p - n junction diode		-	-	56	A
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S	_S = 14 A, V _{GS} = 0 V ^b	-	-	1.4	V
Body Diode Reverse Recovery Time	t _{rr}	T 05 00 1	44.4 dl/dt 400.44 - b	-	540	810	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 14 \text{A}, dI/dt = 100 \text{A}/\mu\text{s}^b$		-	4.8	7.2	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)			 L _D)		

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

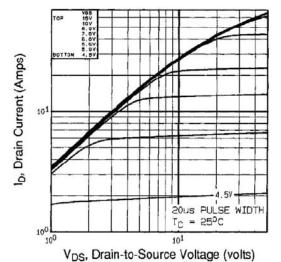


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

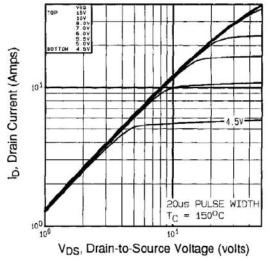


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

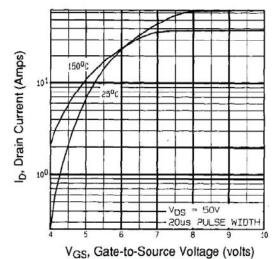


Fig. 3 - Typical Transfer Characteristics

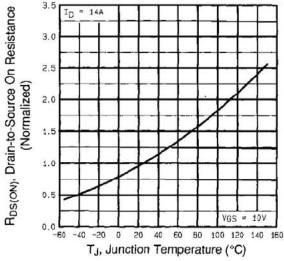


Fig. 4 - Normalized On-Resistance vs. Temperature



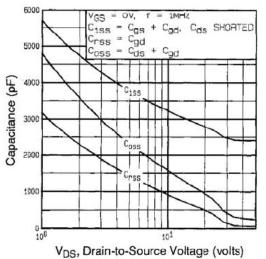


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

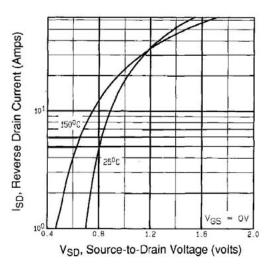


Fig. 7 - Typical Source-Drain Diode Forward Voltage

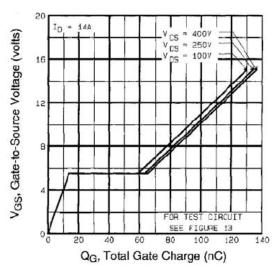


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

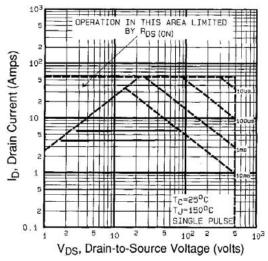


Fig. 8 - Maximum Safe Operating Area

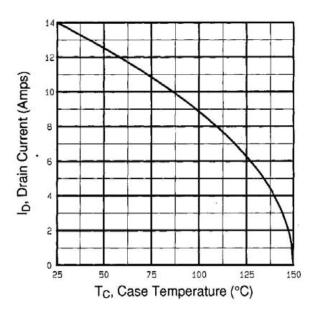


Fig. 9 - Maximum Drain Current vs. Case Temperature

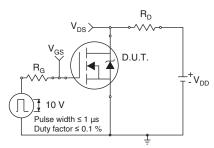


Fig. 10a - Switching Time Test Circuit

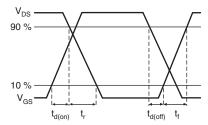


Fig. 10b - Switching Time Waveforms

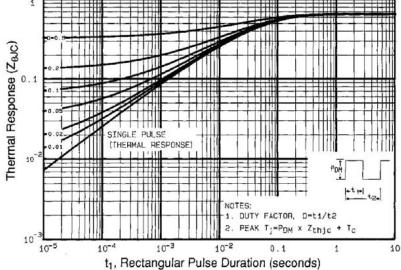


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

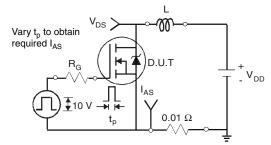


Fig. 12a - Unclamped Inductive Test Circuit

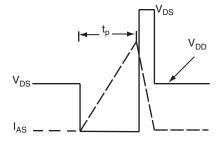


Fig. 12b - Unclamped Inductive Waveforms



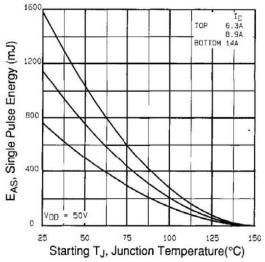


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

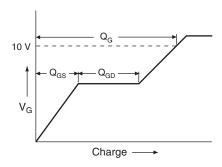


Fig. 13a - Basic Gate Charge Waveform

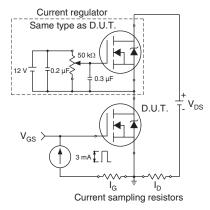
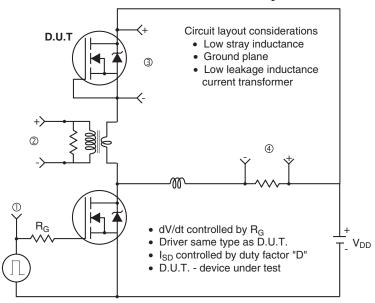
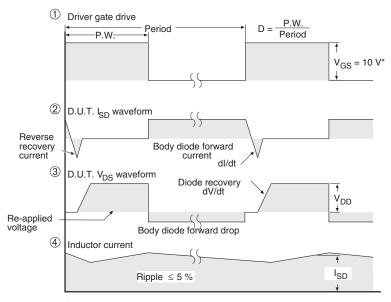


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

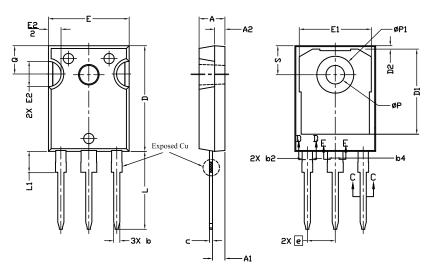
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Document Number: 91233 S-81271-Rev. A, 16-Jun-08

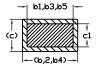


TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D--D,E--E

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
Α	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

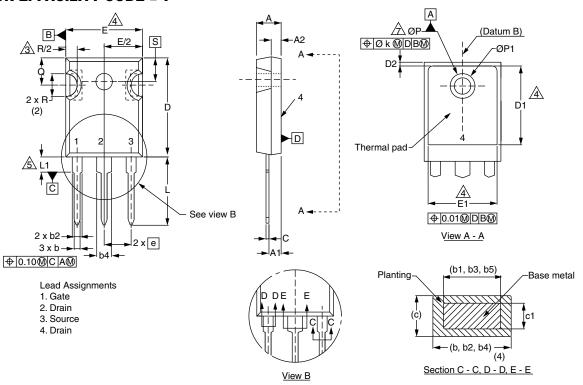
	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØΡ	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	
L		I	1

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

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VERSION 2: FACILITY CODE = Y



	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

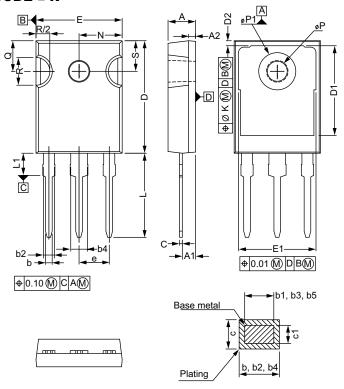
	MILLIN		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	0.254	
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

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VERSION 3: FACILITY CODE = N



	MILLIMETERS		
DIM.	MIN.	MAX.	
Α	4.65	5.31	
A1	2.21	2.59	
A2	1.17	1.37	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.65	2.39	
b3	1.65	2.34	
b4	2.59	3.43	
b5	2.59	3.38	
С	0.38	0.89	
c1	0.38	0.84	
D	19.71	20.70	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	
D2	0.51	1.35	
E	15.29	15.87	
E1	13.46	-	
е	5.46	BSC	
k	0.254		
L	14.20	16.10	
L1	3.71	4.29	
N	7.62 BSC		
Р	3.56	3.66	
P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51	BSC	

ECN: E20-0545-Rev. F, 19-Oct-2020

DWG: 5971

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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