# High-Bandwidth, Low Voltage, Dual SPDT Analog Switches

## DESCRIPTION

The DG2016/DG2026 are monolithic CMOS dual single-pole/double-throw (SPDT) analog switchs. They are specifically designed for low-voltage, high bandwidth applications.

The DG2016/DG2026's on-resistance (3 Ω at 2.7 V), matching and flatness are guaranteed over the entire analog voltage range. Wide dynamic performance is achieved with better than - 80 dB for both cross-talk and off-isolation at 1 MHz.

Both SPDT's operate with independent control logic, conduct equally well in both directions and block signals up to the power supply level when off. Break-before-make is guaranteed.

With fast switching speeds, low on-resistance, high bandwidth, and low charge injection, the DG2016/DG2026 are ideally suited for audio and video switching with high linearity.

Built on Vishay Siliconix's low voltage CMOS technology, the DG2016/DG2026 contain an epitaxial layer which prevents latch-up

## FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Single Supply (1.8 V to 5.5 V)
- Low On-Resistance - $R_{ON}$: 2.4 Ω
- Crosstalk and Off Isolation: - 81 dB at 1 MHz
- MSOP-10 Package
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT
HALOGEN FREE

## BENEFITS

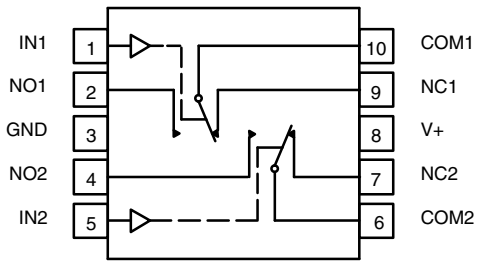
- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- Low-Voltage Logic Compatible
- High Bandwidth

## APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Low-Voltage Data Acquisition
- ATE

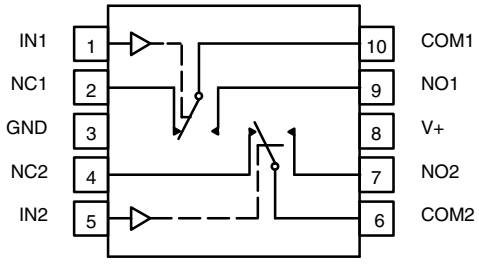
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG2016DQ – MSOP-10**




Top View

**DG2026DQ – MSOP-10**




Top View

| TRUTH TABLE | | |
|---|---|---|
| **Logic** | **NC1 and NC2** | **NO1 and NO2** |
| 0 | ON | OFF |
| 1 | OFF | ON |

| ORDERING INFORMATION | | |
|---|---|---|
| **Temp Range** | **Package** | **Part Number** |
| - 40 °C to 85 °C | MSOP-10 | DG2016DQ-T1-E3 |
| | | DG2026DQ-T1-E3 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Limit | Unit |
|---|---|---|---|
| Reference V+ to GND | | - 0.3 to + 6 | V |
| IN, COM, NC, NO[a] | | - 0.3 to (V+ + 0.3) | |
| Continuous Current (Any terminal) | | ± 50 | mA |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | | ± 200 | |
| Storage Temperature (D Suffix) | | - 65 to 150 | °C |
| Power Dissipation (Packages)[b] | MSOP-10[c] | 320 | mW |

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 4 mW/°C above 70 °C.

## SPECIFICATIONS (V+ = 3 V)

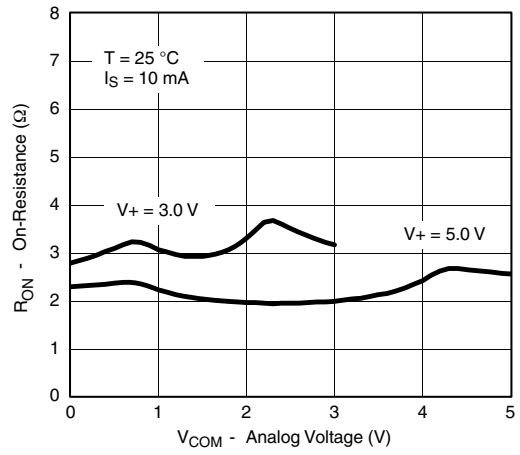
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, $V_{IN}$ = 0.4 V or 2 V[e] | Temp.[a] | Limits - 40 °C to 85 °C Min.[b] | Typ.[c] | Max.[b] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$ $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 2.7 V, $V_{COM}$ = 0.2 V/1.5 V, $I_{NO}$, $I_{NC}$ = 10 mA | Room<br>Full | | 3 | 4.8<br>5.3 | Ω |
| $R_{ON}$ Flatness | $R_{ON}$ Flatness | V+ = 2.7 V, $V_{COM}$ = 0 to V+, $I_{NO}$, $I_{NC}$ = 10 mA | Room | | | 1.6 | |
| Switch Off Leakage Current[f] | $I_{NO(off)}$ $I_{NC(off)}$ | V+ = 3.3 V<br>$V_{NO}$, $V_{NC}$ = 0.3 V/3 V, $V_{COM}$ = 3 V/0.3 V | Room<br>Full | - 1<br>- 10 | | 1<br>10 | nA |
| | $I_{COM(off)}$ | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| Channel-On Leakage Current[f] | $I_{COM(on)}$ | V+ = 3.3 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 0.3 V/3 V | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| **Digital Control** | | | | | | | |
| Input High Voltage[d] | $V_{INH}$ | | Full | 1.6 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.4 | |
| Input Capacitance | $C_{in}$ | | Full | | 5 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 V or V+ | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 2 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room<br>Full | | 28 | 53<br>59 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | | 13 | 38<br>38 | |
| Break-Before-Make Time | $t_d$ | | Full | 1 | | | |
| Charge Injection[d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω | Room | | 38 | | pC |
| Off-Isolation[d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | | - 78 | | dB |
| Crosstalk[d] | $X_{TALK}$ | | Room | | - 82 | | |
| $N_O$, $N_C$ Off Capacitance[d] | $C_{NO(off)}$ | $V_{IN}$ = 0 V or V+, f = 1 MHz | Room | | 15 | | pF |
| | $C_{NC(off)}$ | | Room | | 15 | | |
| Channel-On Capacitance[d] | $C_{NO(on)}$ | | Room | | 49 | | |
| | $C_{NC(on)}$ | | Room | | 45 | | |
| **Power Supply** | | | | | | | |
| Power Supply Current | I+ | $V_{IN}$ = 0 V or V+ | Full | | 0.01 | 1 | µA |

| **SPECIFICATIONS** (V+ = 5 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions Otherwise Unless Specified** V+ = 5 V, ± 10 %, $V_{IN}$ = 0.8 V or 2.4 V[e] | **Temp.[a]** | **Limits - 40 °C to 85 °C** Min.[b] | Typ.[c] | Max.[b] | **Unit** |
| **Analog Switch** | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$ $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 4.5 V, $V_{COM}$ = 3 V, $I_{NO}$, $I_{NC}$ = 10 mA | Room<br>Full | | 2.4 | 4<br>4.3 | Ω |
| $R_{ON}$ Flatness | $R_{ON}$ Flatness | V+ = 4.5 V, $V_{COM}$ = 0 to V+, $I_{NO}$, $I_{NC}$ = 10 mA | Room | | | 1.2 | |
| Switch Off Leakage Current | $I_{NO(off)}$ $I_{NC(off)}$ | V+ = 5.5 V<br>$V_{NO}$, $V_{NC}$ = 1 V/4.5 V, $V_{COM}$ = 4.5 V/1 V | Room<br>Full | - 1<br>- 10 | | 1<br>10 | nA |
| | $I_{COM(off)}$ | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| Channel-On Leakage Current | $I_{COM(on)}$ | V+ = 5.5 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ =1 V/4.5 V | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| **Digital Control** | | | | | | | |
| Input High Voltage[d] | $V_{INH}$ | | Full | 2 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.8 | |
| Input Capacitance | $C_{in}$ | | Full | | 5 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 V or V+ | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 3 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room<br>Full | | 23 | 48<br>52 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | | 8 | 33<br>35 | |
| Break-Before-Make Time | $t_d$ | | Full | 1 | | | |
| Charge Injection[d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω | Room | | 79 | | pC |
| Off-Isolation[d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | | - 81 | | dB |
| Crosstalk[d] | $X_{TALK}$ | | Room | | - 82 | | |
| Source-Off Capacitance[d] | $C_{NO(off)}$ | $V_{IN}$ = 0 V or V+, f = 1 MHz | Room | | 14 | | pF |
| | $C_{NC(off)}$ | | Room | | 14 | | |
| Channel-On Capacitance[d] | $C_{NO(on)}$ | | Room | | 48 | | |
| | $C_{NC(on}$ | | Room | | 44 | | |
| **Power Supply** | | | | | | | |
| Power Supply Range | V+ | | | 1.8 | | 5.5 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 V or V+ | Full | | 0.01 | 1 | µA |

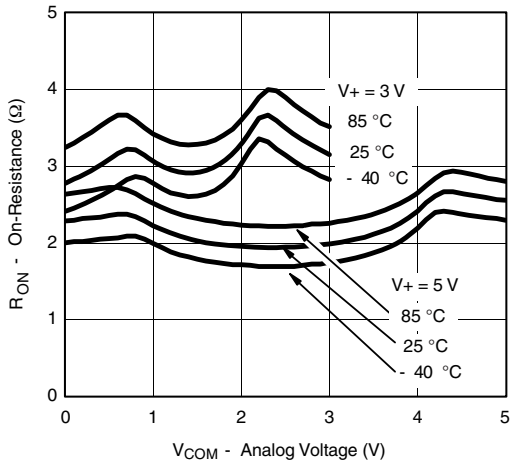
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. $V_{IN}$ = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

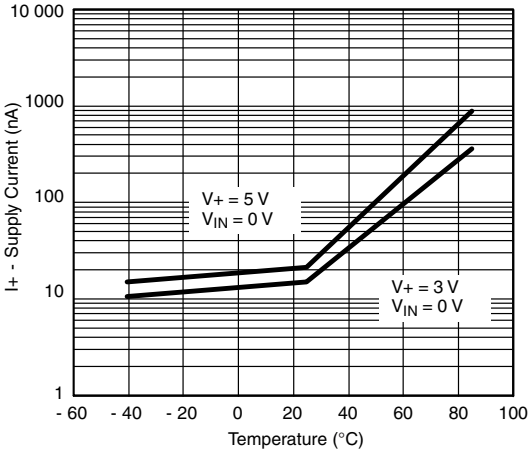
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



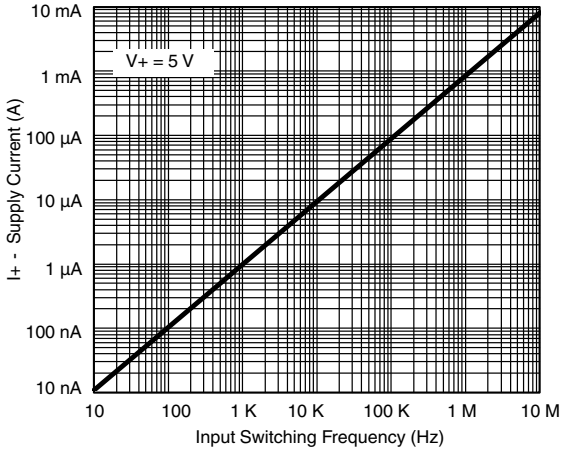

**$R_{ON}$ vs. $V_{COM}$ and Supply Voltage**



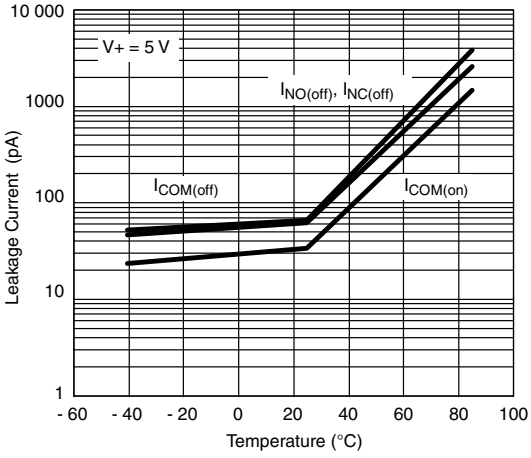

**$R_{ON}$ vs. Analog Voltage and Temperature**



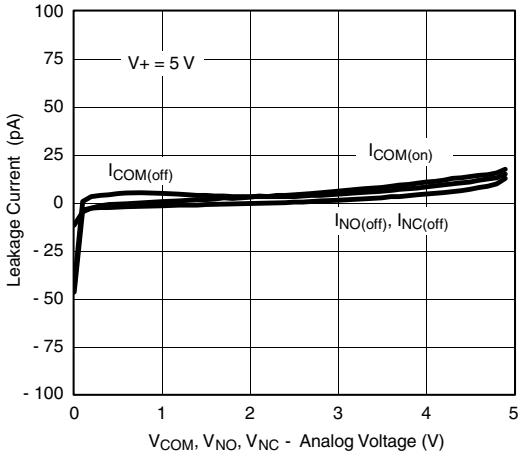

**Supply Current vs. Temperature**




**Supply Current vs. Input Switching Frequency**

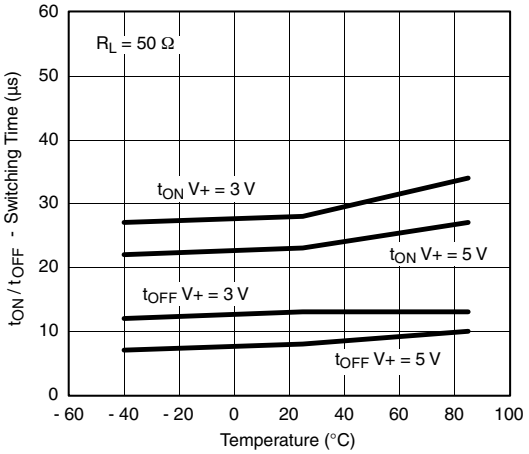



**Leakage Current vs. Temperature**

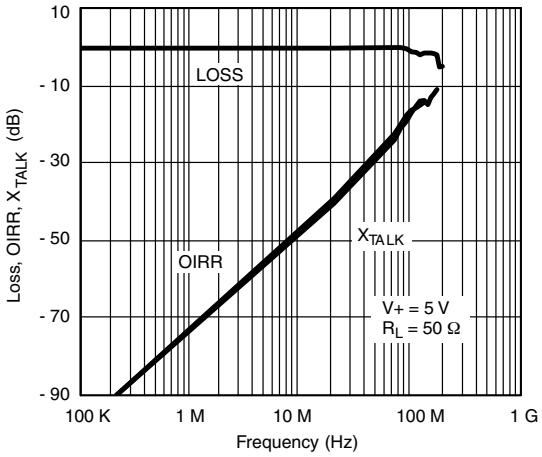



**Leakage vs. Analog Voltage**

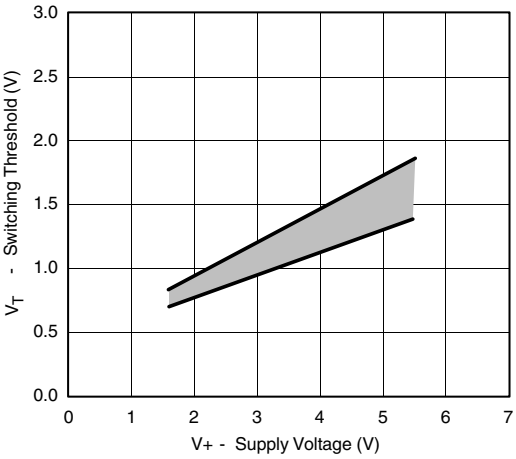
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



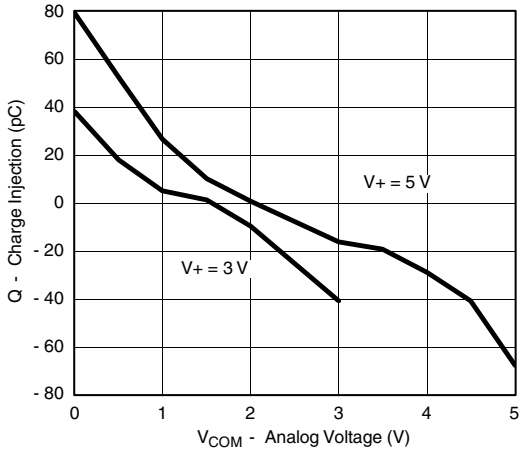

**Switching Time vs. Temperature**




**Insertion Loss, Off-Isolation Crosstalk vs. Frequency**

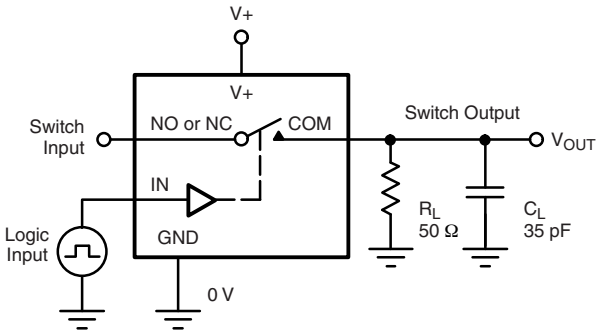



**Switching Threshold vs. Supply Voltage**



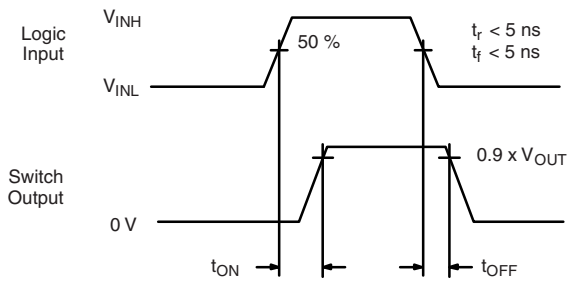

**Charge Injection vs. Analog Voltage**

## TEST CIRCUITS




$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

**Figure 1. Switching Time**

## TEST CIRCUITS

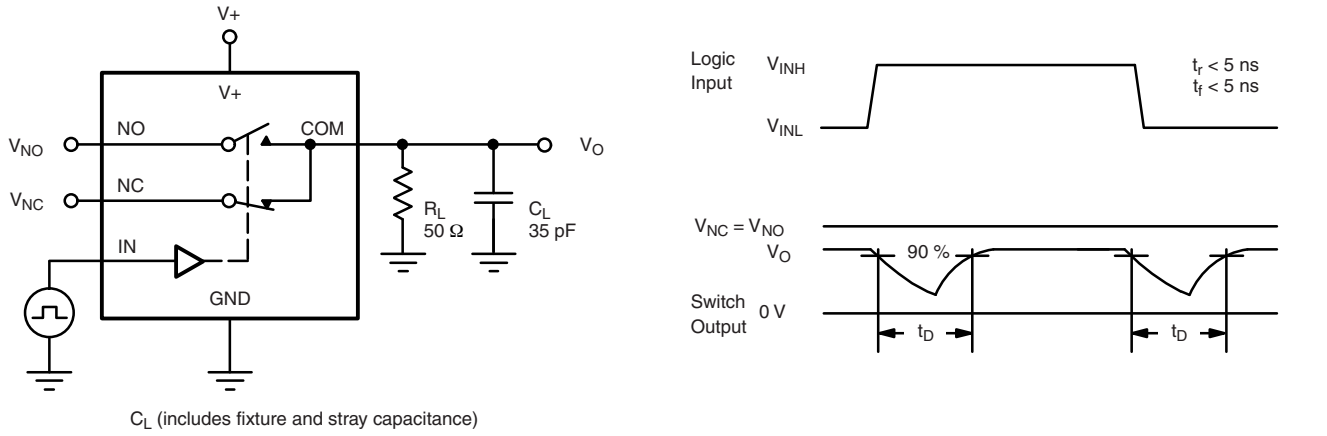



**Figure 2. Break-Before-Make Interval**

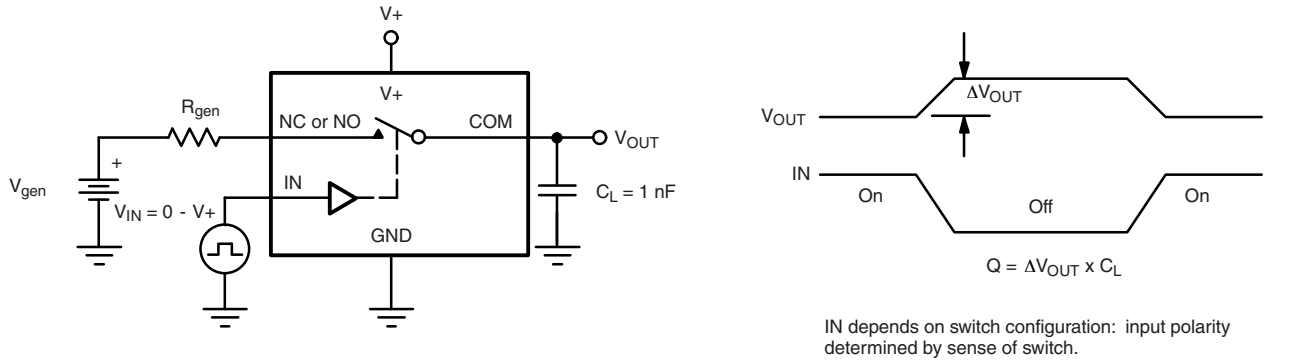



**Figure 3. Charge Injection**

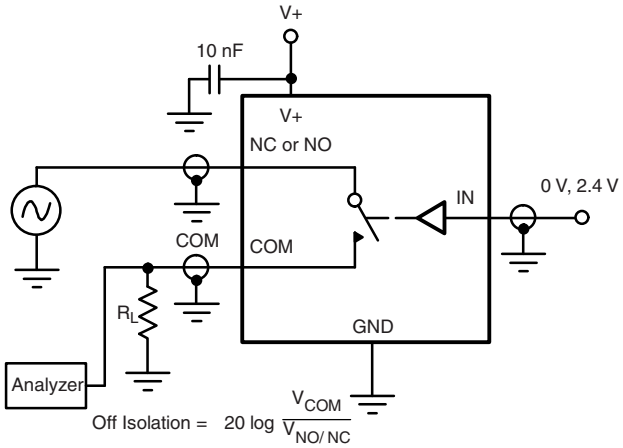



**Figure 4. Off-Isolation**

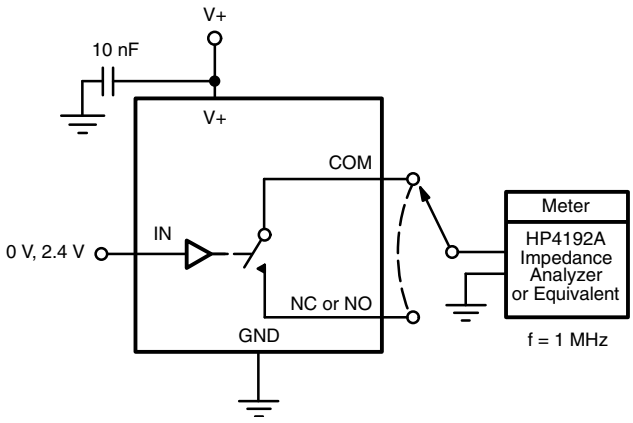
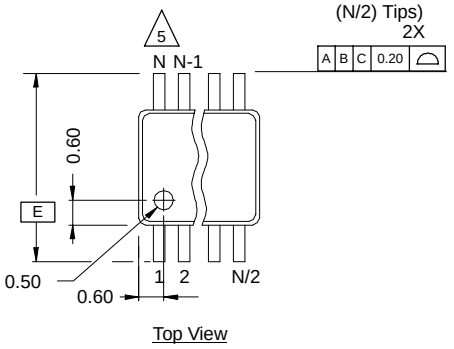



**Figure 5. Channel Off/On Capacitance**

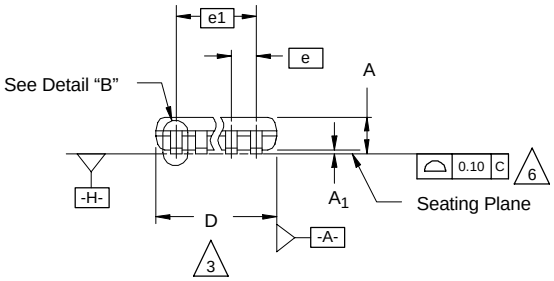
*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72030.*

## MSOP: 10-LEADS

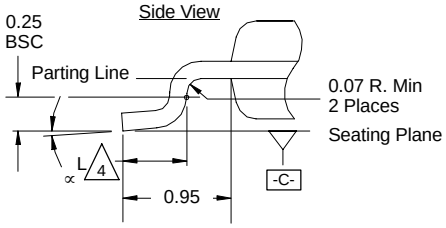
**JEDEC Part Number: MO-187, (Variation AA and BA)**



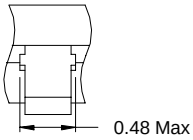

Top View



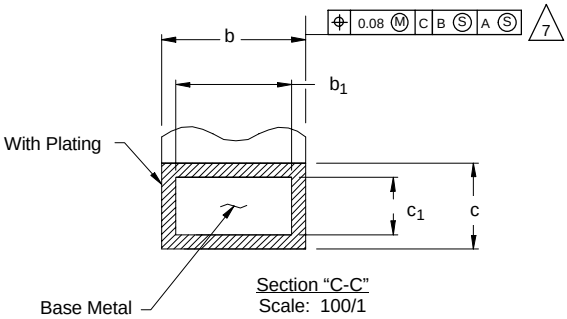

Side View



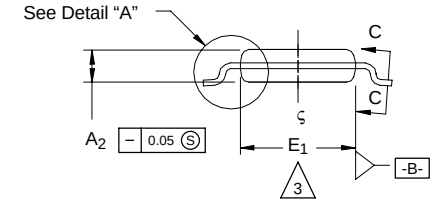

Detail "A"
(Scale: 30/1)




Detail "B"
(Scale: 30/1)
Dambar Protrusion




Section "C-C"
Scale: 100/1
(See Note 8)




End View

NOTES:

1. Die thickness allowable is $0.203 \pm 0.0127$.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "$E_1$" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

**N = 10L**

| Dim | MILLIMETERS | | | Note |
|---|---|---|---|---|
| | Min | Nom | Max | |
| A | - | - | 1.10 | |
| $A_1$ | 0.05 | 0.10 | 0.15 | |
| $A_2$ | 0.75 | 0.85 | 0.95 | |
| b | 0.17 | - | 0.27 | 8 |
| $b_1$ | 0.17 | 0.20 | 0.23 | 8 |
| c | 0.13 | - | 0.23 | |
| $c_1$ | 0.13 | 0.15 | 0.18 | |
| D | 3.00 BSC | | | 3 |
| E | 4.90 BSC | | | |
| $E_1$ | 2.90 | 3.00 | 3.10 | 3 |
| e | 0.50 BSC | | | |
| $e_1$ | 2.00 BSC | | | |
| L | 0.40 | 0.55 | 0.70 | 4 |
| N | 10 | | | 5 |
| ∝ | 0° | 4° | 6° | |

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DWG: 5867

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