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Vishay Siliconix

Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFETs

PRODUCT SUMMARY							
	N-CHANNEL 1 N-CHANNE						
V _{DS} (V)	40	40					
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0160	0.0064					
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0188	0.0076					
I _D (A)	15	18					
Configuration	Dual N						

FEATURES

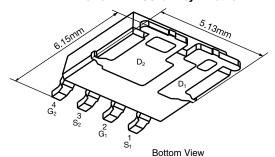
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_a and UIS Tested
- Material categorization:
 For definitions of compliance please see www.vishay.com/doc?99912

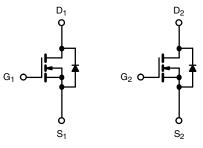




ROHS COMPLIANT HALOGEN FREE

PowerPAK® SO-8L Asymmetric





N-Channel 1 MOSFET

N-Channel 2 MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L Dual Asymmetric
Lead (Pb)-free and Halogen-free	SQJ940EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT			
Drain-Source Voltage		V _{DS}	40	40	V		
Gate-Source Voltage	V_{GS}	±	V				
Continuous Duoin Currents	T _C = 25 °C		15	18			
Continuous Drain Current ^a	T _C = 125 °C	l _D	15	10.5			
Continuous Source Current (Diode Conduction) ^a		I _S	15	39	Α		
Pulsed Drain Current ^b		I _{DM}	60	72	ı		
Single Pulse Avalanche Current	lingle Pulse Avalanche Current		20.5	35.5			
Single Pulse Avalanche Energy	gle Pulse Avalanche Energy		21	63	mJ		
Maximum Power Dissipation ^b	T _C = 25 °C	-	48	43	W		
Maximum Power Dissipation	T _C = 125 °C	P_{D}	16	14	VV		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175		°C		
Soldering Recommendations (Peak Temperature) ^{e, f}			260				

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	70	70	°C/W
Junction-to-Case (Drain)		R_{thJC}	3.3	3.5	C/ VV

Notes

- a. Package limited.
- b. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.
- e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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SPECIFICATIONS (T _C = 25	1	otnerwise no					,	1	
PARAMETER	SYMBOL		TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static						_			
Drain-Source Breakdown Voltage	V_{DS}	V _{GS} =	N-Ch 1	40	-	-			
Prain Coareo Broandown Vollage	• 05	V _{GS} =	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$			-	-	V	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	N-Ch 1	1.5	2	2.5	·		
date course imposible voltage	▼GS(tn)	V _{DS} =	N-Ch 2	1.5	2	2.5			
Gate-Source Leakage	I _{GSS}	V _{DS} =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	N-Ch 1	-	-	± 100	nA	
	.033	50		N-Ch 2	-	-	± 100		
		$V_{GS} = 0 V$	V _{DS} 40 V	N-Ch 1	1	-	1		
		$V_{GS} = 0 V$	V _{DS} = - 40 V	N-Ch 2	1	-	1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	$V_{DS} = 40 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$	N-Ch 1	-	-	50	μΑ	
Zero date voltage Brain odnem	טאטי	$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 125 °C	N-Ch 2	-	-	50	μΛ	
		$V_{GS} = 0 V$	$V_{DS} = 40 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$	N-Ch 1	-	-	150		
		$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 175 °C	N-Ch 2	ı	-	150		
On State Drain Currenta	1	V _{GS} = 10 V	$V_{DS} \ge 5 V$	N-Ch 1	30	-	-	Α	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 \text{ V}$	N-Ch 2	30	-			
		V _{GS} = 10 V	I _D = 15 A	N-Ch 1	-	0.0133	0.0160		
	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A	N-Ch 2	-	0.0053	0.0064	Ω	
		V _{GS} = 10 V	I _D = 15 A, T _J = 125 °C	N-Ch 1	-	-	0.0270		
5 : 6		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	N-Ch 2	1	-	0.0105		
Drain-Source On-State Resistance ^a		V _{GS} = 10 V	I _D = 15 A, T _J = 175 °C	N-Ch 1	-	-	0.0334		
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	N-Ch 2	-	-	0.0130		
		V _{GS} = 4.5 V	I _D = 13 A	N-Ch 1	-	0.0157	0.0188		
		V _{GS} = 4.5 V	I _D = 18 A	N-Ch 2	1	0.0063	0.0076	-	
- IT I b		V_{DS}	= 15 V, I _D = 15 A	N-Ch 1	1	64	-		
Forward Transconductance ^b	9 _{fs}	V _{DS}	= 15 V, I _D = 20 A	N-Ch 2	-	102	-	S	
Dynamic ^b	l					L			
		V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 1	-	717	896		
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 2	-	1850	2313		
	_	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 1	-	118	148	_	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 2	-	272	340	pF	
	_	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 1	-	48	60		
Reverse Transfer Capacitance	C _{rss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 2	-	98	123	1	
	Qg	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 6 A	N-Ch 1	-	13.5	20		
Total Gate Charge ^c		V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_D = 16 \text{ A}$	N-Ch 2	-	31.8	48		
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_D = 6 \text{ A}$	N-Ch 1	-	2.24	-	nC	
		V _{GS} = 10 V	V _{DS} = 20 V, I _D = 16 A	N-Ch 2	-	5.5	-	1	
	Q _{gd}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_D = 6 \text{ A}$	N-Ch 1	-	2.06	-	1	
Gate-Drain Charge ^c		$V_{GS} = 10 \text{ V}$ $V_{DS} = 20 \text{ V}, I_D = 16 \text{ A}$		N-Ch 2	-	4.7	-	1	
	istance R _g			N-Ch 1	1.2	2.52	5		
Gate Resistance			f = 1 MHz		3	7.93	13	Ω	
)	7.50	.0		

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



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SPECIFICATIONS (T _C		•			1	1		
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Turn-On Delay Time ^c	+	$\begin{aligned} V_{DD} &= 20 \text{ V}, \text{ R}_L = 20 \Omega \\ I_D &\cong \text{1 A}, \text{ V}_{GEN} = \text{10 V}, \text{ R}_g = \text{1 }\Omega \end{aligned}$	N-Ch 1	-	4.8	7.2		
	t _{d(on)}	$\begin{aligned} V_{DD} &= 20 \text{ V, } R_L = 20 \Omega \\ I_D &\cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega \end{aligned} \qquad \text{N-Ch 2}$		-	7.7	11.6		
Rise Time ^c		$\begin{aligned} V_{DD} &= 20 \text{ V}, \text{ R}_L = 20 \Omega\\ I_D &\cong \text{1 A}, \text{ V}_{GEN} = \text{10 V}, \text{ R}_g = \text{1 }\Omega \end{aligned}$	N-Ch 1	-	9.3	14		
	t _r -	$\begin{aligned} V_{DD} &= 20 \text{ V}, \text{ R}_L = 20 \Omega\\ I_D &\cong 1 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 2	- 9.5 14.3]		
Turn-Off Delay Time ^c		$\begin{aligned} V_{DD} &= 20 \text{ V}, \text{ R}_L = 20 \Omega\\ I_D &\cong 1 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 1	-	15.6	23.4	ns	
	t _{d(off)} -	V_{DD} = 20 V, R_L = 20 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 2	-	47	70		
Fall Times		$\begin{aligned} V_{DD} &= 20 \text{ V}, \text{ R}_L = 20 \Omega\\ I_D &\cong 1 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 1	-	4.9	7.4		
Fall Time ^c	t _f	V_{DD} = 20 V, R_L = 20 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 2	-	13.5	20.3		
Source-Drain Diode Ratings	and Characteristics	b						
Pulsed Current ^a			N-Ch 1	-		60	^	
	I _{SM}		N-Ch 2	-	-	72	A	
Forward Voltage	.,,	I _F = 8 A, V _{GS} = 0 V N-Ch 1		-	0.8	1.2	V	
	V _{SD}	$I_F = 17 \text{ A}, V_{GS} = 0 \text{ V}$ N-Ch 2 - 0			0.8	1.2	, v	

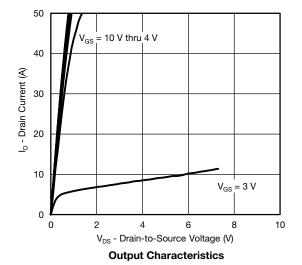
Notes

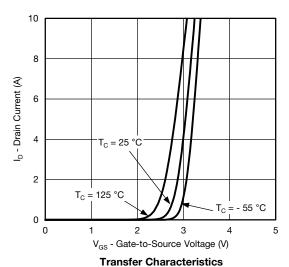
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

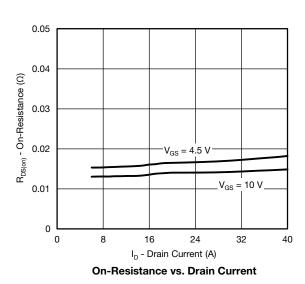
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

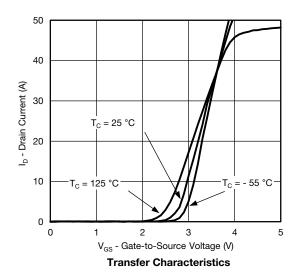


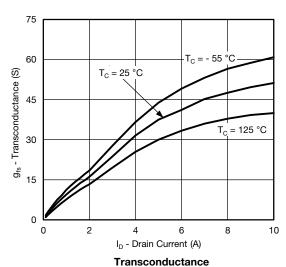
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

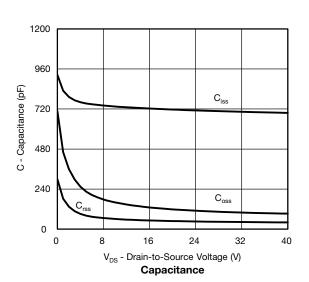






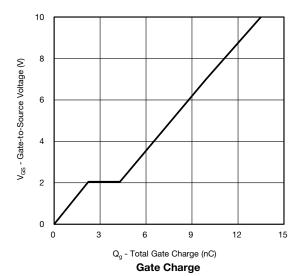


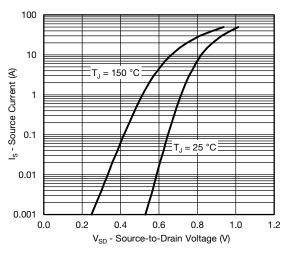




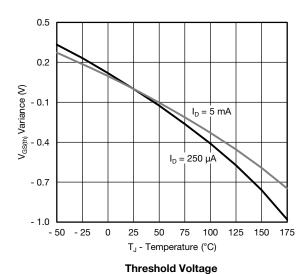


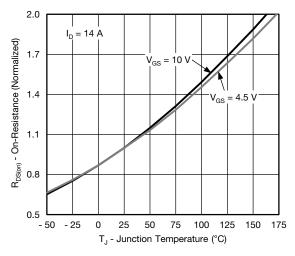
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



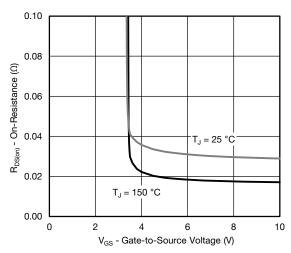


Source Drain Diode Forward Voltage

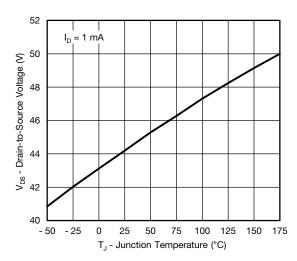




On-Resistance vs. Junction Temperature



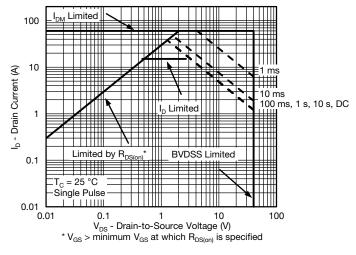
On-Resistance vs. Gate-to-Source Voltage



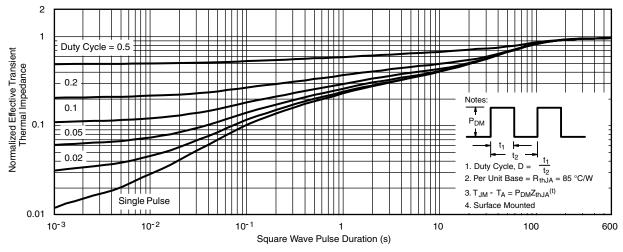
Drain Source Breakdown vs. Junction Temperature



N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



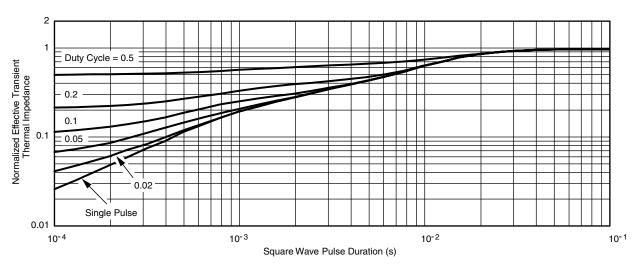
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



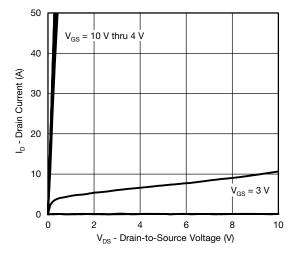
Normalized Thermal Transient Impedance, Junction-to-Case

Note

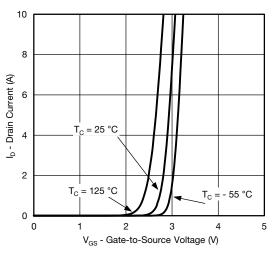
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



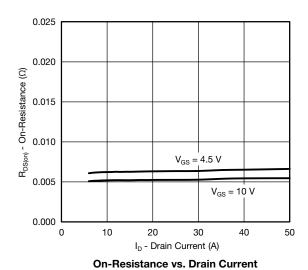
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



Output Characteristics

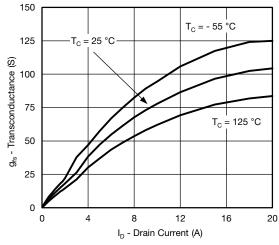


Transfer Characteristics

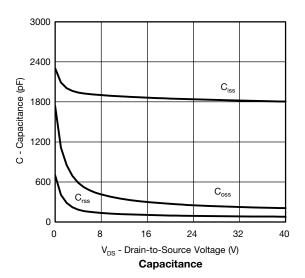


40 $T_{C} = 25 \, ^{\circ}C$ 10 $T_{C} = 125 \, ^{\circ}C$ $T_{C} = -55 \, ^{\circ}C$ $V_{GS} - Gate-to-Source Voltage (V)$

Transfer Characteristics

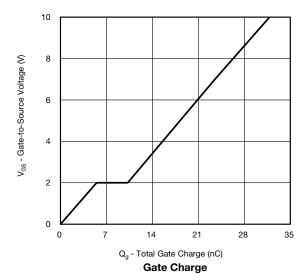


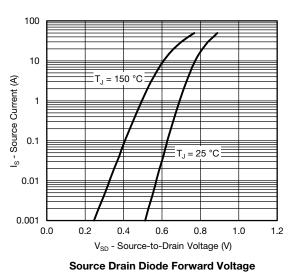
Transconductance

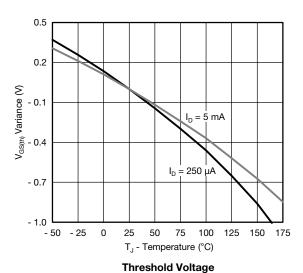


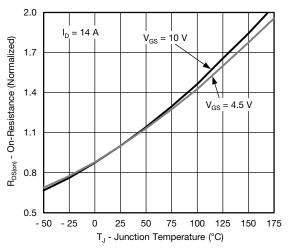


N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

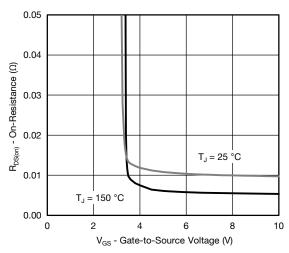




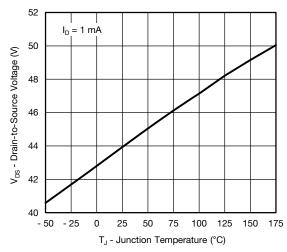




On-Resistance vs. Junction Temperature



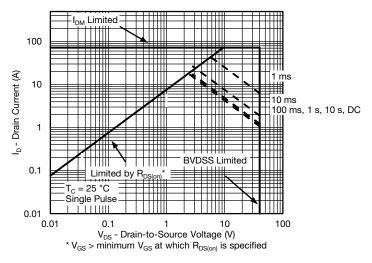
On-Resistance vs. Gate-to-Source Voltage



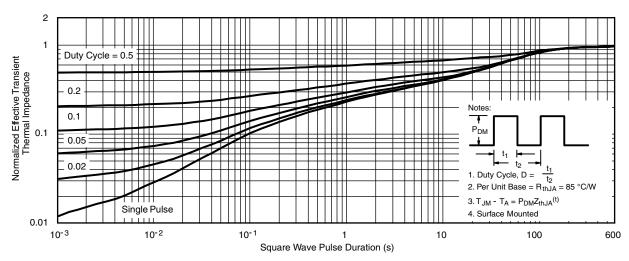
Drain Source Breakdown vs. Junction Temperature



N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



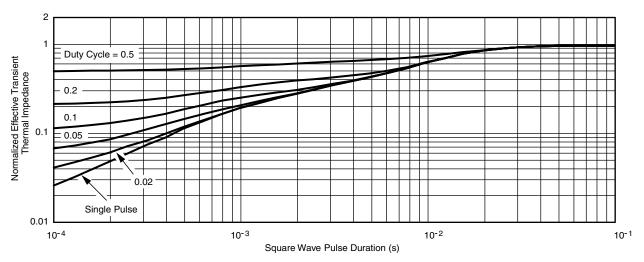
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix

N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

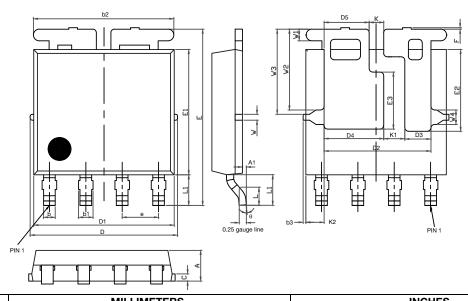
can widely vary depending on actual application parameters and operating conditions.

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62767.



PowerPAK® SO-8L Assymetric Case Outline



DIM	DIM. MILLIMETERS			INCHES				
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	1.00	1.07	1.14	0.039	0.042	0.045		
A1	0.00	0.06	0.13	0.000	0.003	0.005		
b	0.33	0.41	0.48	0.013	0.016	0.019		
b1	0.44	0.51	0.58	0.017	0.020	0.023		
b2	4.80	4.90	5.00	0.189	0.193	0.197		
b3	0.04	0.12	0.20	0.002	0.005	0.008		
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	5.00	5.13	5.25	0.197	0.202	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.63	3.73	3.83	0.143	0.147	0.151		
D3	0.81	0.91	1.01	0.032	0.036	0.040		
D4	1.98	2.08	2.18	0.078	0.082	0.086		
D5	1.47	1.57	1.67	0.058	0.062	0.066		
е	1.20	1.27	1.34	0.047	0.050	0.053		
Е	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	2.75	2.85	2.95	0.108	0.112	0.116		
E3	1.89	1.99	2.09	0.074	0.078	0.082		
F	0.05	0.12	0.19	0.002	0.005	0.007		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
K	0.41	0.51	0.61	0.016	0.020	0.024		
K1	0.64	0.74	0.84	0.025	0.029	0.033		
K2	0.54	0.64	0.74	0.021	0.025	0.029		
W	0.13	0.23	0.33	0.005	0.009	0.013		
W1	0.31	0.41	0.51	0.012	0.016	0.020		
W2	2.72	2.82	2.92	0.107	0.111	0.115		
W3	2.86	2.96	3.06	0.113	0.117	0.120		
W4	0.41	0.51	0.61	0.016	0.020	0.024		
θ	5°	10°	12°	5°	10°	12°		

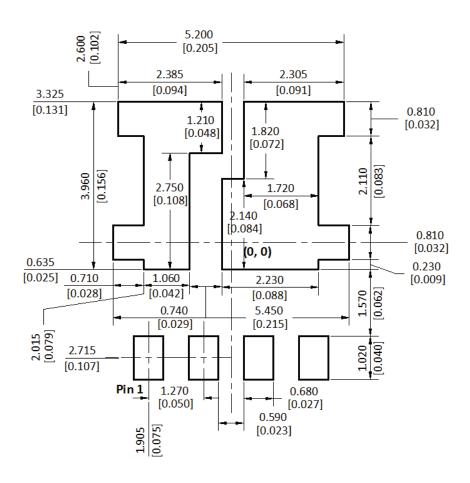
DWG: 6009

Note

• Millimeters will govern



RECOMMENDED MINIMUM PADs FOR PowerPAK® SO-8L DUAL ASYMMETRIC



Recommended Minimum Pads Dimensions in mm [inches]



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