Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

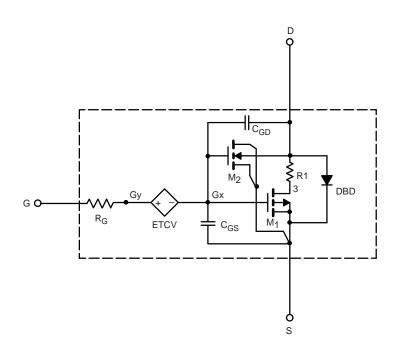
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- · Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer
to the appropriate datasheet of the same number for guaranteed specification limits.

SPICE Device Model Si7615DN

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	0.80	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 20 A	0.0034	0.0031	Ω
		V _{GS} = - 4.5 V, I _D = - 15 A	0.0047	0.0043	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 20 A	57	70	S
Diode Forward Voltage ^a	V _{SD}	I _S = - 4 A	- 0.69	- 0.68	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz	6060	6000	pF
Output Capacitance	C _{oss}		766	780	
Reverse Transfer Capacitance	C _{rss}		412	820	
Total Gate Charge	Qg	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$	107	122	nC
		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 10 A	54	62	
Gate-Source Charge	Q _{gs}		9.4	9.4	
Gate-Drain Charge	Q _{gd}		17.2	17.2	

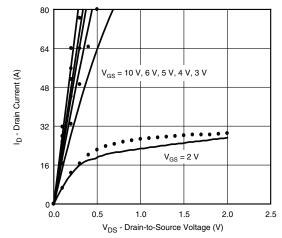
Notes

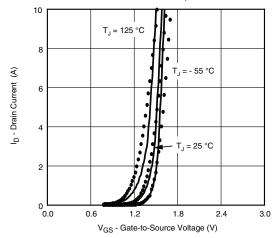
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

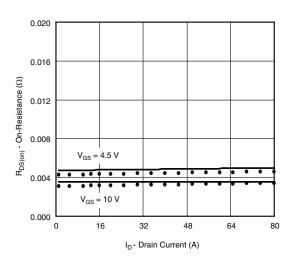
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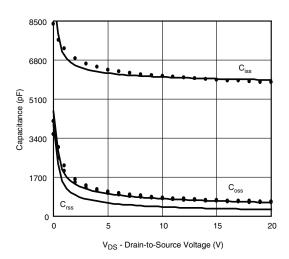
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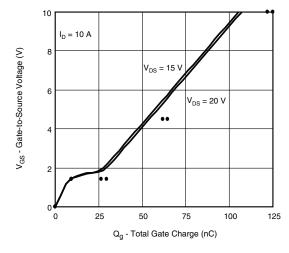
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

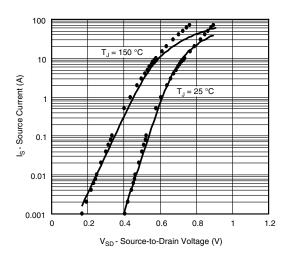












Note

• Dots and squares represent measured data.

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