Low Voltage, Dual DPDT and Quad SPDT Analog Switches

DESCRIPTION

The DG2018 and DG2019 are low voltage, single supply analog switches. The DG2018 is a dual double-pole/double-throw (DPDT) with two control inputs that each controls a pair of single-pole/double-throw (SPDT). The DG2019 uses one control pin to operate four independent SPDT switches.

When operated on a + 3 V supply, the DG2018's control pins are compatible with 1.8 V digital logic. The DG2019 has an available feature of a V_L pin that allows a 1.0 V threshold for the control pin when V_L is powered with 1.5 V.

Built on Vishay Siliconix's low voltage submicron CMOS process, the DG2018 and DG2019 are ideal for high performance switching of analog signals; providing low on-resistance (6 Ω at + 2.7 V), fast speed (T_{on}, T_{off} at 42 ns and 16 ns), and a bandwidth that exceeds 180 MHz.

The DG2018 and DG2019 were designed to offer solutions that extend beyond audio/video functions, to providing the performance required for today's demanding mixed-signal switching in portable applications.

An epitaxial layer prevents latch-up. Brake-before-make is guaranteed for all SPDT's. All switches conduct equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low voltage operation (1.8 V to 5.5 V)
- Low on resistance
  - $R_{DS(on)}$: 6 Ω at 2.7 V
- Low voltage logic compatible
  - DG2019: V_{INH} = 1 V
- High bandwidth: 180 MHz
- QFN-16 package

BENEFITS

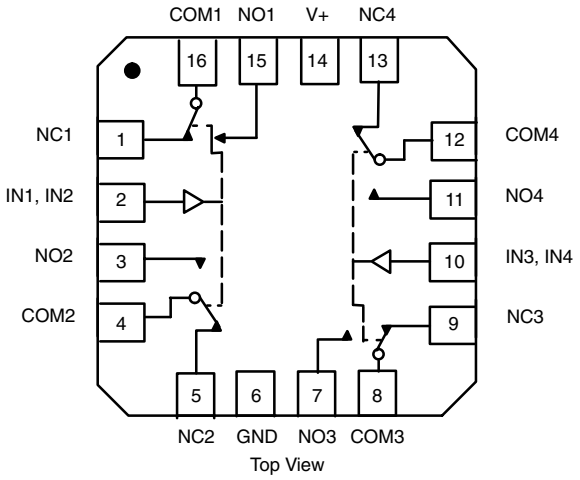
- Ideal for both analog and digital signal switching
- Reduced power consumption
- High accuracy
- Reduced PCB space
- Fast switching
- Low leakage

APPLICATIONS

- Cellular phones
- Audio and video signal routing
- PCMCIA cards
- Battery operated systems
- Portable instrumentation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2018DN
QFN-16 (3 X 3)



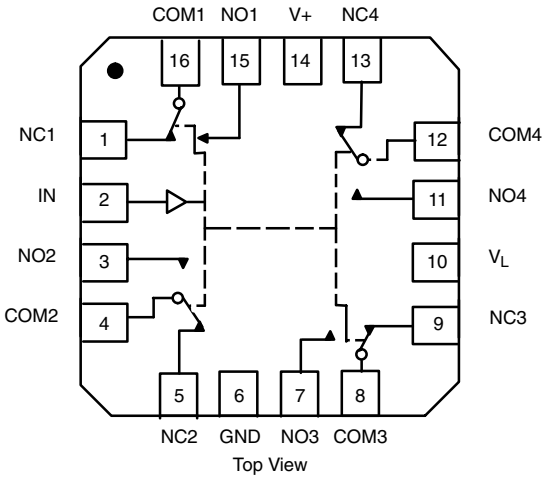
Top View

TRUTH TABLE		
IN1, IN2		
Logic	**NC1 and NC2**	**NO1 and NO2**
0	ON	OFF
1	OFF	ON
IN3, IN4		
Logic	**NC3 and NC4**	**NO3 and NO4**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85 °C	QFN-16 (3 x 3 mm)	DG2018DN

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2019DN
QFN-16 (3 X 3)



Top View

TRUTH TABLE		
Logic	**NC1, 2, 3 and 4**	**NO1, 2, 3 and 4**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85 °C	QFN-16 (3 x 3 mm)	DG2019DN

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % Duty Cycle)		± 100	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages)[b]	QFN-16 (3 x 3 mm)[c]	850	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 4.0 mW/°C above 70 °C.

SPECIFICATIONS V+ = 3 V

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, (DG2018 Only) V_{IN} = 0.5 or 1.4 V[e] (DG2019 Only) V_L = 1.5 V, V_{IN} = 0.4 or 1.0 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 10 mA		Room Full		6	12 15	Ω
R_{ON} Flatness	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA		Room		0.5	2	Ω
R_{ON} Match Between Channels	ΔR_{ON}			Room		0.6	3	Ω
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V		Room Full	- 1 - 10	0.3	1 10	nA
	$I_{COM(off)}$			Room Full	- 1 - 10	0.3	1 10	nA
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V		Room Full	- 1 10	0.3	1 10	nA
Digital Control								
Input High Voltage	V_{INH}		DG2018	Full	1.4			V
		V_L = 1.5 V	DG2019	Full	1.0			V
Input Low Voltage	V_{INL}		DG2018	Full			0.5	V
		V_L = 1.5 V	DG2019	Full			0.4	V
Input Capacitance	C_{in}	f = 1 MHz		Full		9		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	- 1		1	µA
Dynamic Characteristics								
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF		Room Full		42	55 65	ns
Turn-Off Time	t_{OFF}			Room Full		16	25 35	ns
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 2.0 V, R_L = 50 Ω, C_L = 35 pF		Full	1			ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω		Room		- 1.46		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		Room		- 67		dB
Crosstalk[d]	X_{TALK}			Room		- 72		dB
Bandwidth[d]	BW			Room		180		MHz
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		9		pF
	$C_{NC(off)}$			Room		9		pF
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		30		pF
	$C_{NC(on}$			Room		30		pF
Power Supply								
Power Supply Current	I+	V_{IN} = 0 or V+		Full		0.01	1.0	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

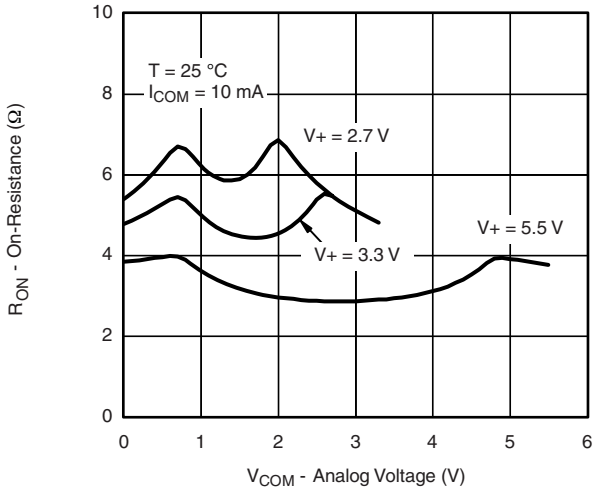
SPECIFICATIONS V+ = 5 V

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, (DG2018 Only) V_{IN} = 0.8 or 1.8 V[e] (DG2019 Only) V_L = 1.5 V, V_{IN} = 0.4 or 1.0 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance	R_{ON}	V+ = 4.5 V, V_{COM} = 3 V, I_{NO}, I_{NC} = 10 mA		Room Full		4	8 10	Ω
R_{ON} Flatness	R_{ON} Flatness	V+ = 4.5 V V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA		Room		0.6	1.2	Ω
R_{ON} Match Between Channels	ΔR_{ON}			Room		0.6	1.2	Ω
Switch Off Leakage Current[f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V		Room Full	- 1 - 10	0.03	1 10	nA
	$I_{COM(off)}$			Room Full	- 1 - 10	0.03	1 10	nA
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V		Room Full	- 1 - 10	0.03	1 10	nA
Digital Control								
Input High Voltage	V_{INH}		DG2018	Full	1.8			V
		V_L = 1.5 V	DG2019	Full	1.0			V
Input Low Voltage	V_{INL}		DG2018	Full			0.8	V
		V_L = 1.5 V	DG2019	Full			0.4	V
Input Capacitance	C_{in}			Full		9		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	1		1	µA
Dynamic Characteristics								
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF		Room Full		44	48 52	ns
Turn-Off Time	t_{OFF}			Room Full		19	33 35	ns
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 3 V, R_L = 50 Ω, C_L = 35 pF		Full	1			ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω		Room		- 2.46		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		Room		- 67		dB
Crosstalk[d]	X_{TALK}			Room		- 72		dB
Bandwidth[d]	BW			Room		180		MHz
Source-Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		7.5		pF
	$C_{NC(off)}$			Room		7.5		pF
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		30		pF
	$C_{NC(on}$			Room		30		pF
Power Supply								
Power Supply Range	V+				1.8		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+		Full		0.01	1.0	µA

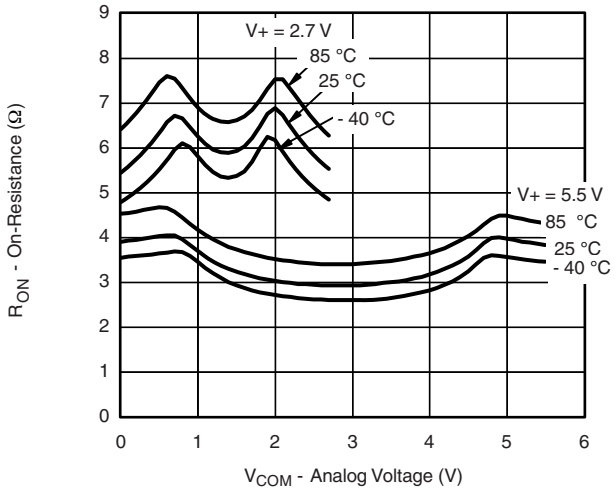
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

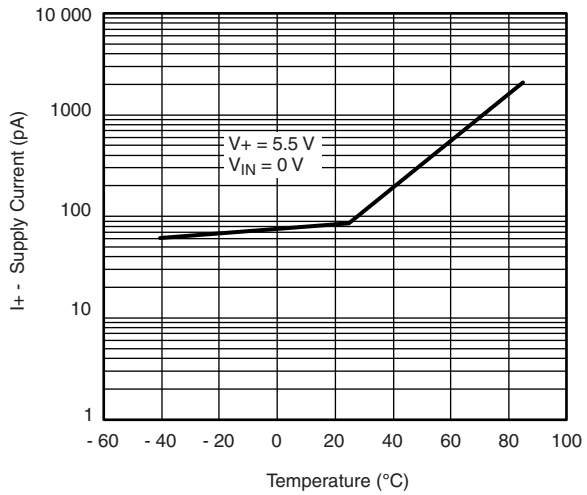
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



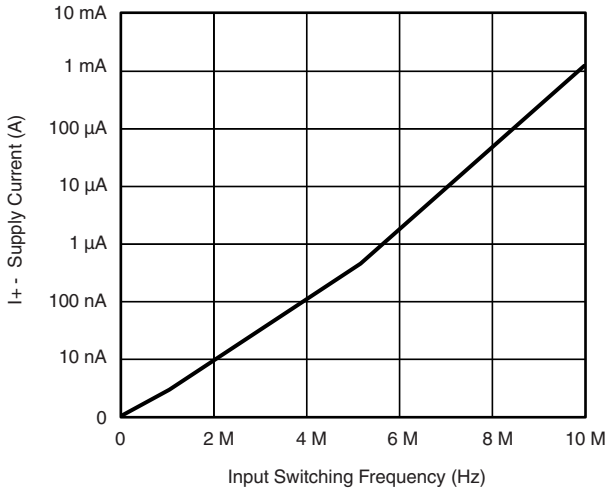
R_{ON} vs. V_{COM} and Supply Voltage



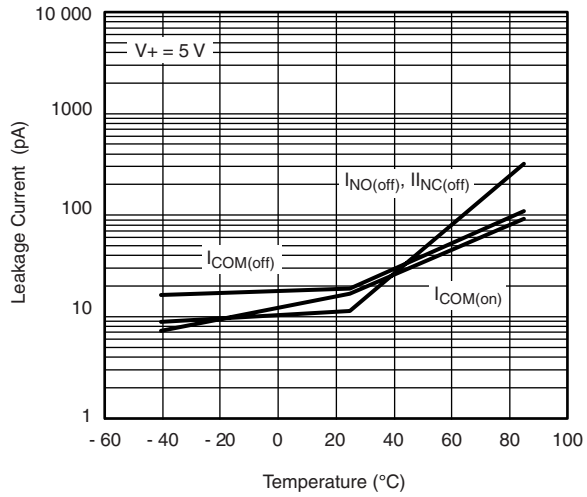
R_{ON} vs. Analog Voltage and Temperature



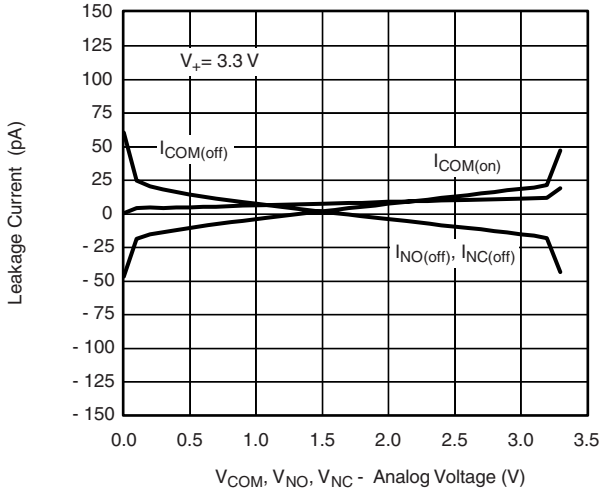
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

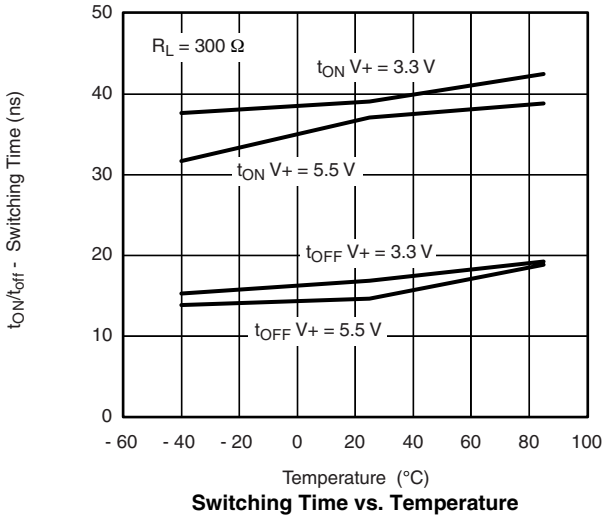


Leakage Current vs. Temperature

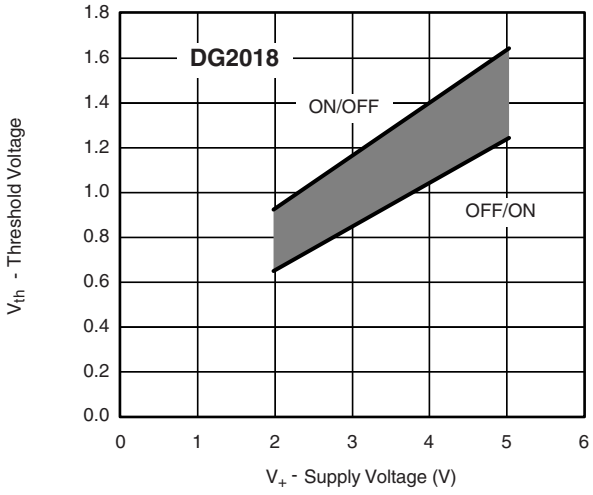


Leakage vs. Analog Voltage

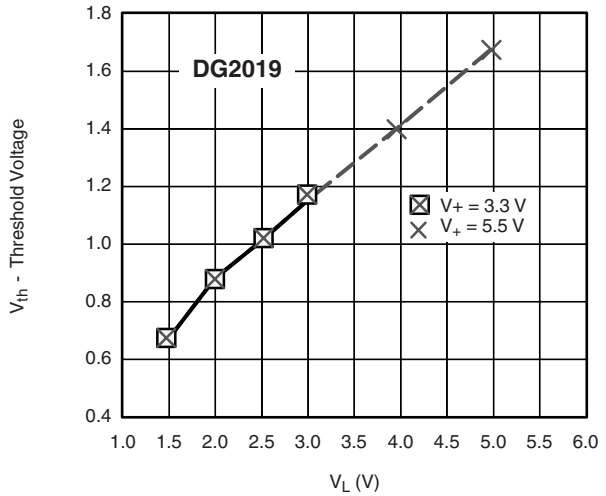
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



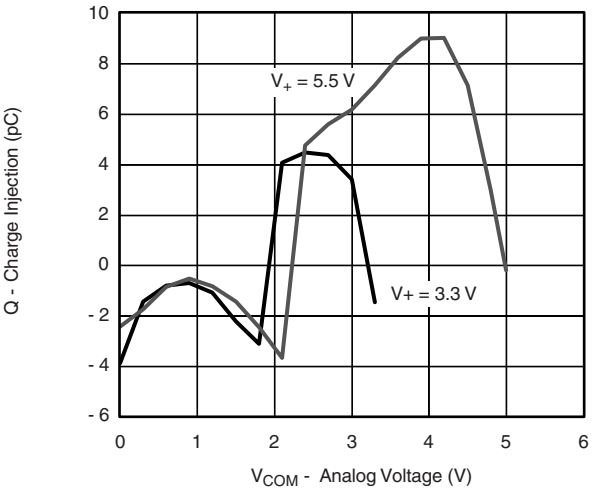
Switching Time vs. Temperature and Supply Voltage



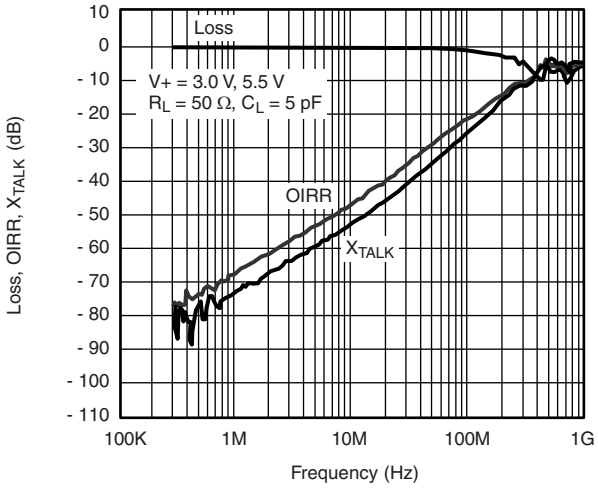
Switching Voltage vs. Supply Voltage (V+)



V_{IN} vs. V_L (Typ)

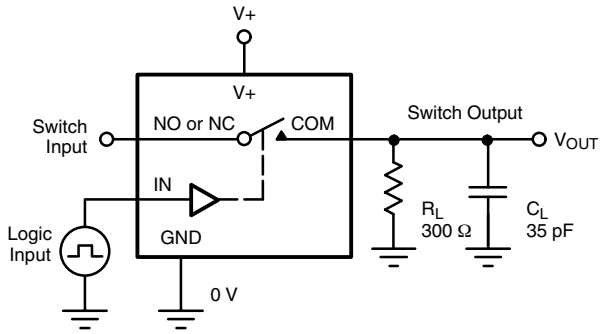


Charge Injection at Source vs. Analog Voltage



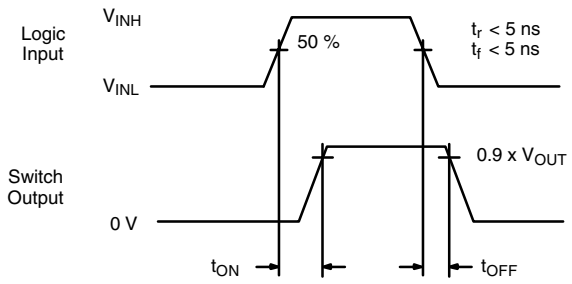
Insertion Loss, Off Isolation and Crosstalk vs. Frequency

TEST CIRCUITS



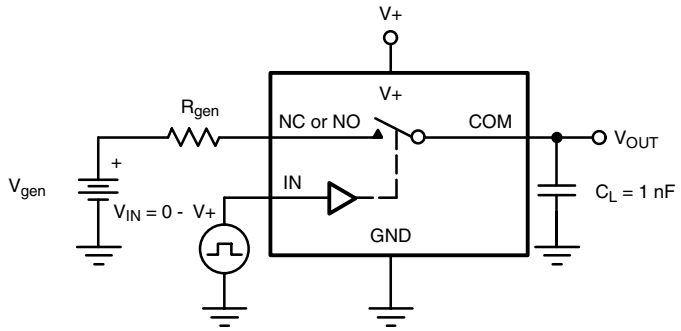
C_L (includes fixture and stray capacitance)

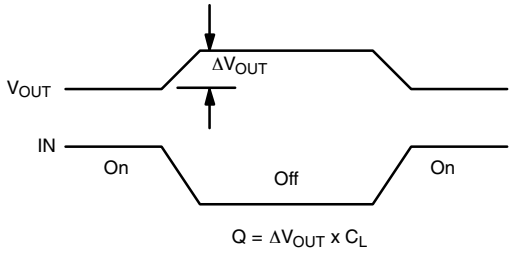
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

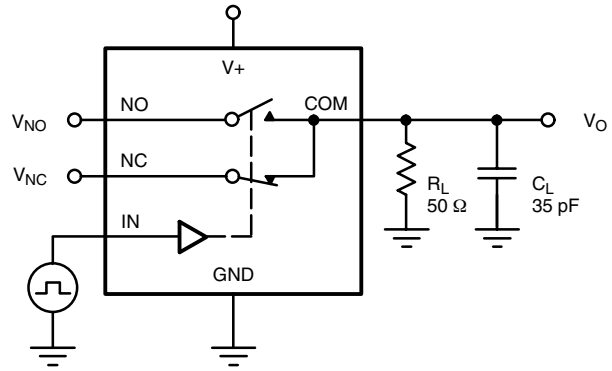




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection



C_L (includes fixture and stray capacitance)

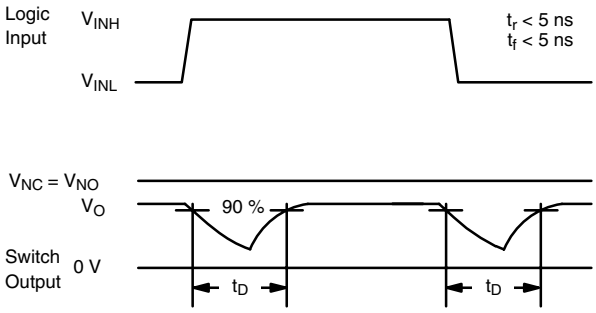


Figure 3. Break-Before-Make Interval

TEST CIRCUITS

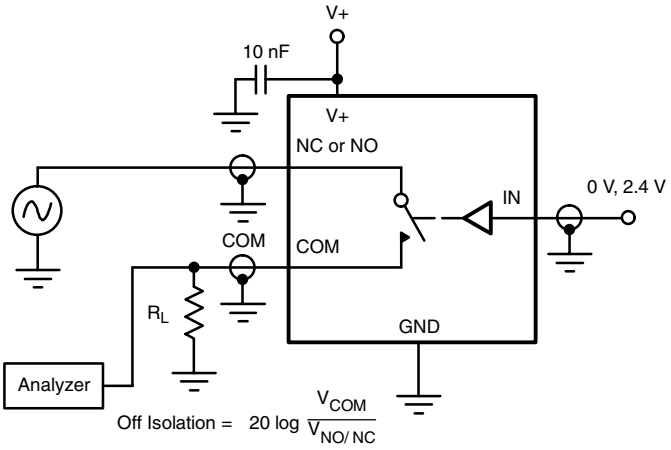


Figure 4. Off-Isolation

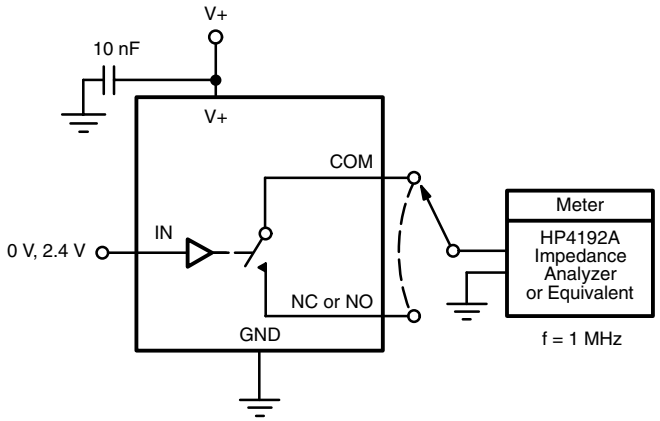
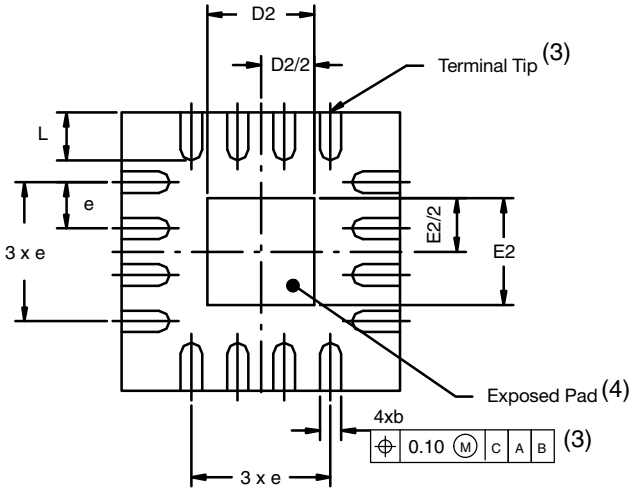


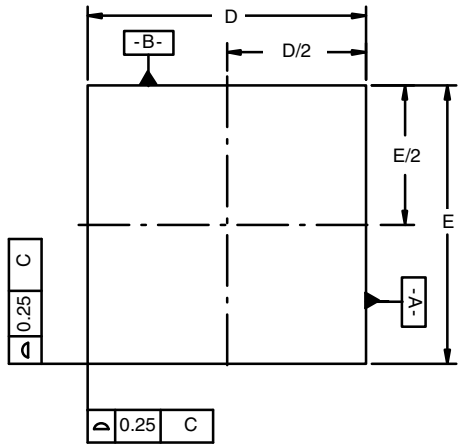
Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72342.

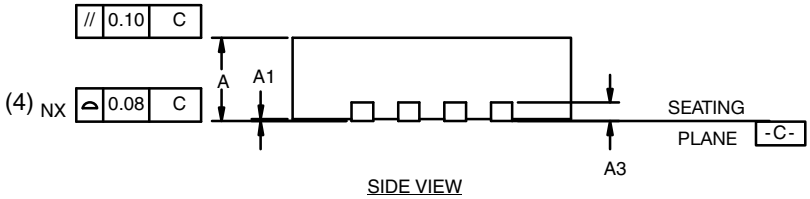
QFN-16 Lead (3 x 3)



BOTTOM VIEW



TOP VIEW



SIDE VIEW

Notes

(1) All dimensions are in millimeters.
(2) N is the total number of terminals.
(3) Dimension b applies to metallized terminal and is measured between 0.25 and 0.30 mm from terminal tip.
(4) Coplanarity applies to the exposed heat sink slug as well as the terminal.
(5) The pin #1 identifier may be either a mold or marked feature, it must be located within the zone indicated.

DIM.	VARIATION 1						VARIATION 2					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039	0.80	0.90	1.00	0.031	0.035	0.039
b	0.18	0.23	0.30	0.007	0.009	0.012	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.00	1.15	1.25	0.039	0.045	0.049	1.50	1.70	1.80	0.059	0.067	0.071
E	2.90	3.00	3.10	0.114	0.118	0.122	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.00	1.15	1.25	0.039	0.045	0.049	1.50	1.70	1.80	0.059	0.067	0.071
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020	0.30	0.40	0.50	0.012	0.016	0.020
ECN: T16-0233-Rev. D, 09-May-16 DWG: 5899												

Disclaimer

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