



# P-Channel 100 V (D-S) MOSFET

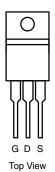
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$ Max.	I <sub>D</sub> (A) <sup>c</sup>	Q <sub>g</sub> (Typ.)		
- 100	0.138 at V <sub>GS</sub> = - 10 V	- 16.3			
	0.141 at V <sub>GS</sub> = - 7.5 V	- 16.1	24 nC		
	0.142 at V <sub>GS</sub> = - 6 V	- 16.1			

#### **FEATURES**

- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



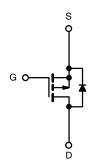
#### TO-220AB



Drain connected to Tab

## **APPLICATIONS**

- DC/DC Converters
- Motor Control



P-Channel MOSFET

## **Ordering Information:**

SUP25P10-138-GE3 (Lead (Pb)-free and Halogen-free)

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	- 100	V		
Gate-Source Voltage	V <sub>GS</sub>	± 20	V		
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	T <sub>C</sub> = 25 °C	l <sub>D</sub>	- 16.3	A	
Continuous Diam Current (1) = 150°C)	T <sub>C</sub> = 125 °C		- 7.3		
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	- 40	A		
Avalanche Current L = 0.1 mH		I <sub>AS</sub>	- 25		
Single Pulse Avalanche Energy <sup>a</sup>	L = 0.1 IIII1	E <sub>AS</sub>	31.25	mJ	
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	73.5 <sup>b</sup>	W	
Tower Dissipation	T <sub>A</sub> = 25 °C	' D	3.1		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient Free Air	R <sub>thJA</sub>	40	°C/W		
Junction-to-Case	R <sub>thJC</sub>	1.7			

#### Notes:

a. Duty cycle  $\leq$  1 %.

b. See SOA curve for voltage derating.

c.  $T_C = 25$  °C

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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	- 100			V	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 2		- 4	]	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 105	mV/°C		
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	I <sub>D</sub> = - 250 μA		6.6		liiv/ C	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V <sub>DS</sub> = - 100 V, V <sub>GS</sub> = 0 V			- 1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -100 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			- 50	μΑ	
		$V_{DS} = -100 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$			- 200		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 20			Α	
		V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 6 A		0.115	0.138		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 7.5 V, I <sub>D</sub> = - 6 A		0.117	0.141	Ω	
		V <sub>GS</sub> = - 6 V, I <sub>D</sub> = - 6 A		0.118	0.142		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 6 A		18		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			2110			
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = - 50 V, f = 1 MHz		105		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			58			
Tatal Cata Chausac	Qg	V <sub>DS</sub> = - 50 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 6.7 A		40	60	nC	
Total Gate Charge <sup>c</sup>	<b>u</b> g			24	36		
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = -50 \text{ V}, V_{GS} = -6 \text{ V}, I_{D} = -6.7 \text{ A}$		12.5			
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			6.7			
Gate Resistance	$R_g$	f = 1 MHz	2	8	16	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			7	14		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = - 50 V, $R_L$ = 10 $\Omega$		12	20		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong -5 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		46	70		
Fall Time <sup>c</sup>	t <sub>f</sub>			40	60	1	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			12	20	ns	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = - 50 V, $R_L$ = 10 $\Omega$		105	160		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong -5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		36	54	-	
Fall Time <sup>c</sup>	t <sub>f</sub>			34	51		
Source-Drain Diode Ratings and Ch	aracteristics 7	C <sub>C</sub> = 25 °C <sup>b</sup>					
Continuous Current	I <sub>S</sub>				- 16.3		
Pulsed Current (t = 100 μs)	I <sub>SM</sub>		- 40 A		A		
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = - 5 A, V <sub>GS</sub> = 0 V		- 0.85	- 1.5	V	
Reverse Recovery Time	t <sub>rr</sub>	. 35		70	105	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = - 5 A, dl/dt = 100 A/μs		- 7	- 14	A	
Reverse Recovery Charge	Q <sub>rr</sub>	' '		220	330	nC	

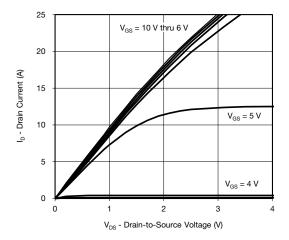
## Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

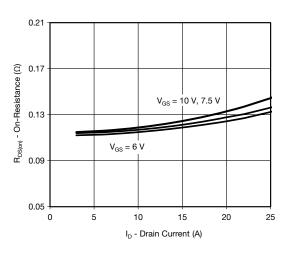
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



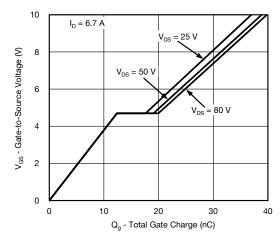
# TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



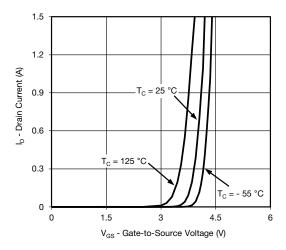
#### **Output Characteristics**



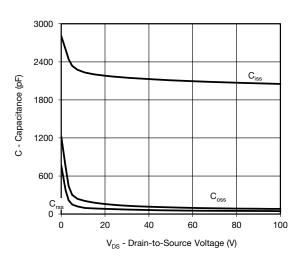
On-Resistance vs. Drain Current and Gate Voltage



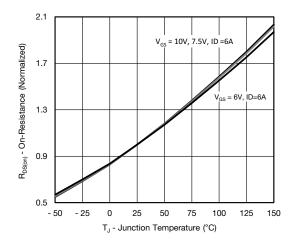
**Gate Charge** 



**Transfer Characteristics** 



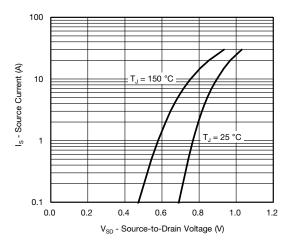
Capacitance



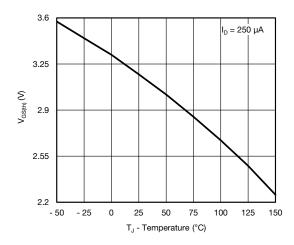
On-Resistance vs. Junction Temperature

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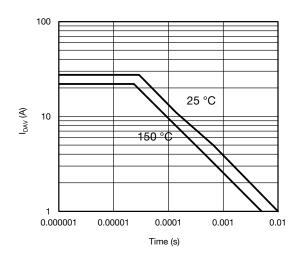
# TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



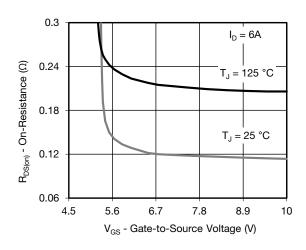
## Source-Drain Diode Forward Voltage



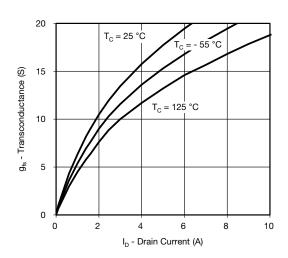
## Threshold Voltage



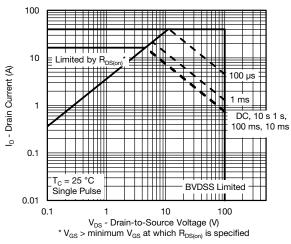
Single Pulse Avalanche Capability



## On-Resistance vs. Gate-to-Source Voltage



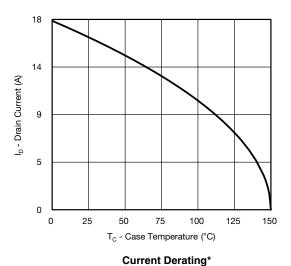
Transconductance

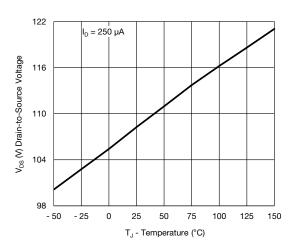


Safe Operating Area, Junction-to-Case



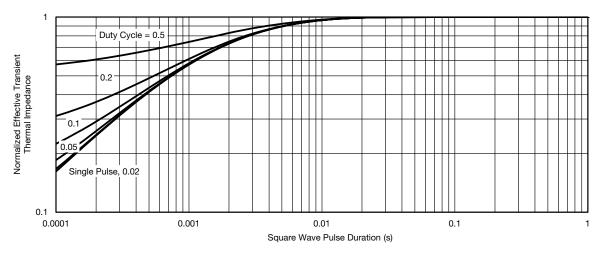
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Drain Source Breakdown vs. Junction Temperature

<sup>\*</sup> The power dissipation P<sub>D</sub> is based on T<sub>J(max.)</sub> = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heats inking is used. It is used to determine the current rating, when this rating falls below the package



Normalized Thermal Transient Impedance, Junction-to-Case

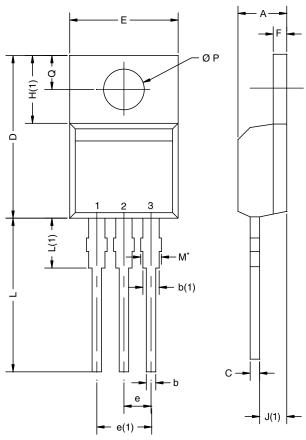
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Document Number: 62885 S13-2074-Rev. A, 30-Sep-13 For technical questions, contact: pmostechsupport@vishay.com





# **TO-220AB**



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		D2

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
С	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
ØР	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: T14-0413-Rev. P, 16-Jun-14 DWG: 5471				

### Note

 $<sup>^{\</sup>star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM

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