Monolithic Quad SPST CMOS Analog Switches

(Obsolete for non-hermetic. Use DG201B/202B as pin-for-pin replacements.)

FEATURES

- ±15-V Input Range
- Low Off Leakage—$I_{D(on)}$: 0.1 nA
- Low On-Resistance—$r_{DS(on)}$: 115 Ω
- 44-V Maximum Supply Ratings
- TTL and CMOS Compatible

BENEFITS

- Wide Input Range
- Low Distortion Switching
- Can Be Driven from Comparators or Op Amps Without Limiting Resistors

APPLICATIONS

- Disk Drives
- Radar Systems
- Communications Systems
- Sample-and-Hold

DESCRIPTION

The DG201A_MIL and DG202_MIL are quad SPST analog switches designed to provide accurate switching over a wide range of input signals. When combining a low on-resistance and a wide signal range (±15 V) with low charge-transfer these devices are well suited for industrial and military applications.

Built on Vishay Siliconix' high voltage metal gate process to achieve optimum switch performance, each switch conducts equally well in both directions when on. When off these switches will block up to 30 V peak-to-peak and have a 44-V absolute maximum power supply rating.

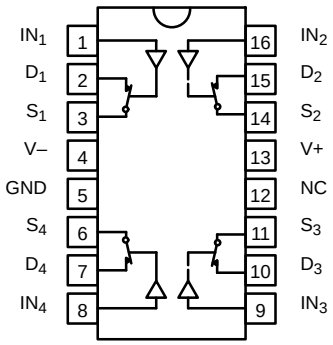
These two devices are differentiated by the type of switch actions (See Truth Table).

The DG201A_MIL/202_MIL are available in hermetic packages. For plastic packages, use the DG201B/202B as pin-for-pin replacements.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG201A_MIL

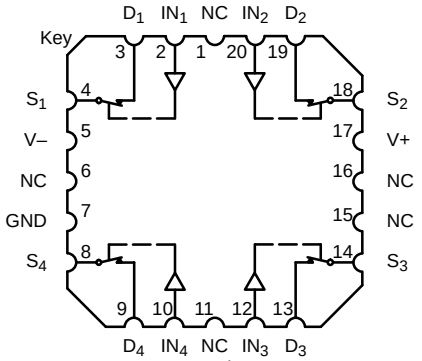
Dual-In-Line



Top View

DG201A_MIL

LCC



Top View

Logic	DG201A_MIL	DG202_MIL
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
–55 to 125°C	16-Pin CerDIP	DG201AAK
		DG201AAK/883, JM38510/12302BEA
		7705301EA
		DG202AK
		DG202AK/883
–55 to 125°C	16-Pin Sidebraze	JM38510/12302BEC
		7705301EC
	LCC-20	77053012A

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ . . . . . 44 V

GND . . . . . 25 V

Digital Inputs[a] V_S, V_D . . . . . (V–) –2 V to (V+) +2 V
or 20 mA, whichever occurs first

Current, Any Terminal Except S or D . . . . . 30 mA

Continuous Current, S or D . . . . . 20 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) . . . . . 70 mA

Storage Temperature (K, Z Suffix) . . . . . –65 to 150°C
(J, Y Suffix) . . . . . –65 to 125°C

Power Dissipation (Package)b
16-Pin CerDIP and Sidebraze[c] . . . . . 900 mW
LCC-20[d] . . . . . 750 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 12 mW/°C above 75°C
d. Derate 10 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

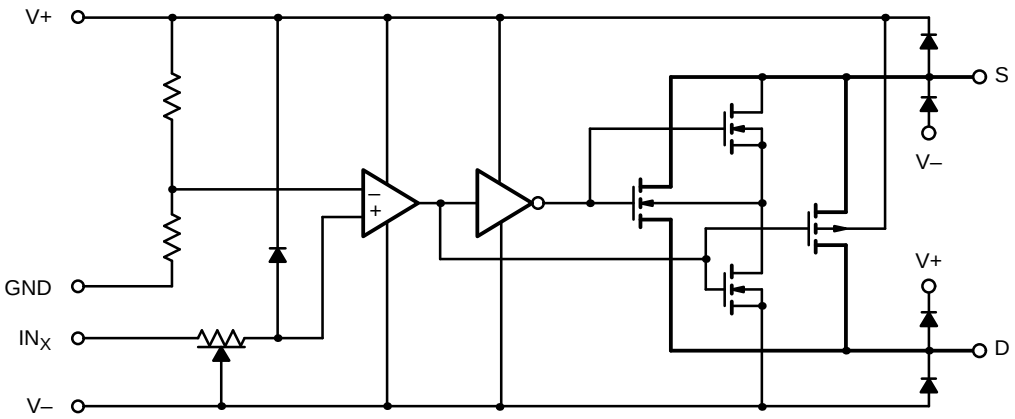


FIGURE 1.

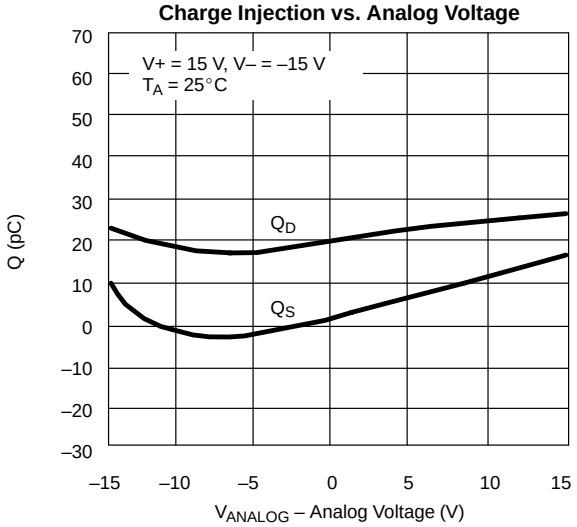
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V– = –15V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	A Suffix –55 to 125°C Min[d]	Typ[c]	Max[d]	Unit
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room		115	175	Ω
			Full			250	
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Full	–1 –100	±0.02	1 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room Full	–1 –100	±0.02	1 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±14 V	Room Full	–1 –200	±0.15	1 200	
Digital Control							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4 V	Room Full	–1 –1	–0.0004		µA
		V_{IN} = 15 V	Room Full		0.003	1 10	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	–1 –10	–0.0004		
Dynamic Characteristics							
Turn-On Time	t_{ON}	See Switching Time Test Circuit	Room		480	600	ns
Turn-Off Time	t_{OFF}		Room		370	450	
Charge Injection	Q	C_L = 1000 pF, V_g= 0 V R_g = 0 Ω	Room		20		pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, V_{IN} = 5 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		5		
Channel On Capacitance	$C_{D(on)}$ + $C_{S(on)}$	V_D = V_S = 0 V, V_{IN} = 0 V f = 1 MHz	Room		16		
Off Isolation	OIRR	V_{IN} = 5 V, R_L = 75 Ω V_S = 2 V, f = 100 kHz	Room		70		dB
Channel-to-Channel Crosstalk	X_{TALK}		Room		90		
Power Supply							
Positive Supply Current	I+	All Channels On or Off	Room		0.9	2	mA
Negative Supply Current	I–		Room	–1	–0.3		

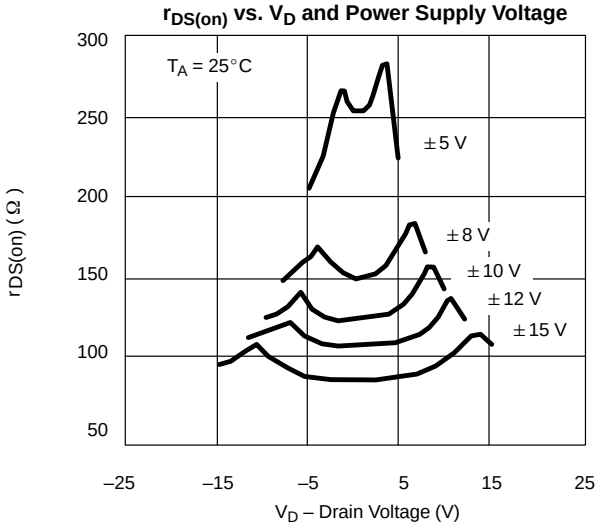
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

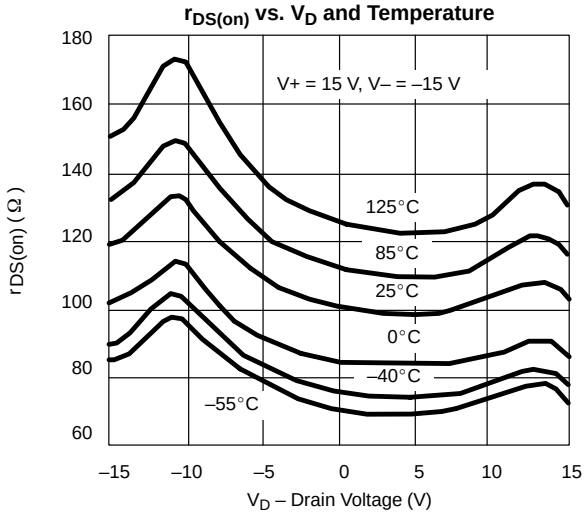
Charge Injection vs. Analog Voltage



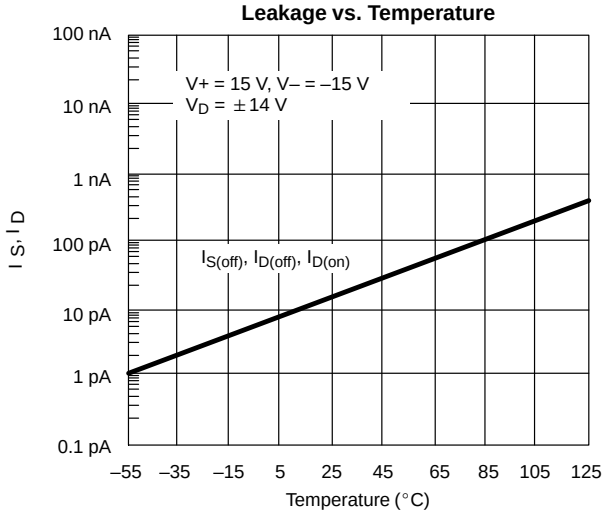
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



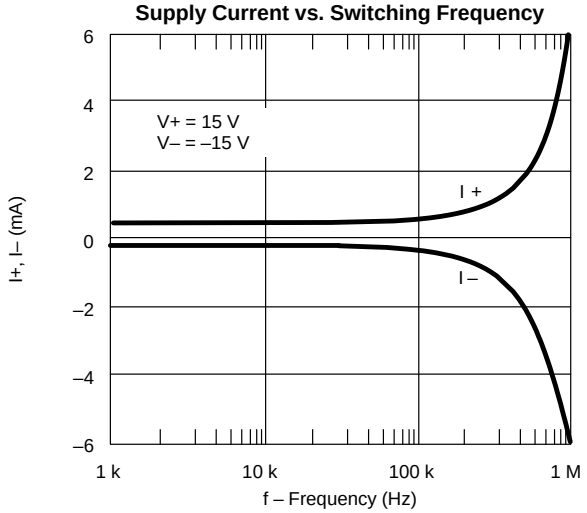
$r_{DS(on)}$ vs. V_D and Temperature



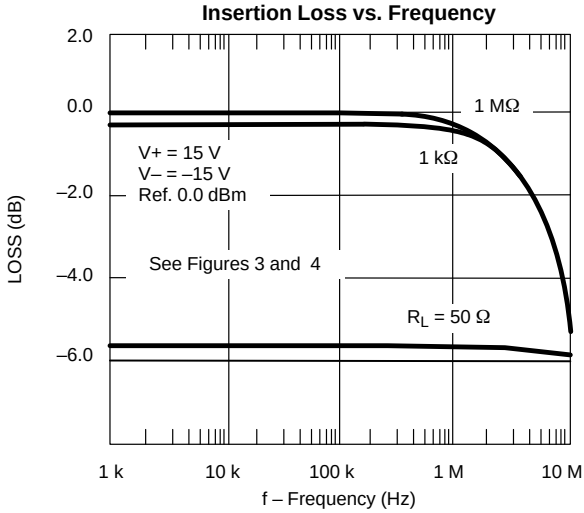
Leakage vs. Temperature



Supply Current vs. Switching Frequency

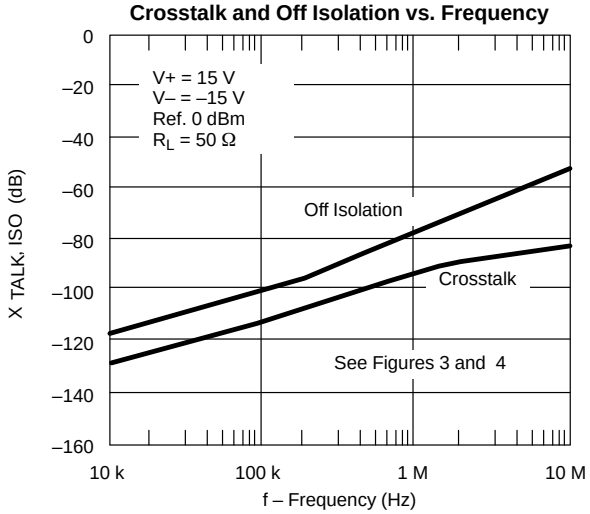


Insertion Loss vs. Frequency

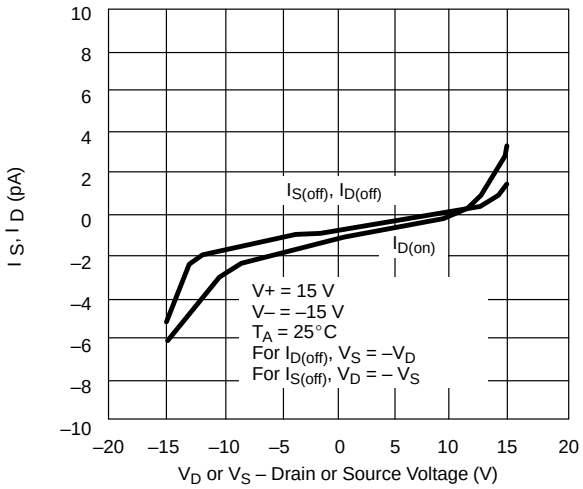


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

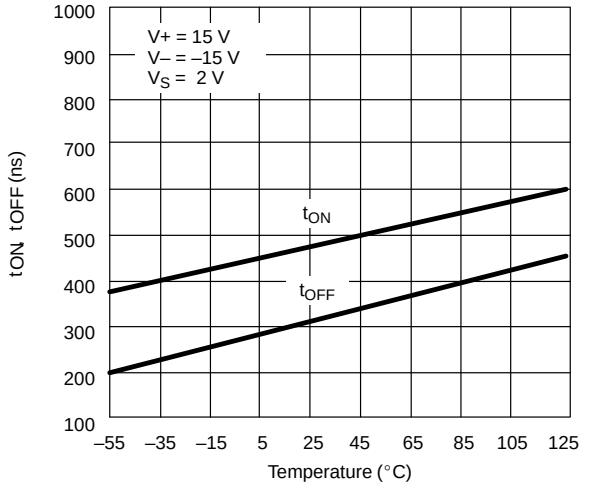
Crosstalk and Off Isolation vs. Frequency



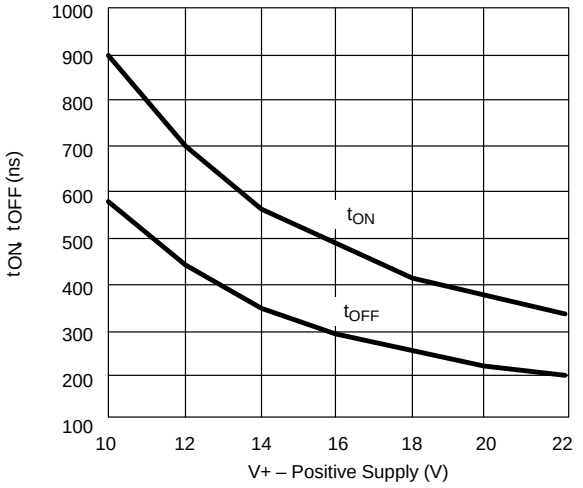
Leakage Current vs. Analog Voltage



Switching Time vs. Temperature



Switching Time vs. Power Supply Voltage



TEST CIRCUITS

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

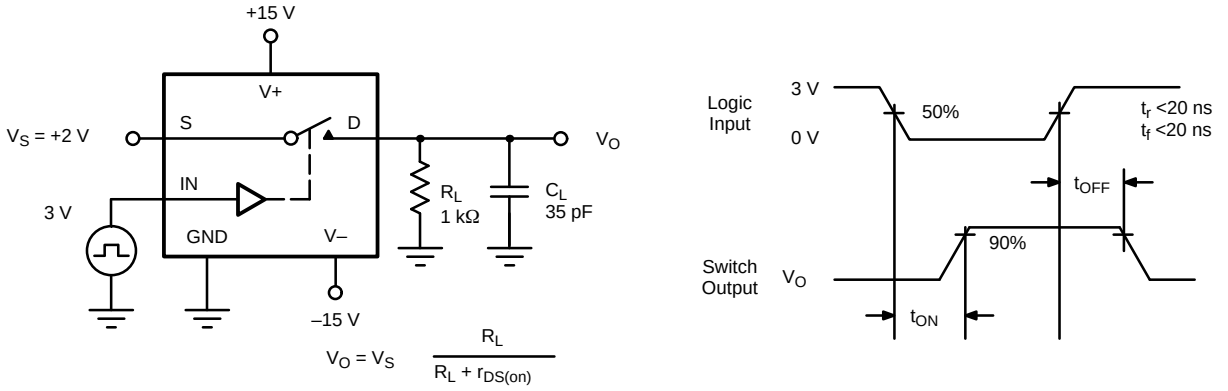


FIGURE 2. Switching Time

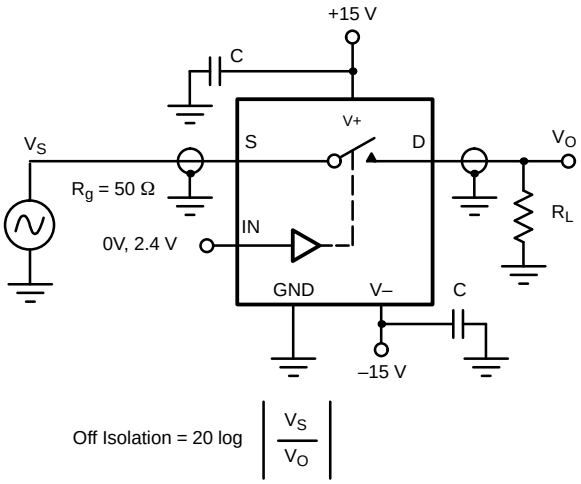


FIGURE 3. Off Isolation

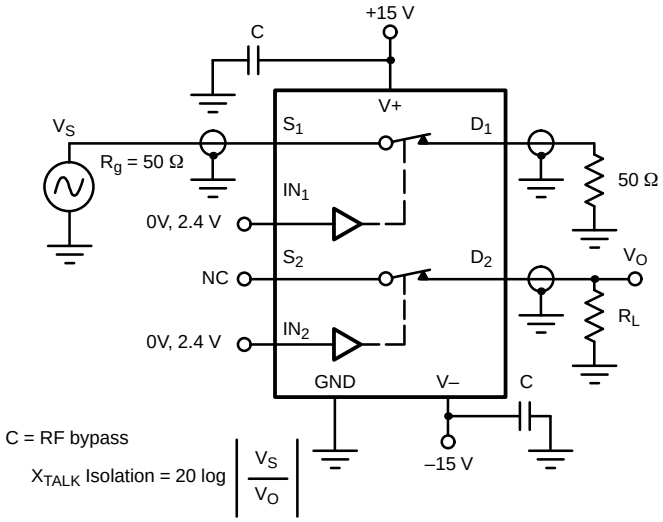
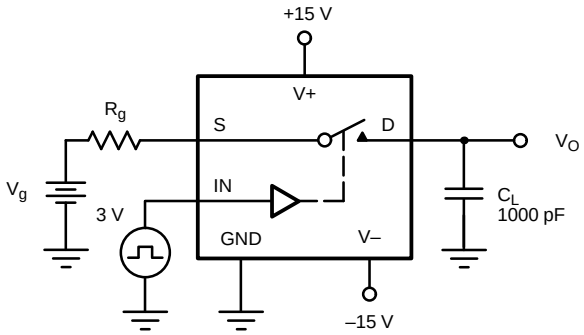
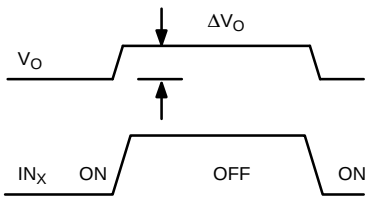


FIGURE 4. Channel-to-Channel Crosstalk





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

FIGURE 5. Charge Injection

APPLICATION HINTS[a]			
V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	–15	2.4/0.8	–15 to 15
10	–12	2.4/0.8	–12 to 12
12	–10	2.2/0.6	–10 to 10
8[b]	–8	2.0/0.5	–8 to 8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Operation below ±8 V is not recommended.

APPLICATIONS

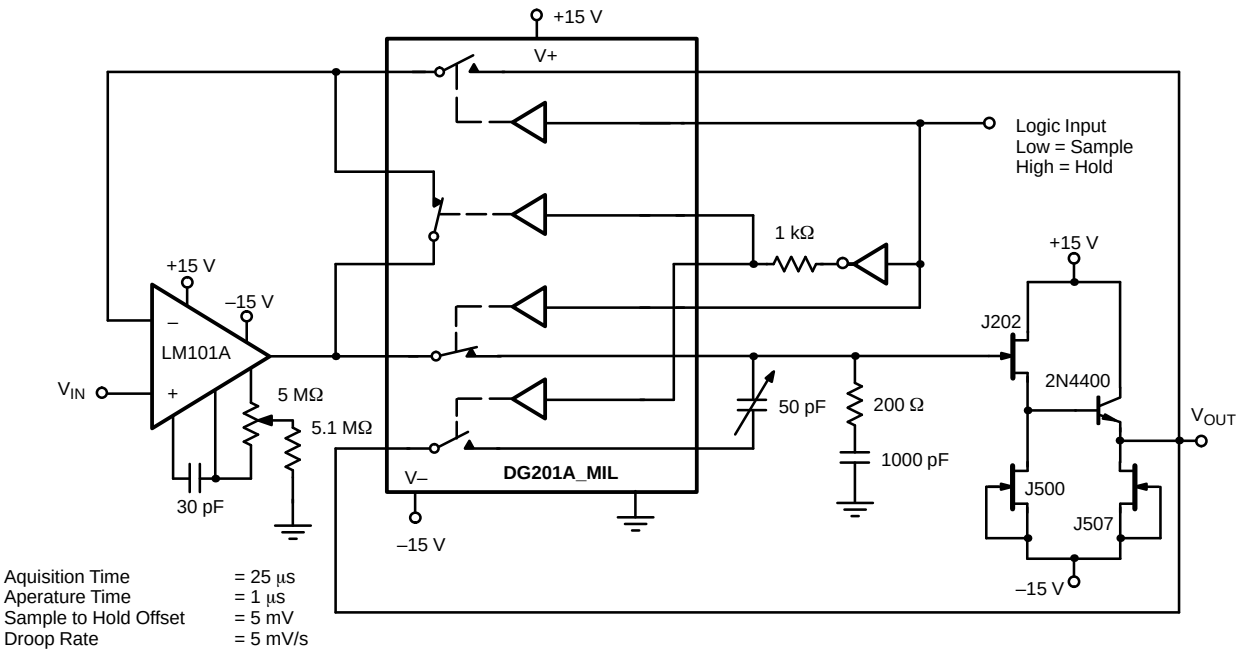


FIGURE 6. Sample-and-Hold

APPLICATIONS

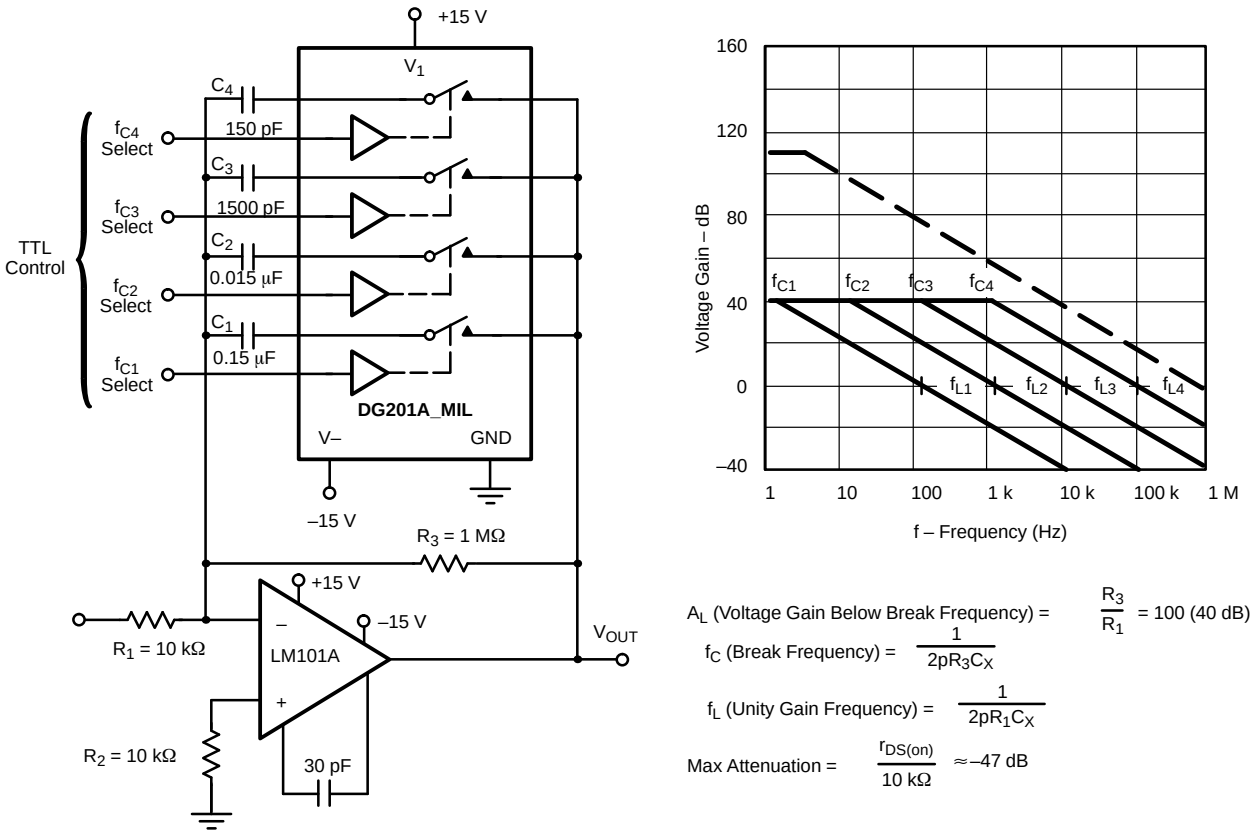


FIGURE 7. Active Low Pass Filter with Digitally Selected Break Frequency

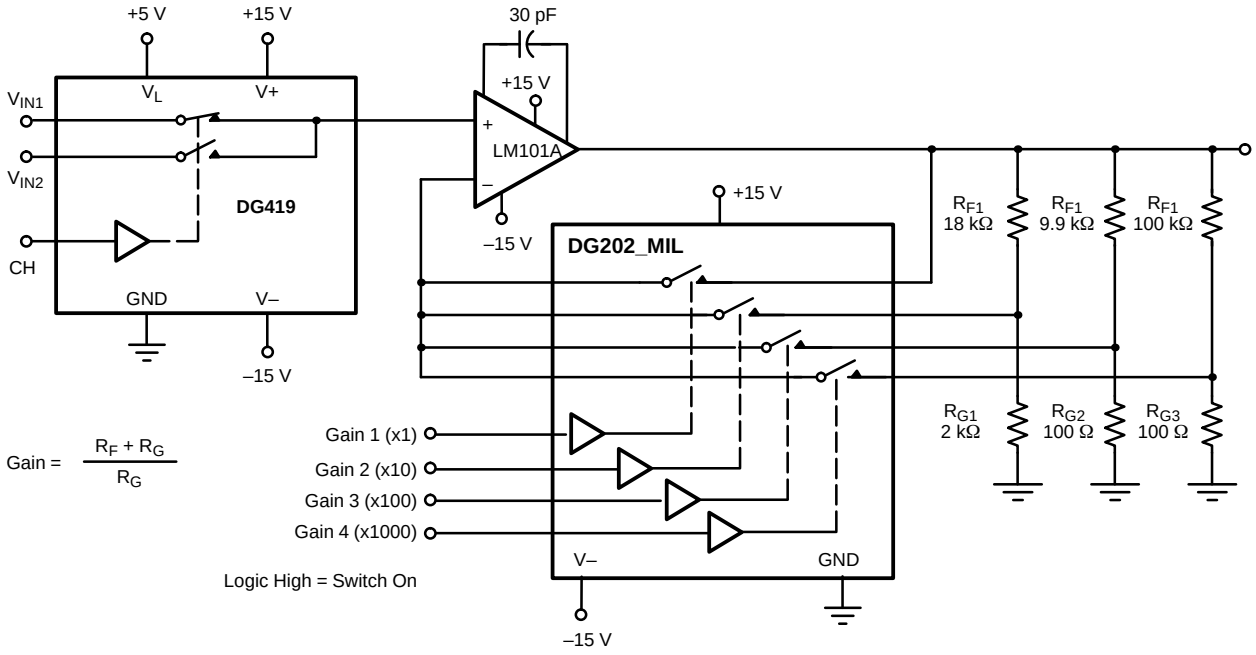


FIGURE 8. A Precision Amplifier with Digitally Programable Input and Gains

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