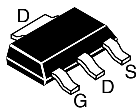
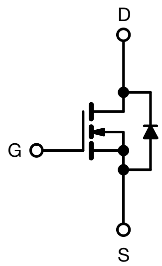
Power MOSFET

SOT-223





N-Channel MOSFET

Marking code: LB

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 5.0 V	0.54
Q_g (Max.) (nC)	6.1	
Q_{gs} (nC)	2.6	
Q_{gd} (nC)	3.3	
Configuration	Single	

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Logic-level gate drive
- $R_{DS(on)}$ specified at V_{GS} = 4 V and 5 V
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

HALOGEN FREE Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Lead (Pb)-free and halogen-free	SiHLL110TR-GE3
	IRLL110TRPbF-BE3 [a, b]
Lead (Pb)-free	IRLL110TRPbF [a]

Notes

a. See device orientation

b. “-BE3” denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	100	V
Gate-source voltage			V_{GS}	± 10	
Continuous drain current	V_{GS} at 5 V	T_C = 25 °C	I_D	1.5	A
		T_C = 100 °C		0.93	
Pulsed drain current [a]			I_{DM}	12	
Linear derating factor				0.025	W/°C
Linear derating factor (PCB mount) [e]				0.017	
Single pulse avalanche energy [b]			E_{AS}	50	mJ
Avalanche current [a]			I_{AR}	1.5	A
Repetitive avalanche energy [a]			E_{AR}	0.31	mJ
Maximum power dissipation	T_C = 25 °C		P_D	3.1	W
Maximum power dissipation (PCB mount) [e]	T_A = 25 °C			2.0	
Peak diode recovery dv/dt [c]			dV/dt	5.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = 25 V, starting T_J = 25 °C, L = 25 mH, R_g = 25 Ω, I_{AS} = 1.5 A (see fig. 12)

c. $I_{SD} \leq 5.6$ A, dI/dt $\leq$ 75 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C

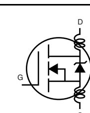
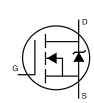
d. 1.6 mm from case

e. When mounted on 1" square PCB (FR-4 or G-10 material)

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) [a]	R_{thJA}	-	60	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.12	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0	-	2.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 10 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 5.0 V, I_D = 0.90 A [b]	-	-	0.54	Ω
		V_{GS} = 4.0 V, I_D = 0.75 A	-	-	0.76	
Forward transconductance	g_{fs}	V_{DS} = 25 V, I_D = 0.90 A	0.57	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	250	-	pF
Output capacitance	C_{oss}		-	80	-	
Reverse transfer capacitance	C_{rss}		-	15	-	
Total gate charge	Q_g	V_{GS} = 5.0 V, I_D = 5.6 A, V_{DS} = 80 V, see fig. 6 and 13 [b]	-	-	6.1	nC
Gate-source charge	Q_{gs}		-	-	2.6	
Gate-drain charge	Q_{gd}		-	-	3.3	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 5.6 A, R_g = 12 Ω, R_D = 8.4 Ω	-	9.3	-	ns
Rise time	t_r		-	47	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	t_f		-	18	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.0	-	nH
Internal source inductance	L_S		-	6.0	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	1.5	A
Pulsed diode forward current [a]	I_{SM}		-	-	12	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 1.5 A, V_{GS} = 0 V [b]	-	-	2.5	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 5.6 A, dI/dt = 100 A/μs [b]	-	110	130	ns
Body diode reverse recovery charge	Q_{rr}		-	0.50	0.65	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

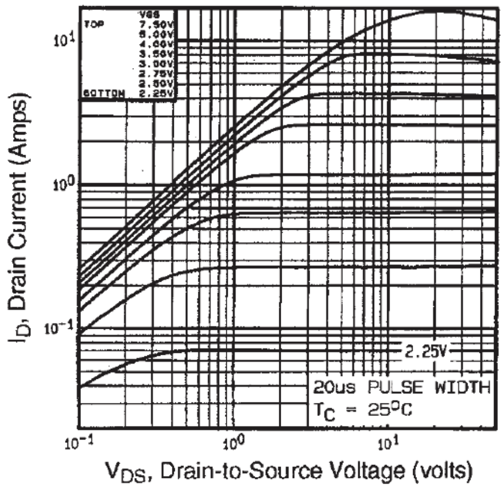


Fig. 1 - Typical Output Characteristics

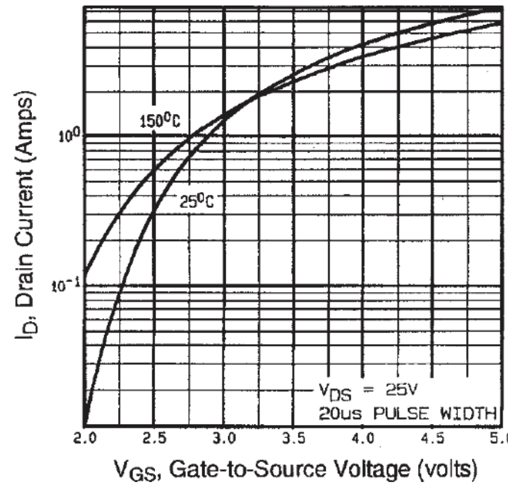


Fig. 3 - Typical Transfer Characteristics

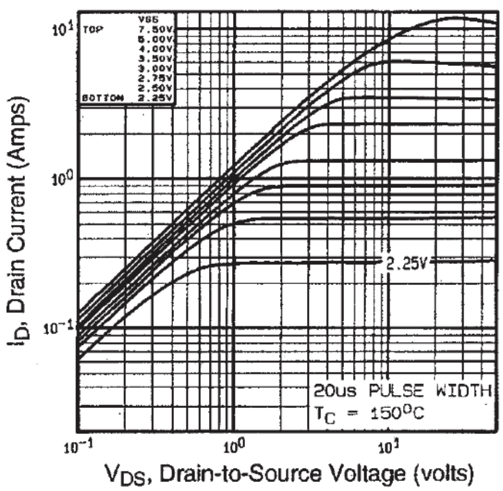


Fig. 2 - Typical Output Characteristics

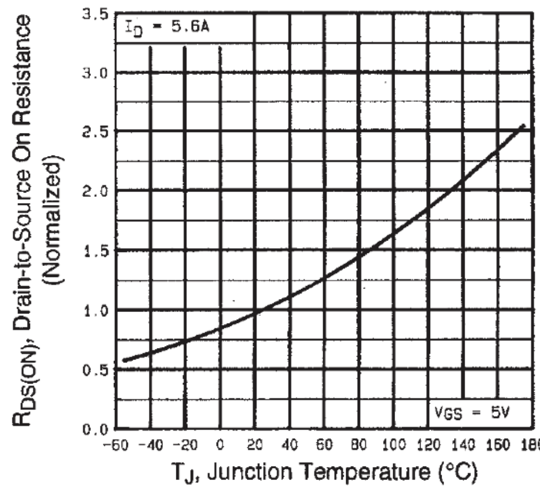


Fig. 4 - Normalized On-Resistance vs. Temperature

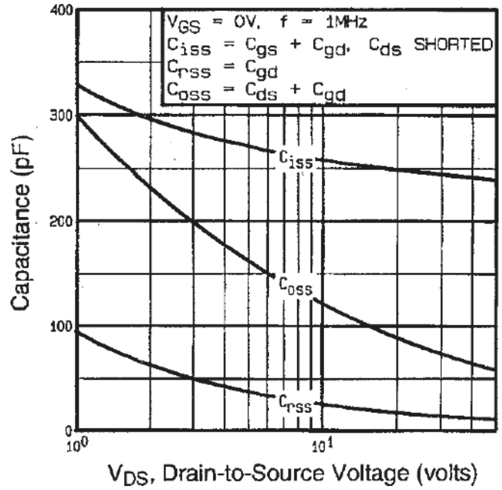


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

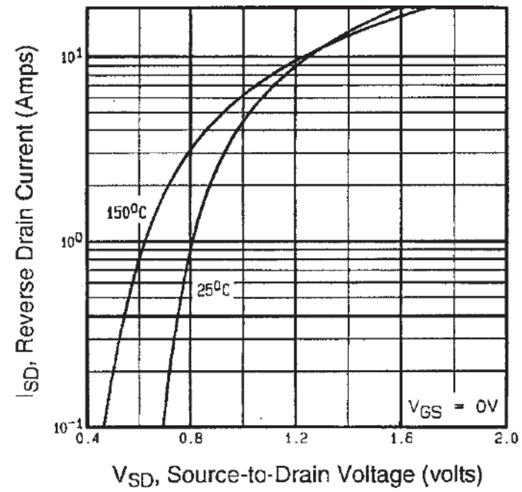


Fig. 7 - Typical Source-Drain Diode Forward Voltage

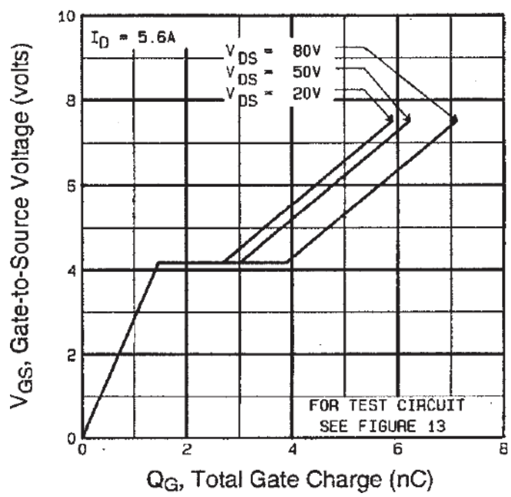


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

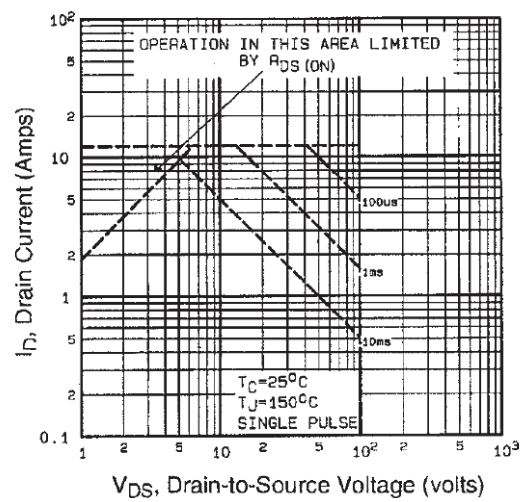


Fig. 8 - Maximum Safe Operating Area

For technical questions, contact: hvm@vishay.com

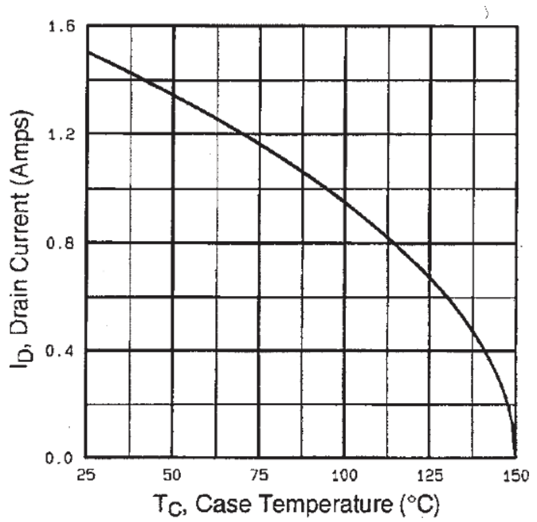


Fig. 9 - Maximum Drain Current vs. Case Temperature

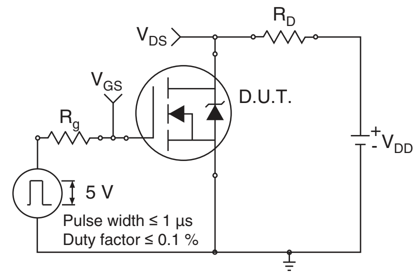


Fig. 10a - Switching Time Test Circuit

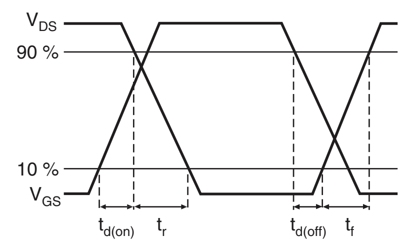


Fig. 10b - Switching Time Waveforms

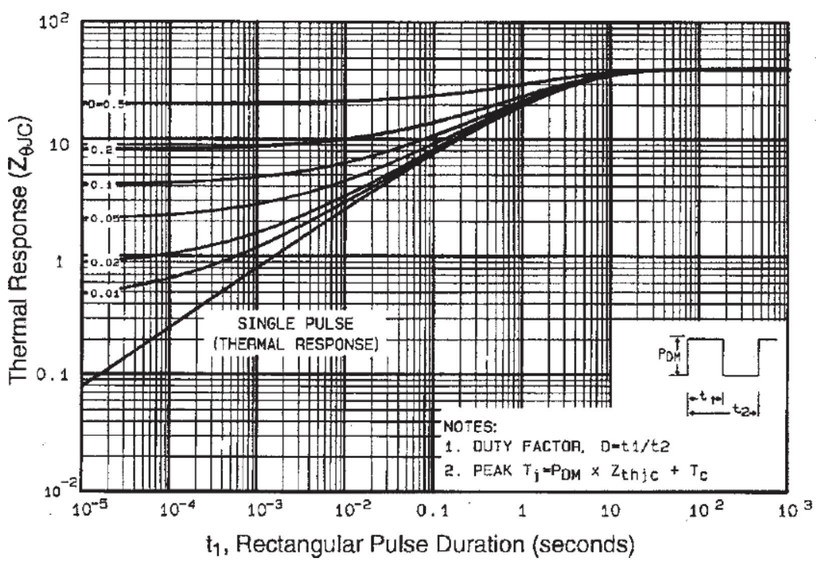


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

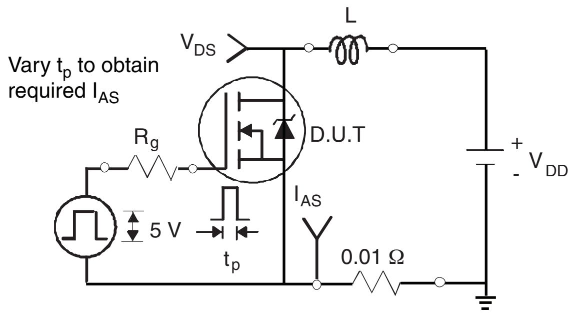


Fig. 12a - Unclamped Inductive Test Circuit

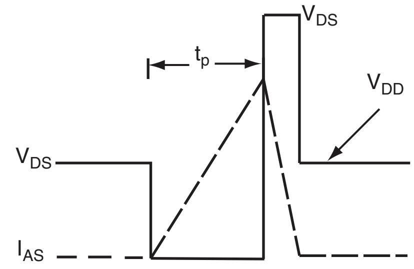


Fig. 12b - Unclamped Inductive Waveforms

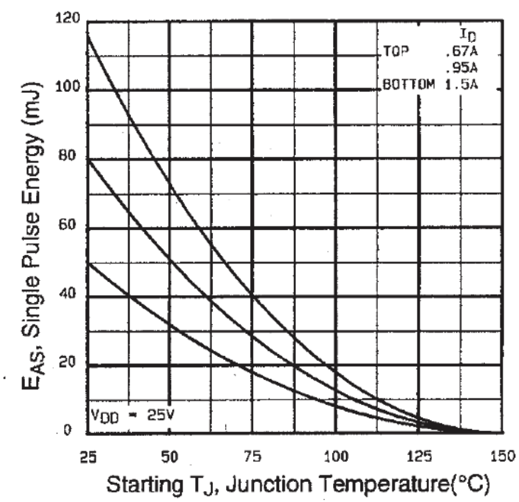


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

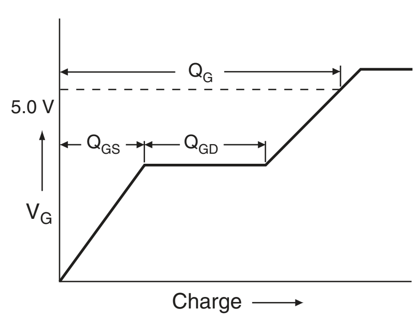


Fig. 13a - Basic Gate Charge Waveform

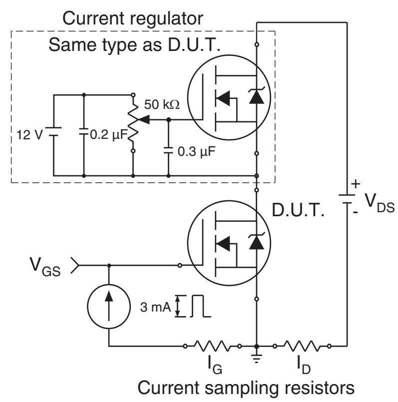
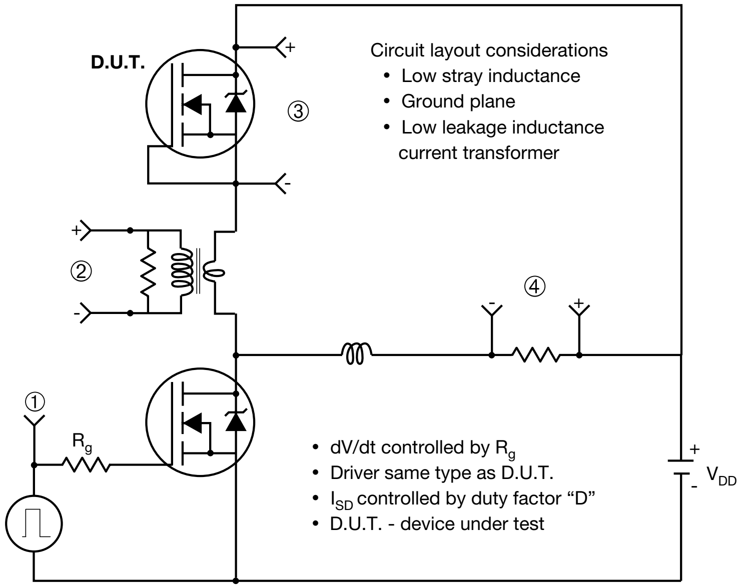
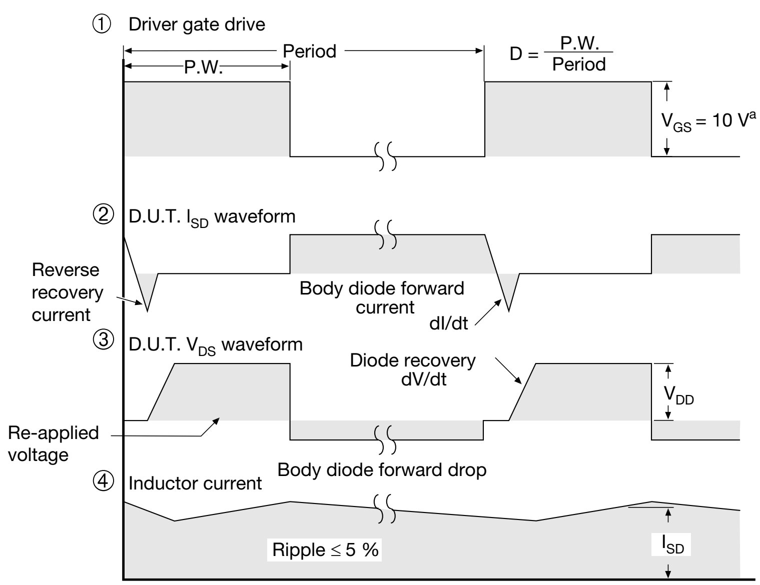


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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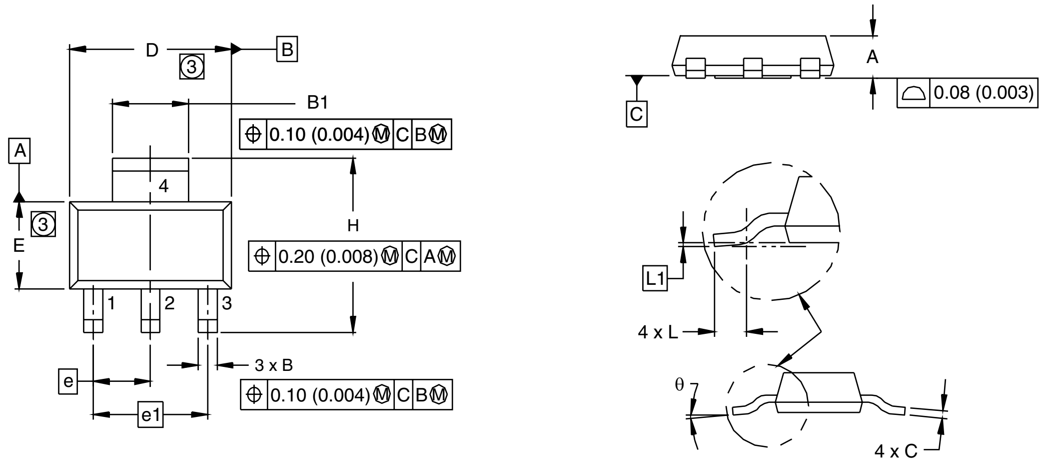
SOT-223 (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10'	-	10'
ECN: S-82109-Rev. A, 15-Sep-08 DWG: 5969				

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.

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