

## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.028
$Q_g$ (Max.) (nC)	95	
$Q_{gs}$ (nC)	27	
$Q_{gd}$ (nC)	46	
Configuration	Single	

### FEATURES

- Dynamic  $dV/dt$  Rating
- Isolated Central Mounting Hole
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

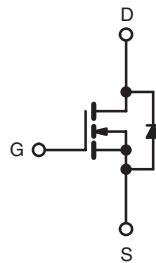
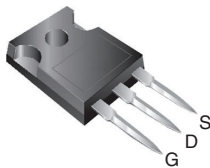

 Available  
**RoHS\***  
 COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

TO-247



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP044PbF
	SiHFP044-E3
SnPb	IRFP044
	SiHFP044

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	57
			$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	230	A
Linear Derating Factor			1.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	53	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	180	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	4.5	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw		10	
			1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 19\text{ }\mu\text{H}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 57\text{ A}$  (see fig. 12).
- $I_{SD} \leq 52\text{ A}$ ,  $dI/dt \leq 250\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.83	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		60	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.060	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 48\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 34\text{ A}^b$	-	-	0.028	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}$ , $I_D = 34\text{ A}^b$		17	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	2500	-	pF
Output Capacitance	$C_{oss}$			-	1200	-	
Reverse Transfer Capacitance	$C_{rss}$			-	200	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 52\text{ A}$ , $V_{DS} = 48\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	95	nC
Gate-Source Charge	$Q_{gs}$			-	-	27	
Gate-Drain Charge	$Q_{gd}$			-	-	46	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$ , $I_D = 52\text{ A}$ , $R_G = 9.1\text{ }\Omega$ , $R_D = 0.56$ , see fig. 10 <sup>b</sup>		-	19	-	ns
Rise Time	$t_r$			-	120	-	
Turn-Off Delay Time	$t_{d(off)}$			-	55	-	
Fall Time	$t_f$			-	86	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	$L_S$			-	13	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	57	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	230	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 57\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 52\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	140	300	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	1.2	2.8	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

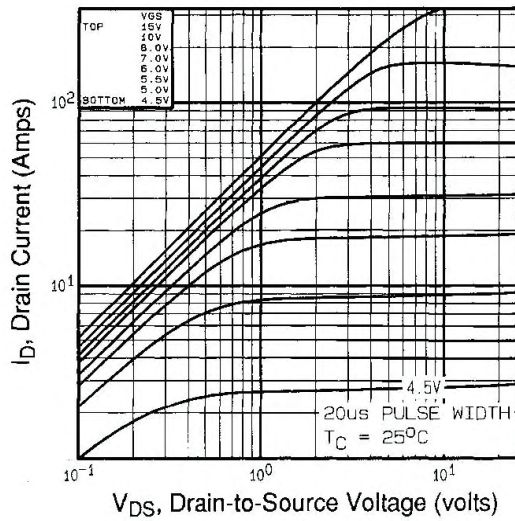


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

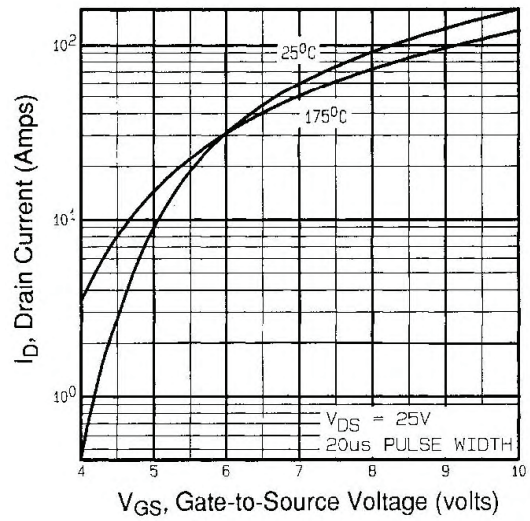


Fig. 3 - Typical Transfer Characteristics

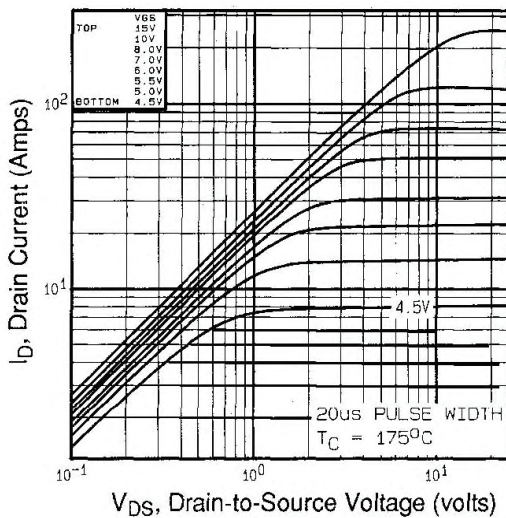


Fig. 2 - Typical Output Characteristics,  $T_C = 175^\circ\text{C}$

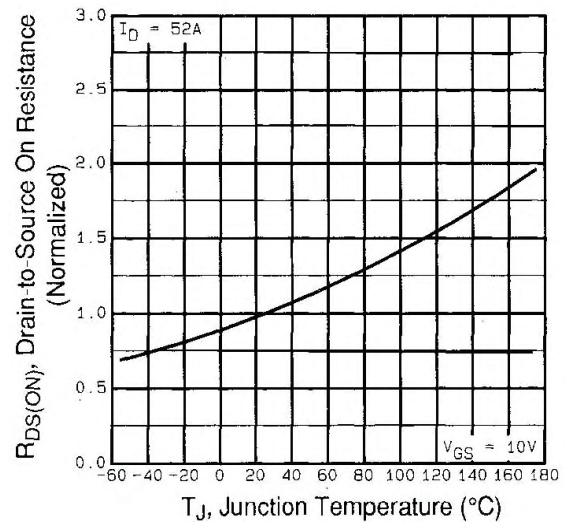


Fig. 4 - Normalized On-Resistance vs. Temperature

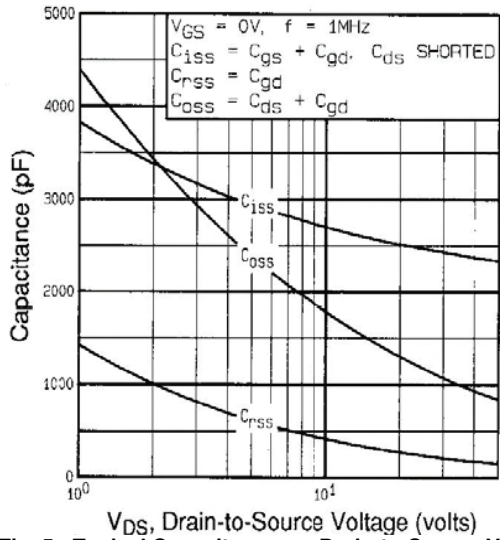


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

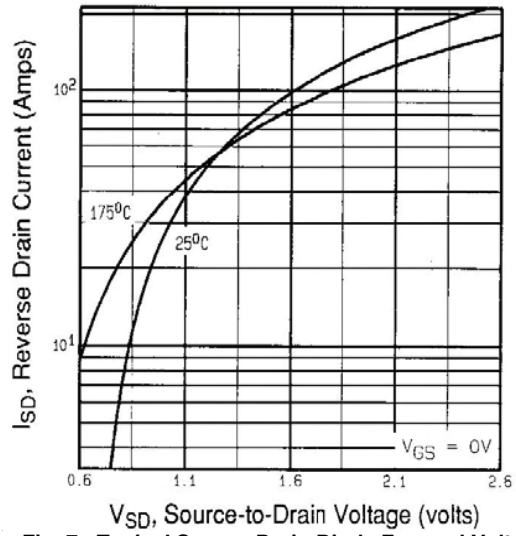


Fig. 7 - Typical Source-Drain Diode Forward Voltage

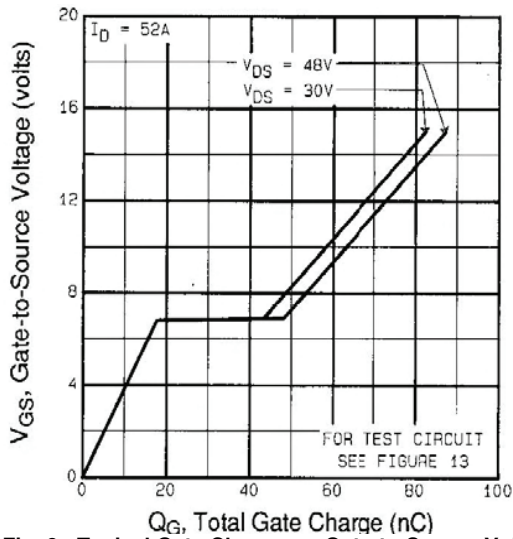


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

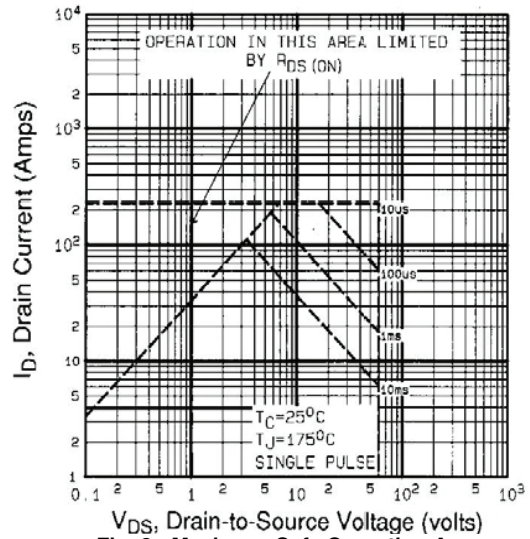


Fig. 8 - Maximum Safe Operating Area

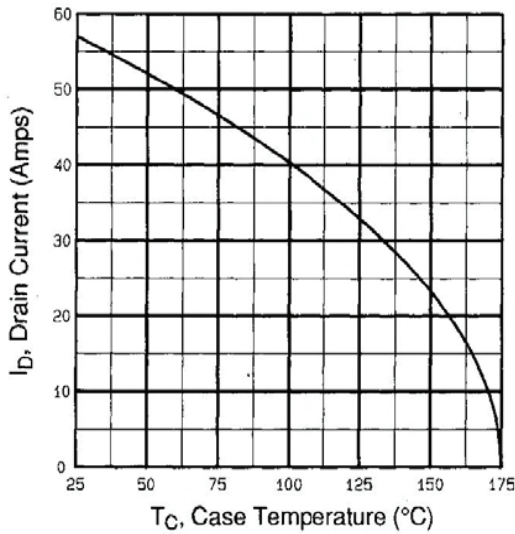


Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

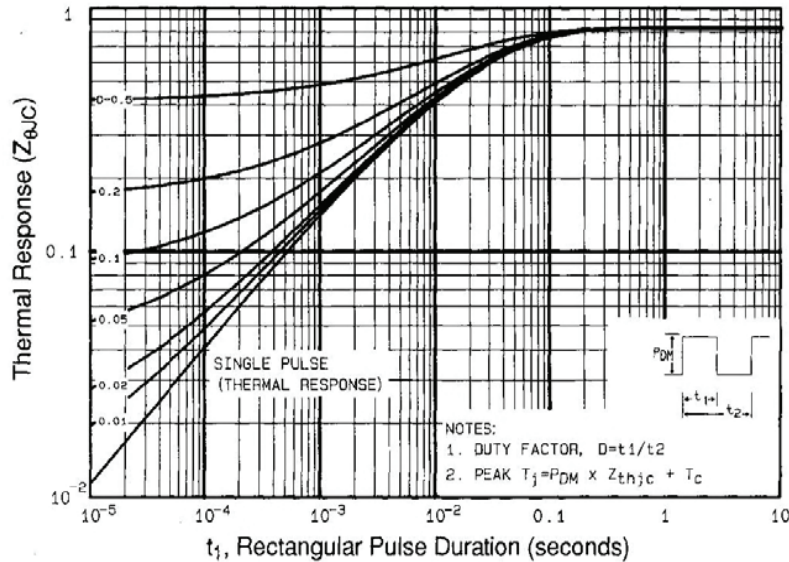


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

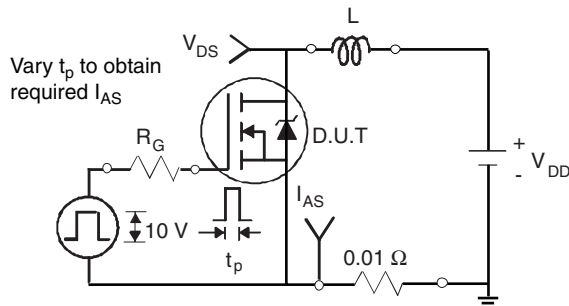


Fig. 12a - Unclamped Inductive Test Circuit

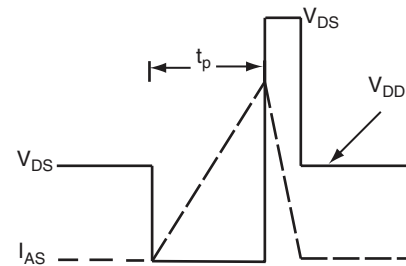


Fig. 12b - Unclamped Inductive Waveforms

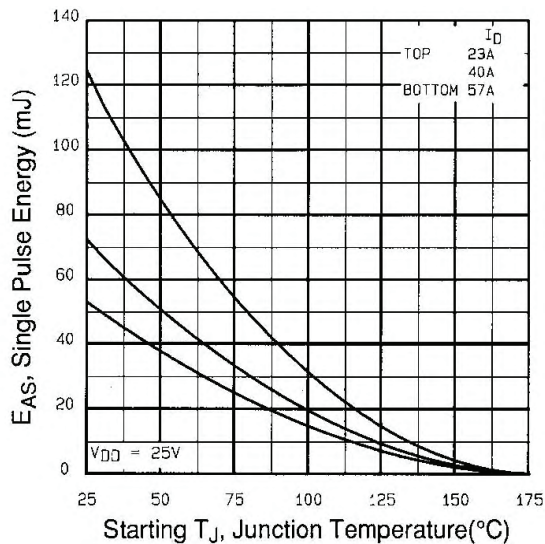


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

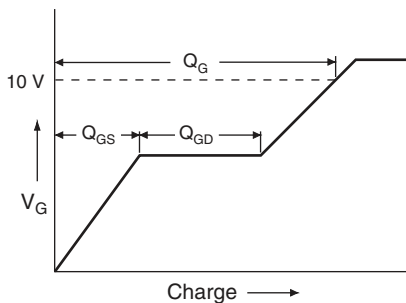


Fig. 13a - Basic Gate Charge Waveform

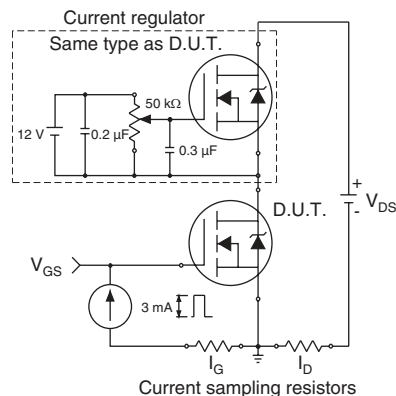
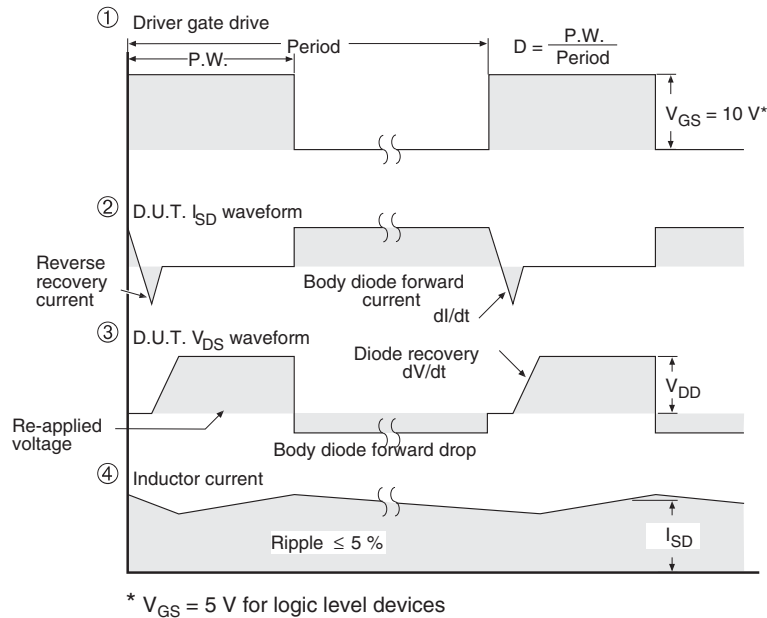
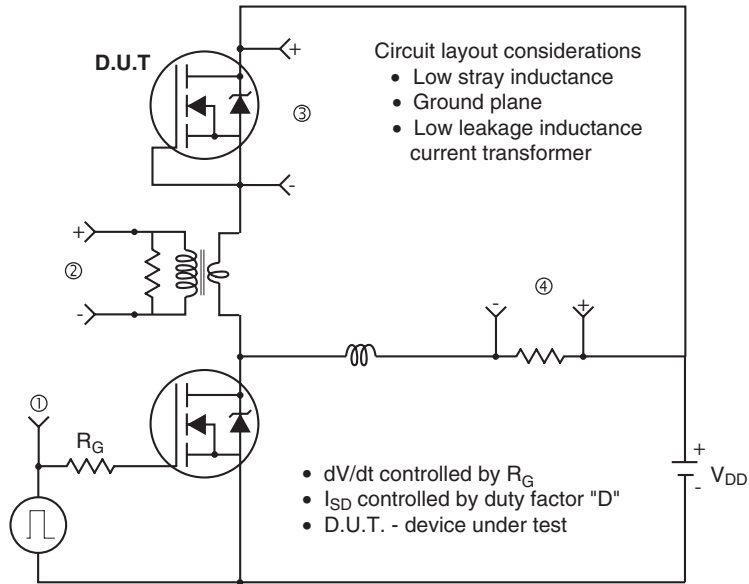


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit



**Fig. 14 - For N-Channel**

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