

Vishay Siliconix

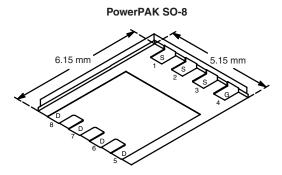
# N-Channel 40-V (D-S) Fast Switching MOSFET

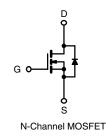
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω)	I <sub>D</sub> (A)		
40	0.0053 at V <sub>GS</sub> = 10 V	25		
	0.0066 at V <sub>GS</sub> = 4.5 V	23		

### FEATURES

- Halogen-free According to IEC 61249-2-21
  Available
- TrenchFET<sup>®</sup> Power MOSFET
- New Low Thermal Resistance PowerPAK<sup>®</sup> Package with Low 1.07 mm Profile







Bottom View Ordering Information: Si7476DP-T1-E3 (Lead (Pb)-free) Si7476DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	40		V
Gate-Source Voltage		V <sub>GS</sub>	± 20		v
Continuous Droin Current (T 150 °C)a	T <sub>A</sub> = 25 °C	I <sub>D</sub>	25	15	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		20	12	
Pulsed Drain Current		I <sub>DM</sub>	80		А
Continuous Source Current (Diode Conduction) <sup>a</sup>		۱ <sub>S</sub>	4.5	1.6	
Avalanche Current		I <sub>AS</sub>	60		
Avalanche Energy		E <sub>AS</sub>	180		mJ
Maximum Dawar Dissinction	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5.4	1.9	W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>		Ŭ	260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Marrier un lun stien te Amhientă	t ≤ 10 s	R <sub>thJA</sub>	18	23	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.0	1.3	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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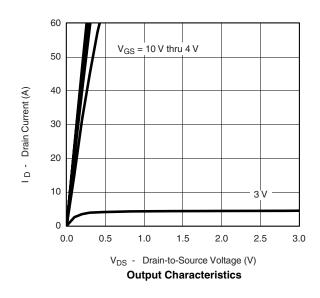
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static			•	•		
Gate Threshold Voltage V <sub>GS</sub>		$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.0		3.0	V
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zana Cata Malta na Duain Comunat	I <sub>DSS</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
Zero Gate Voltage Drain Current		$V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_{J}$ = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	40			А
Drain-Source On-State Resistance <sup>a</sup>	Б	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A		0.0042	0.0053	0
	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 23 \text{ A}$		0.0053	0.0066	Ω
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A		85		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{S} = 4.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.76	1.2	V
Dynamic <sup>b</sup>						
Total Gate Charge	Qg			118	177	nC
Gate-Source Charge	$\frac{Q_{gs}}{Q_{gd}}$ V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 25 \text{ A}$		25		
Gate-Drain Charge				21.2		
Gate Resistance	Rg			1.0		Ω
Turn-On Delay Time	t <sub>d(on)</sub>			30	45	
Rise Time	t <sub>r</sub>	$\label{eq:loss} \begin{array}{c} t_r & V_{DD} = 20 \ \text{V}, \ \text{R}_L = 20 \ \Omega \\ \hline t_{\text{d(off)}} & \text{I}_D \cong 1 \ \text{A}, \ \text{V}_{\text{GEN}} = 10 \ \text{V}, \ \text{R}_g = 6 \ \Omega \end{array}$		22	35	ns
Turn-Off Delay Time	t <sub>d(off)</sub>			130	195	
Fall Time	t <sub>f</sub>			55	85	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 4.5 A, dI/dt = 100 A/μs		45	70	

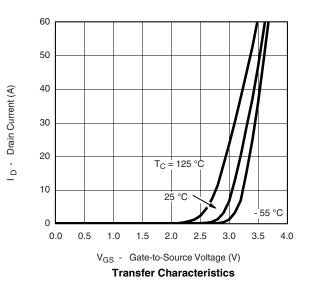
Notes:

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

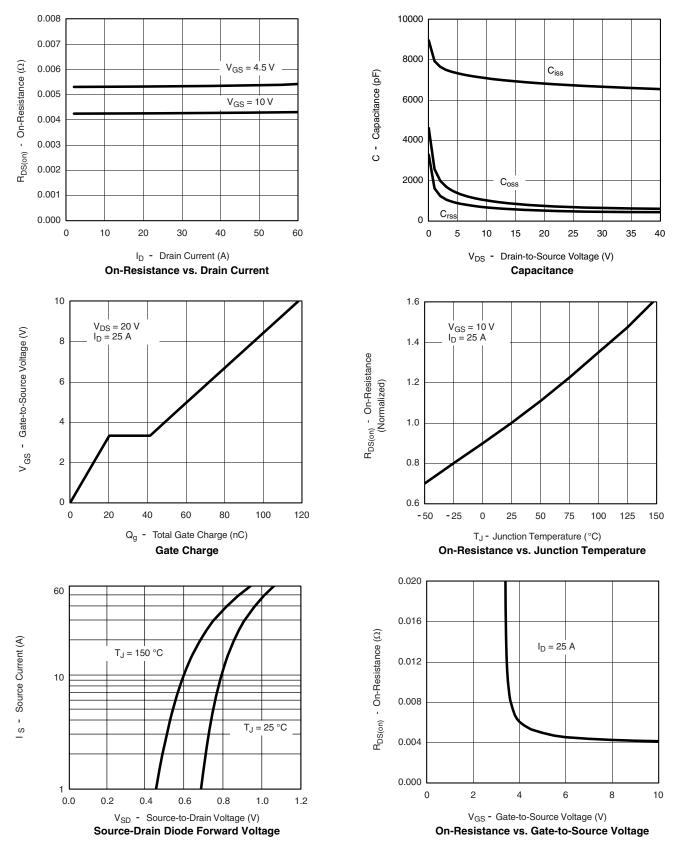






### Si7476DP Vishay Siliconix

### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



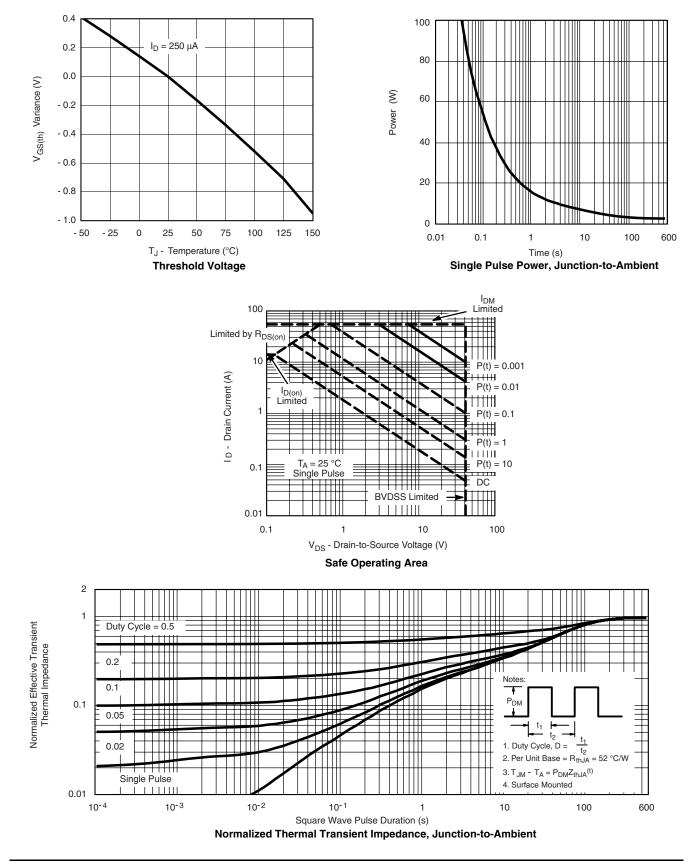
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# Si7476DP

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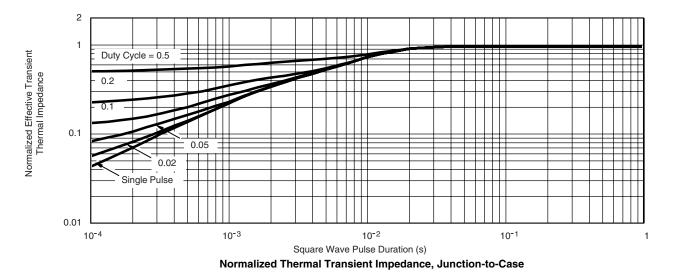
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Si7476DP Vishay Siliconix

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