1 pC Charge Injection, 100 pA Maximum Leakage, +5 V / +3 V, SPDT Analog Switch

DESCRIPTION

The DG9431E is a monolithic CMOS switch designed for precision signal switching. The 17 Ω low voltage part exhibits low charge injection over the full signal range, low leakage, low parasitic capacitance, and fast switching.

The DG9431E can switch both analog and digital signals. Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make switching is guaranteed.

The DG9431E offers 1 nW typical power consumption and 8 kV ESD (HBM), 1 kV ESD (CDM) tolerance. It is ideal for use in low voltage instruments and healthcare devices, fitting the circuits of low voltage ADC and DAC, sample and hold, analog front end gain control, and signal path switching. The DG9431E is available in 6-lead TSOP and 8-lead SOIC packages.

APPLICATIONS

- Automatic test equipment
- Process control and automation
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Sample-and-hold systems
- Relay replacements
- Battery powered systems

FEATURES

Pb-free Available

RoHS* Available

- 1 pC charge injection
- Guaranteed 100 pA max. switch on leakage at 25 °C
- 3.8 pF switch off and 7.8 pF switch on capacitances
- +2.7 V to +5 V single supply operation
- Low on-resistance - $R_{DS(on)}$: 17 Ω (typ.) at 5 V
- t_{ON}: 32 ns, t_{OFF}: 10 ns switching time
- Typical power consumption: 1 nW
- Over voltage tolerance on logic control IN pin
- TTL / CMOS compatible
- ESD (HBM): > 8000 V, ESD (CDM): >1000 V
- Latch-up current: > 300 mA (JESD78)
- Available in TSOP-6 and SOIC-8

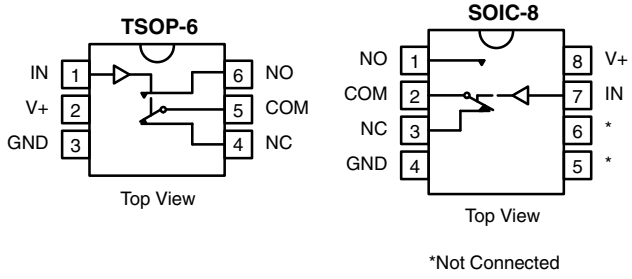
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

BENEFITS

- Low charge injection and leakage
- Low parasitic capacitance
- Fast switching speed
- High ESD tolerance

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
LOGIC	NC	NO
0	ON	OFF
1	OFF	ON

Note

- Logic “0” ≤ 0.8 V
  Logic “1” ≥ 2.4 V

ORDERING INFORMATION				
TEMP. RANGE	CONFIGURATION	PART NUMBER	PACKAGE	MINIUM ORDER / PACKAGING QUANTITY
-40 °C to +85 °C	DG9431E	6-pin TSOP	DG9431EDV-T1-GE3	Tape and reel 3000 units
		8-pin SOIC	DG9431EDY-T1-GE3	Tape and reel 2500 units
			DG9431EDY-GE3	Tube 500 units

ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
Reference V+ to GND		-0.3 to +6	V
IN, COM, NC, NO [a]		-0.3 to (V+ + 0.3)	
Continuous current (any terminal)		± 20	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 40	
ESD (HBM) (MIL-STD-883, method 3015)		> 8000	V
ESD (CDM) (ANSI / ESDA / JEDEC® JS-002)		> 1000	
Latch up current, per JESD78		300	mA
Storage temperature (D suffix)		-65 to +125	°C
Power dissipation (packages) [b]	8-pin narrow body SOIC [c]	400	mW
	6-pin TSOP [d]	570	

Notes

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.5 mW/°C above 75 °C.
d. Derate 7 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V [e]	TEMP. [a]	D SUFFIX -40 °C TO +85 °C			UNIT
				MIN. [c]	TYP. [b]	MAX. [c]	
Analog Switch							
Analog signal range [d]	V_{ANALOG}		Full	0	-	3	V
Drain-source on–resistance	$R_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V, V+ = 2.7 V, I_{COM} = 5 mA	Room	-	35	50	Ω
			Full	-	-	65	
$R_{DS(on)}$ match [d]	$\Delta R_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V	Room	-	0.4	2	
$R_{DS(on)}$ flatness [f]	$R_{DS(on)}$ flatness	V_{NO} or V_{NC} = 1 V and 2 V	Room	-	4	8	
NO or NC off leakage current [g]	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V / 2 V, V_{COM} = 2 V / 1 V	Room	-100	5	100	pA
			Full	-5000	-	5000	
COM off leakage current [g]	$I_{COM(off)}$	V_{COM} = 1 V / 2 V, V_{NO} or V_{NC} = 2 V / 1 V	Room	-100	5	100	
			Full	-5000	-	5000	
Channel-on leakage current [g]	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V / 2 V	Room	-200	5	200	
			Full	-10 000	-	10 000	
Digital Control							
Input current	I_{INL} or I_{INH}		Full	-	0.001	-	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 1.5 V	Room	-	43	120	ns
			Full	-	-	200	
Turn-Off Time	t_{OFF}		Room		16	50	
			Full	-	-	120	
Break-before-make time	t_d		Room	3	26	-	
Charge injection	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-	-0.28	-	pC
Off-isolation	O_{IRR}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-80	-	dB
Crosstalk	X_{TALK}		Room	-	-108	-	
Source off capacitance	$C_{S(off)}$	f = 1 MHz	Room	-	4	-	pF
Channel-on capacitance	$C_{D(on)}$		Room	-	8	-	
Power Supply							
Power supply range	V+			2.7	-	5.5	V
Power supply current	I+	V+ = 3.3 V, V_{IN} = 0 V or 3.3 V		-	0.0003	1	µA

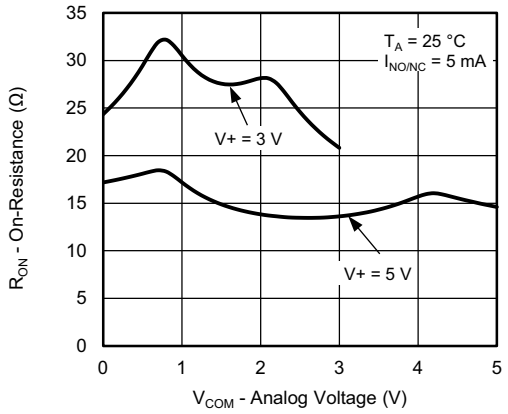
SPECIFICATIONS (V+ = 5 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V [e]	**TEMP.** [a]	**D SUFFIX** -40 °C to +85 °C			**UNIT**
				MIN. [c]	**TYP.** [b]	**MAX.** [c]	
Analog Switch							
Analog signal range [d]	V_{ANALOG}		Full	0	-	5	V
Drain-source on–resistance	$R_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V, V+ = 4.5 V, I_{COM} = 5 mA	Room	-	17	25	Ω
			Full	-	-	35	
$R_{DS(on)}$ match [d]	$\Delta R_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V	Room	-	0.4	2	
$R_{DS(on)}$ flatness [f]	$R_{DS(on)}$ flatness	V_{NO} or V_{NC} = 1 V, 2 V, and 3 V	Room	-	3.5	6	
NO or NC off leakage current	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V / 4 V, V_{COM} = 4 V / 1 V	Room	-100	10	100	pA
			Full	-5000	-	5000	
COM off leakage current	$I_{COM(off)}$	V_{COM} = 1 V / 4 V, V_{NO} or V_{NC} = 4 V / 1 V	Room	-100	10	100	
			Full	-5000	-	5000	
Channel-on leakage current	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V / 4 V	Room	-200	-	200	
			Full	-10 000	-	10 000	
Digital Control							
Input current	I_{INL} or I_{INH}		Full	-	0.001	-	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 3 V	Room	-	32	75	ns
			Full	-	-	150	
Turn-off time	t_{OFF}		Room	-	10	50	
			Full	-	-	100	
Break-before-make time	t_d		Room	3	22	-	
Charge injection	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-	-0.78	-	pC
Off-isolation	O_{IRR}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-80	-	dB
Crosstalk	X_{TALK}		Room	-	-108	-	
NC and NO capacitance	$C_{(off)}$	f = 1 MHz	Room	-	3.8	-	pF
Channel-on capacitance	$C_{D(on)}$		Room	-	7.8	-	
Power Supply							
Power supply range	V+			2.7	-	5.5	V
Power supply current	I+	V+ = 5.5 V, V_{IN} = 0 V or 5.5 V		-	0.0004	1	µA

Notes

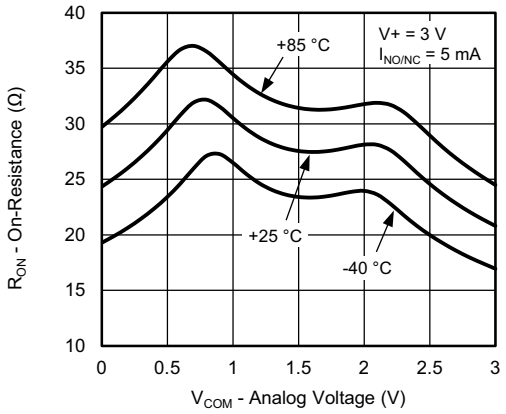
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.
g. Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

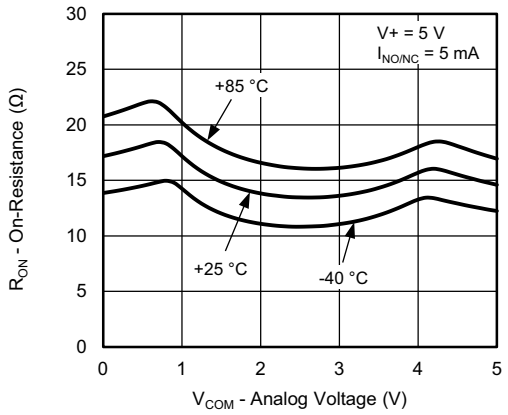
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



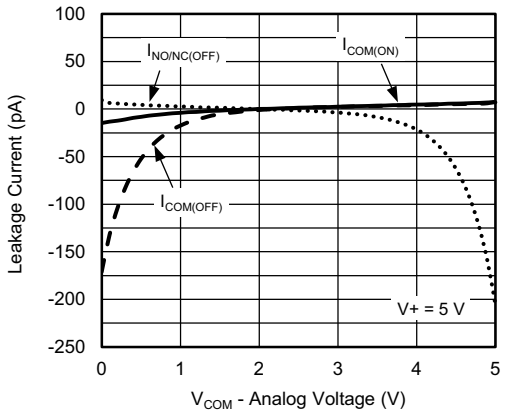
On-Resistance vs. Analog Voltage



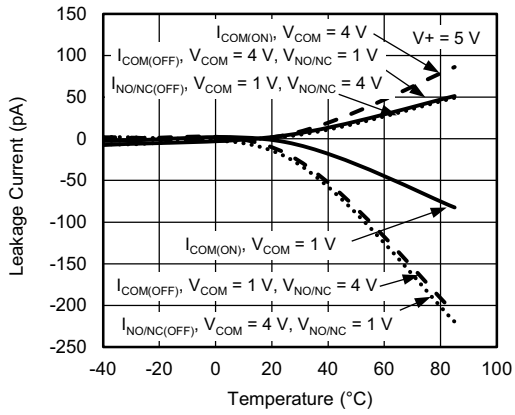
On-Resistance vs. Analog Voltage



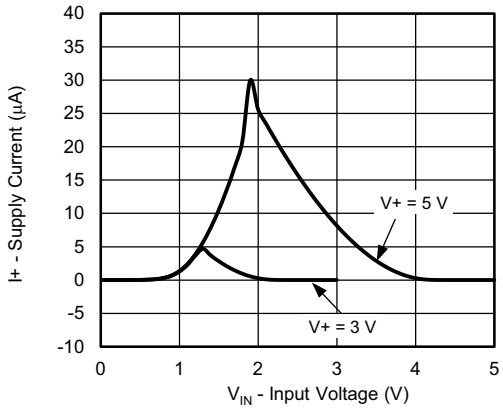
On-Resistance vs. Analog Voltage



Leakage Current vs. Analog Voltage

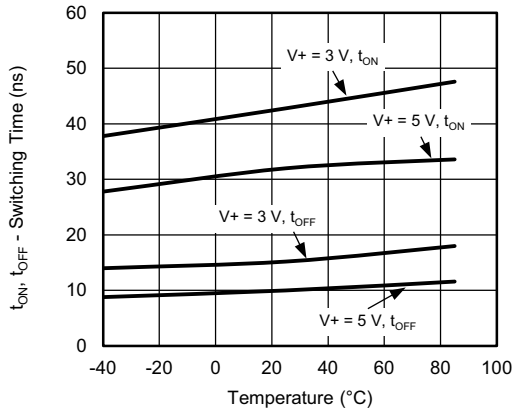


Leakage Current vs. Temperature

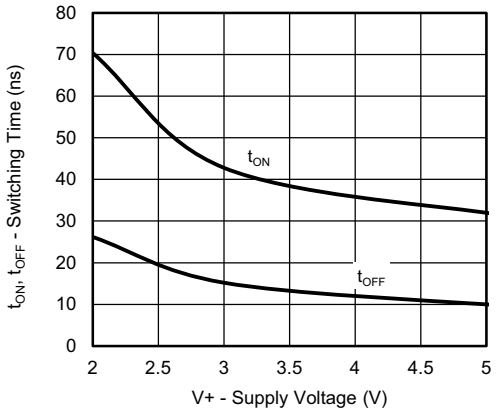


Supply Current vs. Input Voltage

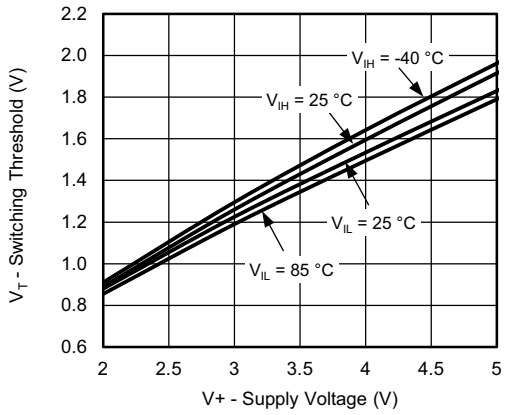
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



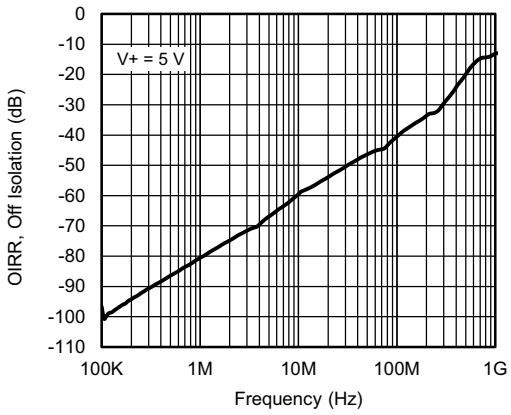
Switching Time vs. Temperature



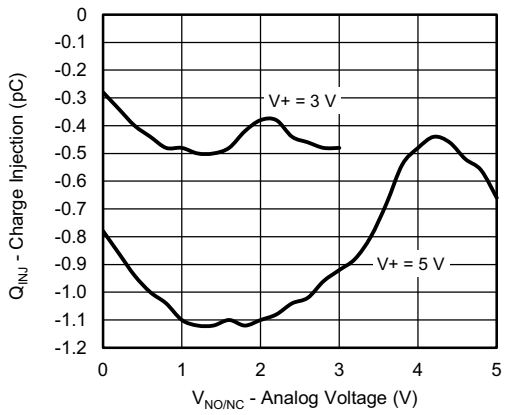
Switching Time vs. Supply Voltage



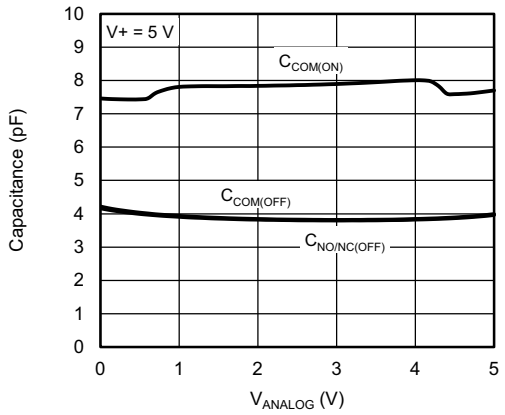
Switching Threshold vs. Supply Voltage



OIRR, Off Isolation vs. Frequency

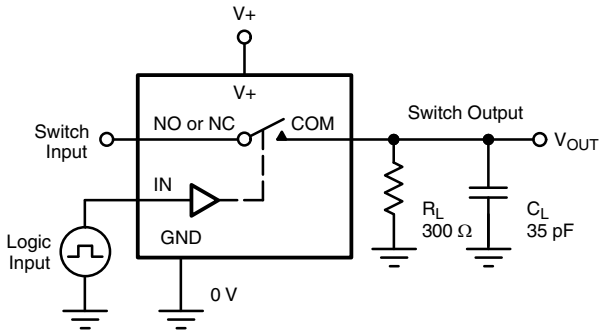


Charge Injection vs. Analog Voltage



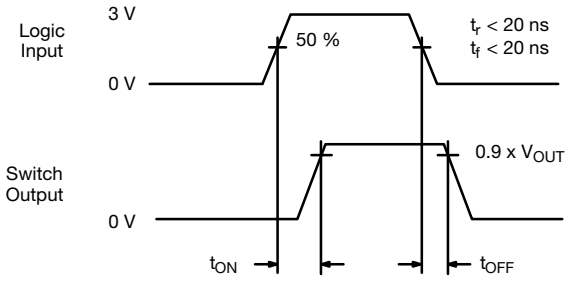
Capacitance

TEST CIRCUITS



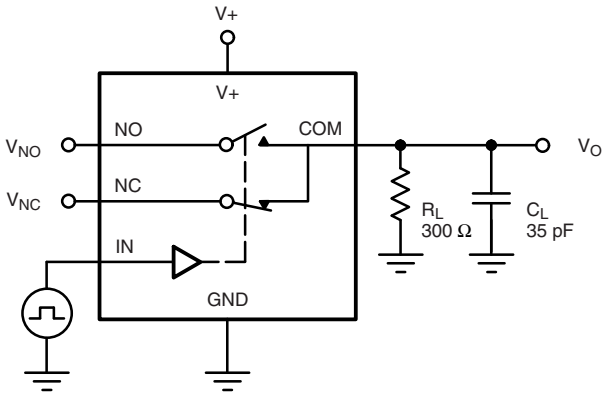
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

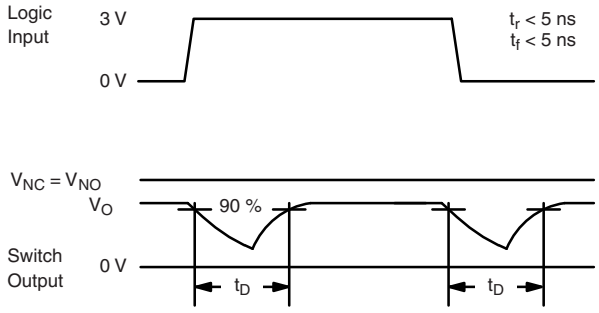
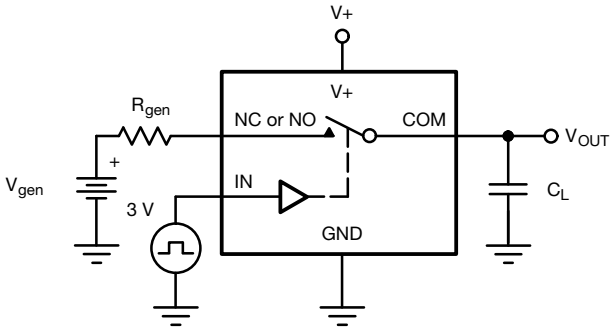
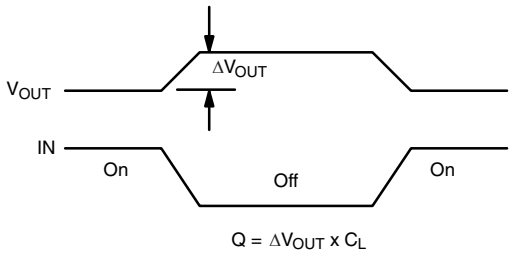


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

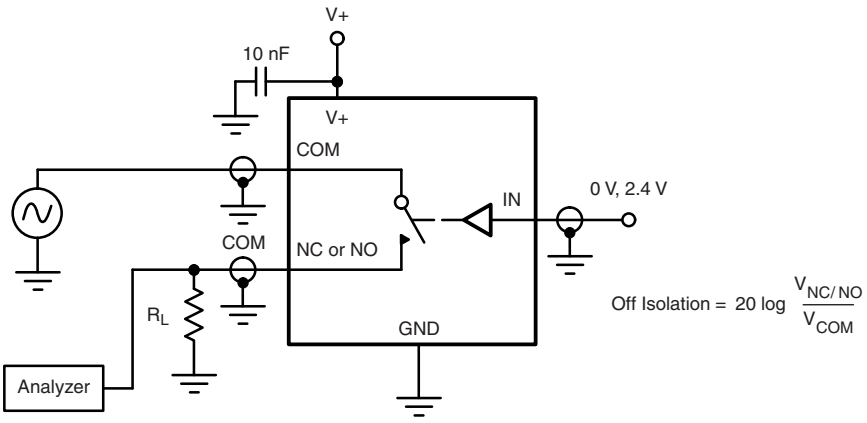


Figure 4. Off-Isolation

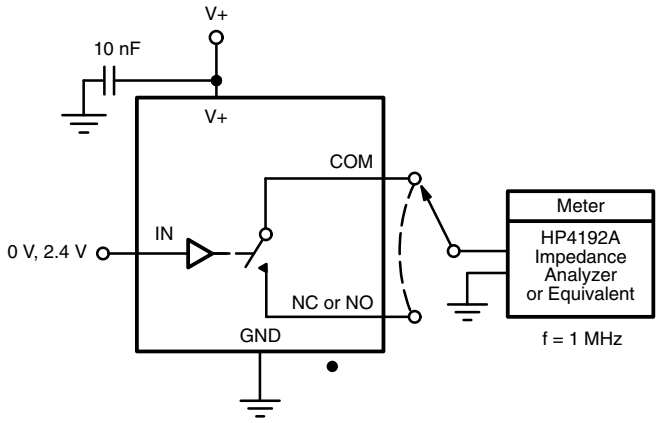
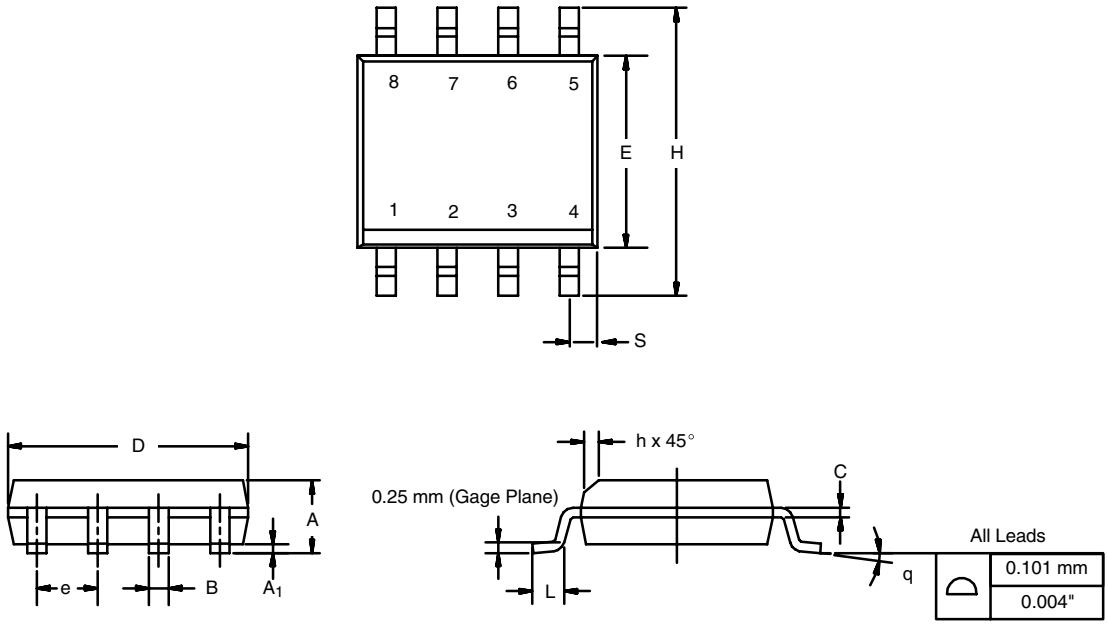


Figure 5. Channel Off/On Capacitance

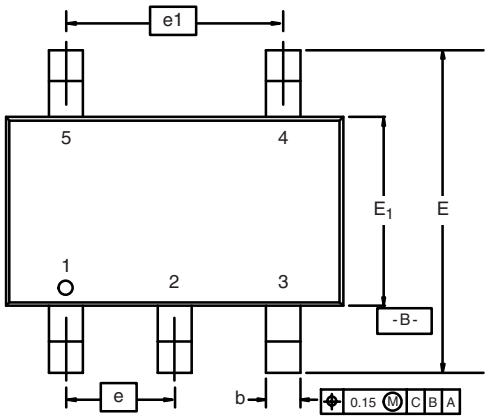
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76459.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012

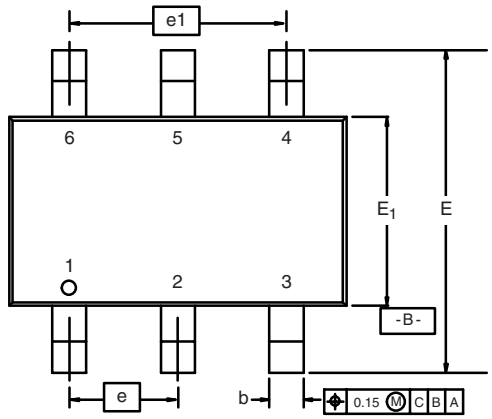


DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

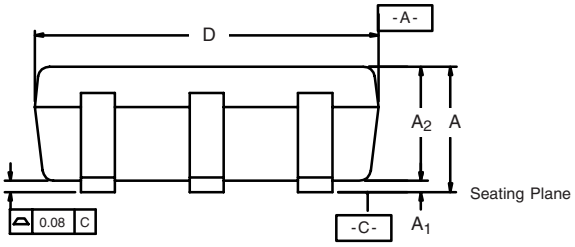
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

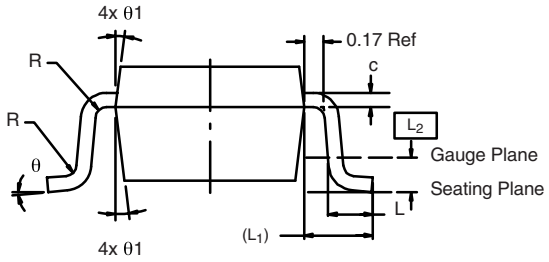


5-LEAD TSOP



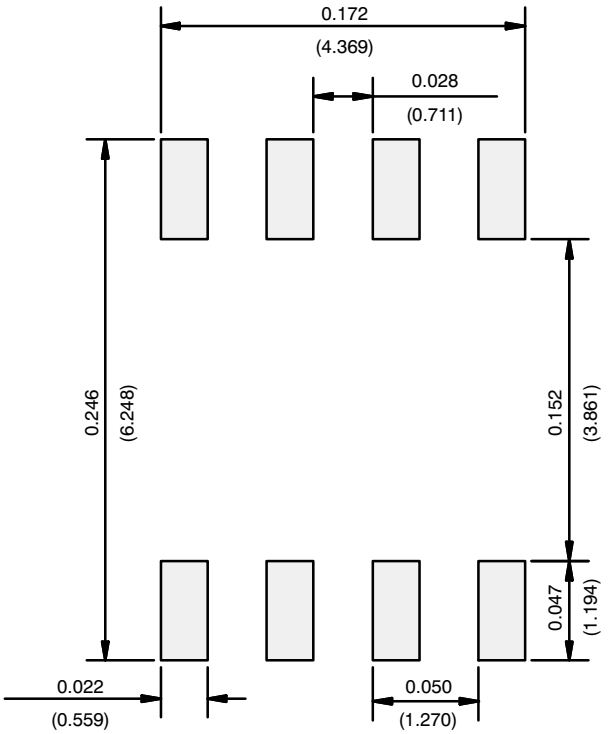
6-LEAD TSOP





Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
$θ_1$	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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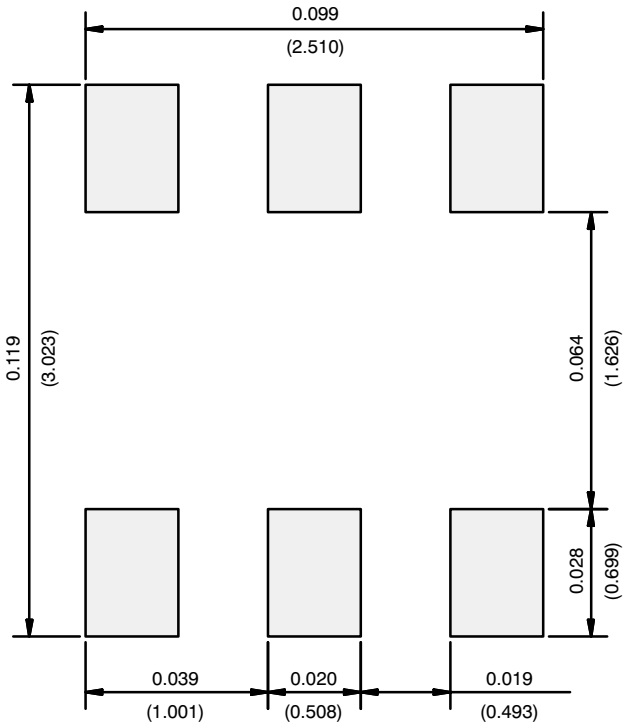
RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

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