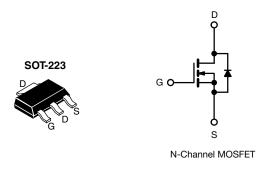
Vishay Siliconix



Power MOSFET



Marking code: FA

PRODUCT SUMMA	RY	
V _{DS} (V)	60	
R _{DS(on)} (Ω)	$V_{GS} = 10 V$	0.20
Q _g max. (nC)	11	
Q _{gs} (nC)	3.1	
Q _{gd} (nC)	5.8	1
Configuration	Sing	le

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Fast switching
- Ease of paralleling
- Simple drive requirements



 Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Lead (Pb)-free and halogen-free	SiHFL014TR-GE3 ^a
Lead (PD)-free and halogen-free	IRFL014TRPbF-BE3 ^{a, b}
Lead (Pb)-free	IRFL014TRPbF ^a

Notes

a. See device orientation

b. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS (T _C	, -					
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	60	v	
Gate-source voltage			V _{GS}	± 20		
Continuous drain current	V _{GS} at 10 V	$T_{C} = 25 \text{ °C}$ $T_{C} = 100 \text{ °C}$	I _D	2.7		
	VGS AL TO V			1.7	А	
Pulsed drain current ^a	I _{DM} 22			22	\neg	
Linear derating factor			0.025	W/°C		
Linear derating factor (PCB mount) ^e			0.017			
Single pulse avalanche energy ^b			E _{AS}	100	mJ	
Maximum power dissipation $T_{C} = 25 \text{ °C}$		Р	3.1	14/		
Maximum power dissipation (PCB mount) e	T _A = 25 °C		PD	2.0	W	
Peak diode recovery dv/dt ^c		dV/dt	4.5	V/ns		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	- °C		
Soldering recommendations (peak temperature) d			300			

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = 25 V, starting T_J = 25 °C, L = 16 mH, R_g = 25 Ω , I_{AS} = 2.7 A (see fig. 12)

c. $I_{SD} \le 10$ A, dI/dt ≤ 90 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C

d. 1.6 mm from case

e. When mounted on 1" square PCB (FR-4 or G-10 material)

S21-0322-Rev. G, 05-Apr-2021



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THERMAL RESISTANCE RAT	INGS				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	-	60	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} :	= 0 V, I _D = 250 μA	60	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 1 mA	-	0.068	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μΑ	2.0	-	4.0	V
Gate-source leakage	I _{GSS}		V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}		= 60 V, V _{GS} = 0 V , V _{GS} = 0 V, T _J = 125 °C	-	-	25 250	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	$I_{\rm D} = 1.6 {\rm A}^{\rm b}$	-	-	0.20	Ω
Forward transconductance	g _{fs}	$V_{DS} = 25 \text{ V}, \text{ I}_{D} = 1.6 \text{ A}$		1.9	-	-	S
Dynamic	010			1	I.	I.	
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V,		-	300	-	pF
Output capacitance	C _{oss}			-	160	-	
Reverse transfer capacitance	C _{rss}	f = 1	.0 MHz, see fig. 5	-	29	-	
Total gate charge	Qq			-	-	11	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$I_D = 10 \text{ A}, V_{DS} = 48 \text{ V},$ see fig. 6 and 13 ^b	-	-	3.1	nC
Gate-drain charge	Q _{gd}		see lig. 0 and 15	-	-	5.8	
Turn-on delay time	t _{d(on)}		·	-	10	-	
Rise time	t _r	VDD	= 30 V, I _D = 10 A,	-	50	-	
Turn-off delay time	t _{d(off)}	$R_g = 24 \Omega$,	$R_D = 2.7 \Omega$, see fig. 10 ^b	-	13	-	ns
Fall time	t _f			-	19	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from - 4.0 -		nH			
Internal source inductance	L _S	package and die contact	center of	-	6.0	-	
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	MOSFET symbol showing the		-	-	2.7	_
Pulsed diode forward current ^a	I _{SM}	p - n junction		-	-	22	A
Body diode voltage	V _{SD}	T _J = 25 °C	, I _S = 2.7 A, V _{GS} = 0 V ^b	-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _ 05 °O I	- 10 A dl/dt . 100 A/u- h	-	70	140	ns
Body diode reverse recovery charge	Q _{rr}	$I_{\rm J} = 25 {}^{-}{\rm C}, I_{\rm F}$	= 10 A, dl/dt = 100 A/µs ^b	-	0.20	0.40	μC
Forward turn-on time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn	on is dor	ninated b	v Ls and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %

2



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

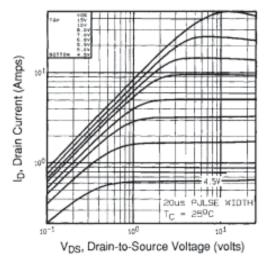


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

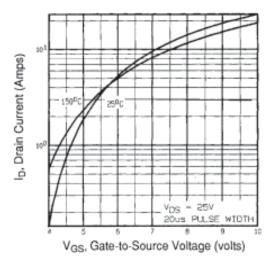


Fig. 3 - Typical Transfer Characteristics

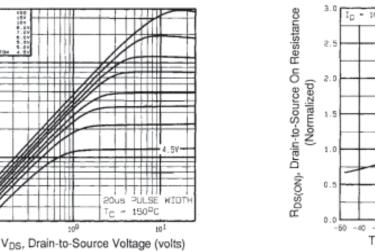


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

100

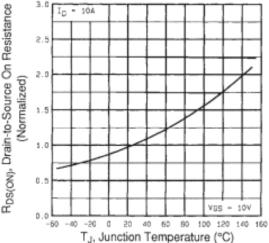


Fig. 4 - Normalized On-Resistance vs. Temperature

ID, Drain Current (Amps)

10

 10^{-3}



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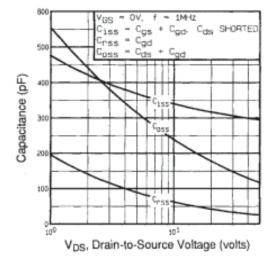


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

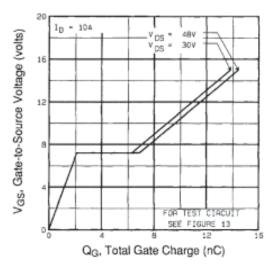


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

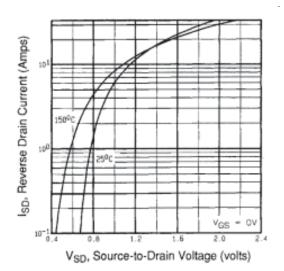


Fig. 7 - Typical Source-Drain Diode Forward Voltage

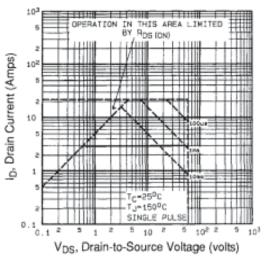


Fig. 8 - Maximum Safe Operating Area



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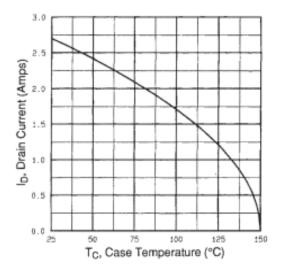


Fig. 9 - Maximum Drain Current vs. Case Temperature

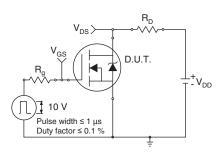


Fig. 10a -Switching Time Test Circuit

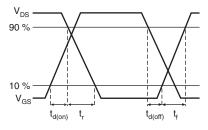


Fig. 10b -Switching Time Waveforms

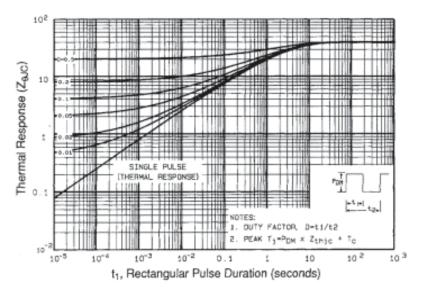


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



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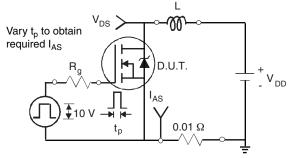


Fig. 12a - Unclamped Inductive Test Circuit

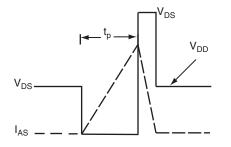


Fig. 12b - Unclamped Inductive Waveforms

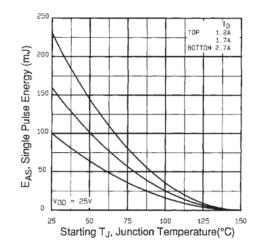


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

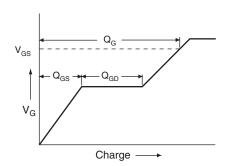


Fig. 13a - Basic Gate Charge Waveform

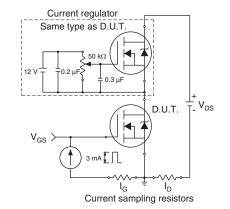


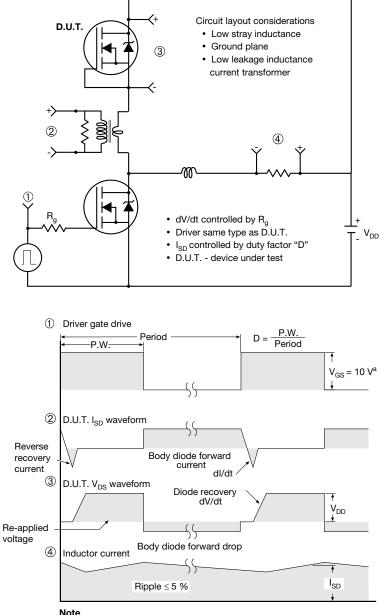
Fig. 13b - Gate Charge Test Circuit

6





Peak Diode Recovery dV/dt Test Circuit



a. $V_{GS} = 5$ V for logic level devices

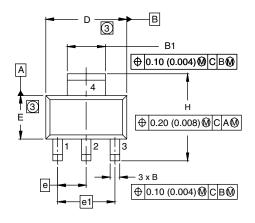
Fig. 12 - For N-Channel

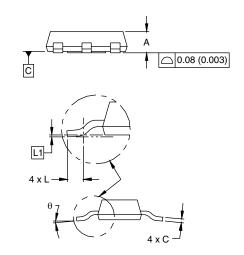
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SOT-223 (HIGH VOLTAGE)





	MILLI	METERS	INCHES			
DIM.	MIN.	MAX.	MIN.	MAX.		
А	1.55	1.80	0.061	0.071		
В	0.65	0.85	0.026	0.033		
B1	2.95	3.15	0.116	0.124		
С	0.25	0.35	0.010	0.014		
D	6.30	6.70	0.248	0.264		
E	3.30	3.70	0.130	0.146		
е	2.30	2.30 BSC		0.0905 BSC		
e1	4.60	BSC	0.181 BSC			
Н	6.71	7.29	0.264	0.287		
L	0.91	-	0.036	-		
L1	L1 0.061 BSC		0.002	4 BSC		
θ	-	10'	-	10'		

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Dimensions are shown in millimeters (inches).

3. Dimension do not include mold flash.

4. Outline conforms to JEDEC outline TO-261AA.



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