

## Dual N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) MAX.	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
Channel-1 and Channel-2	30	0.0115 at V <sub>GS</sub> = 10 V	30 <sup>a</sup>	4.5 nC
		0.0153 at V <sub>GS</sub> = 4.5 V	27.5	

### FEATURES

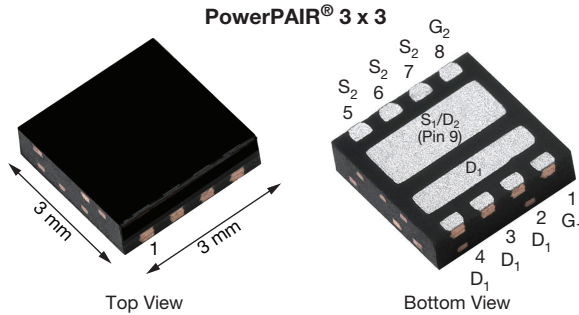
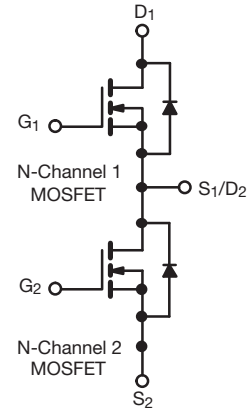
- PowerPAIR® optimizes high-side and low-side MOSFETs for synchronous buck converters
- TrenchFET® Gen IV power MOSFETs
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous buck
  - Battery charging
  - Computer system power
  - Graphic cards
- POL



### Ordering Information:

SiZ342DT-T1-GE3 (lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
PARAMETER	CHANNEL-1 AND CHANNEL-2			UNIT
	SYMBOL	LIMIT		
Drain-Source Voltage	V <sub>DS</sub>	30		V
Gate-Source Voltage	V <sub>GS</sub>	+20 / -16		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	30 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	26.5	
		T <sub>A</sub> = 25 °C	15.6 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	12.4 <sup>b, c</sup>	
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	100		
Continuous Source Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	13.9	
		T <sub>A</sub> = 25 °C	3.1 <sup>b, c</sup>	
Avalanche Current	I <sub>AS</sub>	10		
Single Pulse Avalanche Energy	E <sub>AS</sub>	5		mJ
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	16.7	W
		T <sub>C</sub> = 70 °C	10.7	
		T <sub>A</sub> = 25 °C	3.7 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	2.4 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR 3 x 3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



THERMAL RESISTANCE RATINGS						
PARAMETER		CHANNEL-1 AND CHANNEL-2				
		SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient <sup>a, b</sup>	t ≤ 10 s	R <sub>thJA</sub>	27	34	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	6	7.5		

**Notes**

- a. Surface mounted on 1" x 1" FR4 board.
- b. Maximum under steady state conditions is 69 °C/W.

**SPECIFICATIONS** (T<sub>J</sub> = 25 °C, unless otherwise noted)

PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	20	-	mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-5.6	-	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.2	-	2.4	V
Gate Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20 V/ -16 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	5	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ 5 V, V <sub>GS</sub> = 10 V	10	-	-	A
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14.4 A	-	0.0084	0.0115	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 13 A	-	0.0111	0.0153	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 14.4 A	-	37	-	S
<b>Dynamic <sup>a</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	650	-	pF
Output Capacitance	C <sub>oss</sub>		-	236	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	20	-	
C <sub>rss</sub> / C <sub>iss</sub> Ratio			0.03	-	0.06	-
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14.4 A	-	10	20	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14.4 A	-	4.5	9	
Gate-Drain Charge	Q <sub>gd</sub>		-	2.1	-	
Output Charge	Q <sub>oss</sub>		-	0.7	-	
			-	6.6	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.3	1.4	2.8	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	15	23	ns
Rise Time	t <sub>r</sub>		-	50	75	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	16	24	
Fall Time	t <sub>f</sub>		-	10	20	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	8	16	
Rise Time	t <sub>r</sub>		-	15	23	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	17	26	
Fall Time	t <sub>f</sub>		-	7	14	



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	13.9	A
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>		-	-	100	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	20	35	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	10	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>		-	12.5	-	ns
Reverse Recovery Rise Time	t <sub>b</sub>		-	7.5	-	

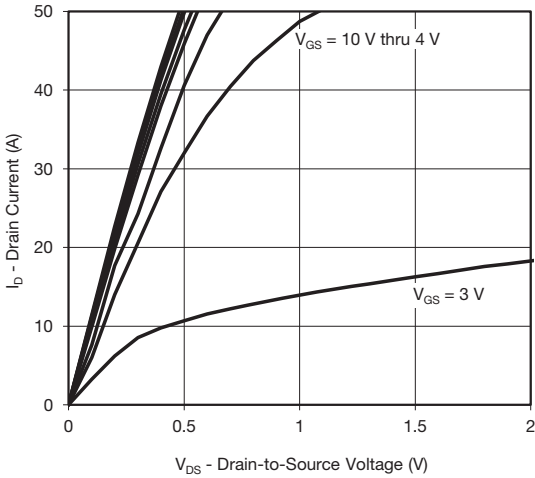
**Notes**

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

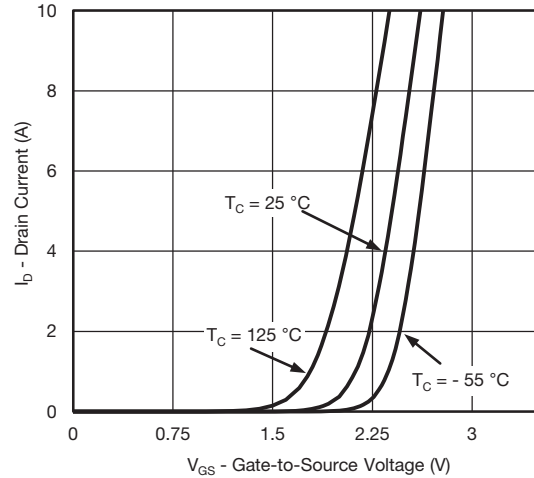
*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



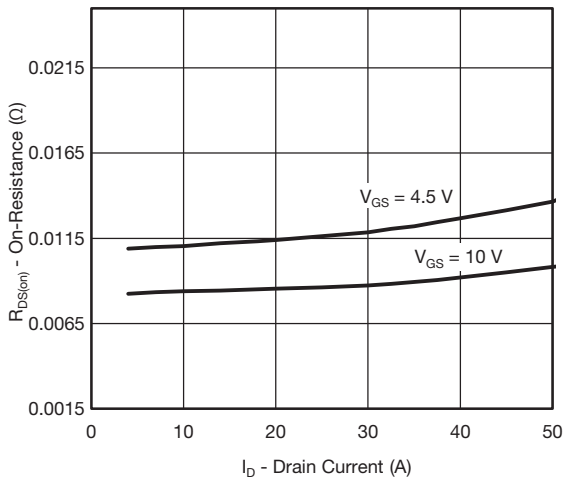
CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



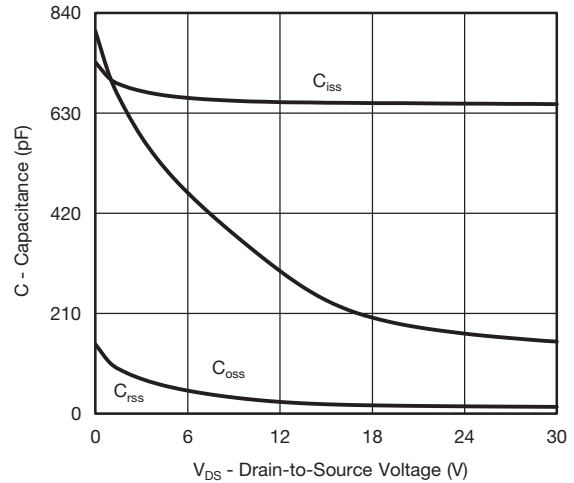
Output Characteristics



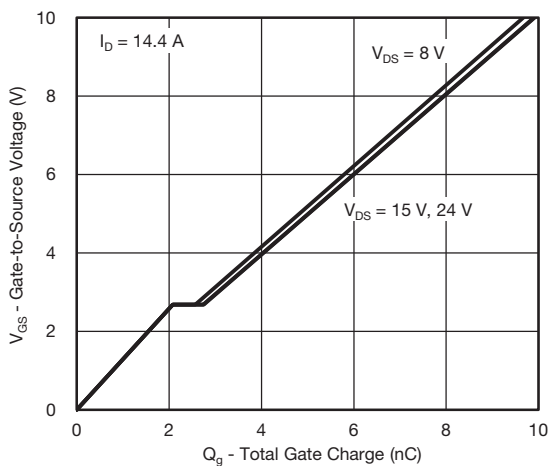
Transfer Characteristics



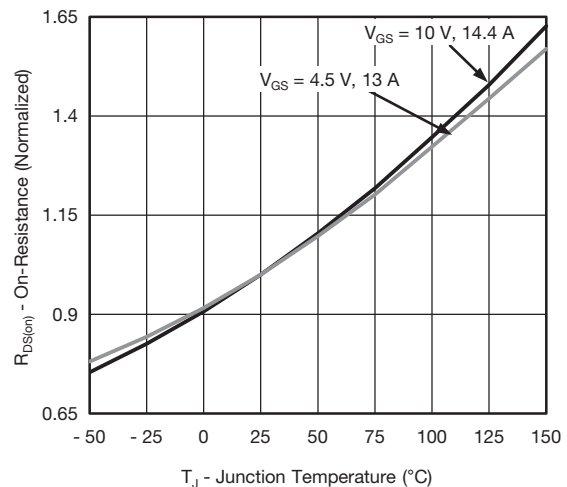
On-Resistance vs. Drain Current



Capacitance



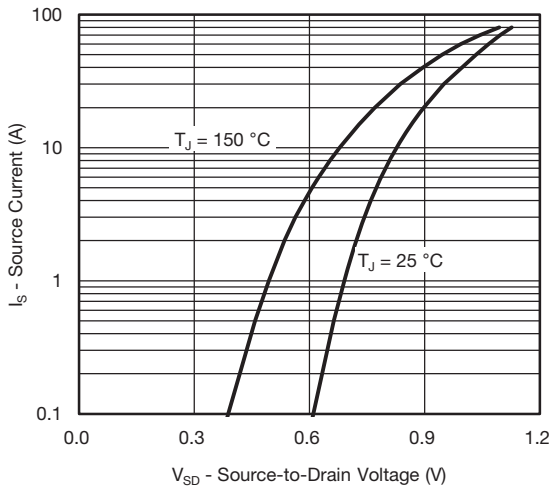
Gate Charge



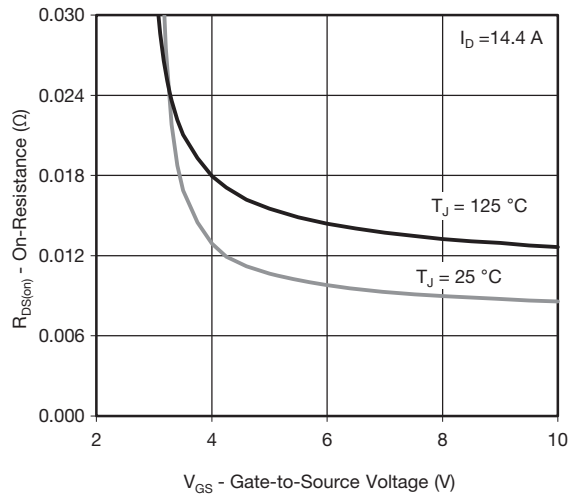
On-Resistance vs. Junction Temperature



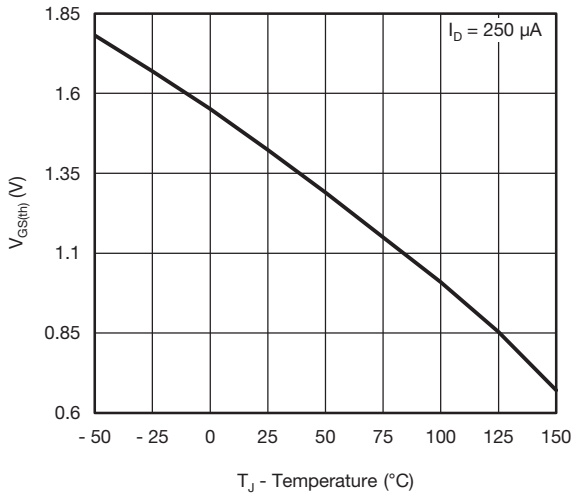
CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



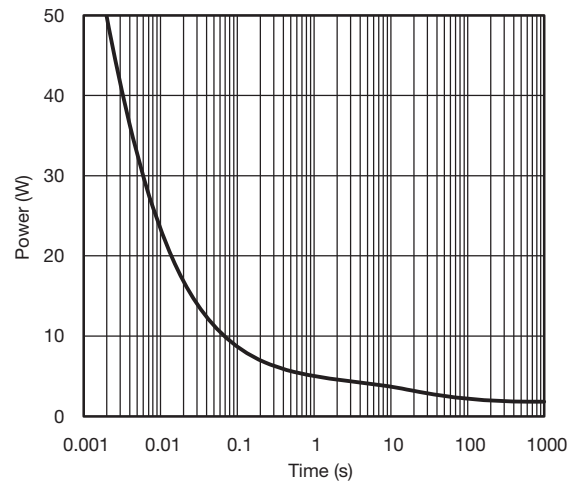
Source-Drain Diode Forward Voltage



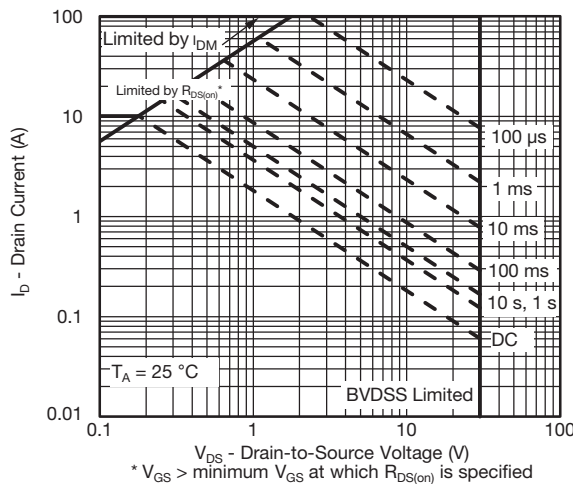
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

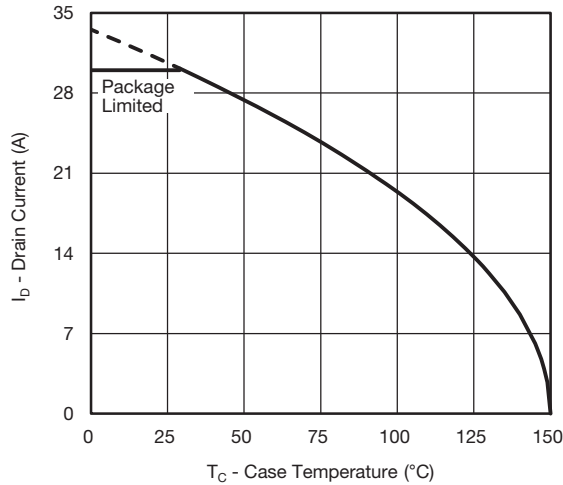


Single Pulse Power (Junction-to-Ambient)

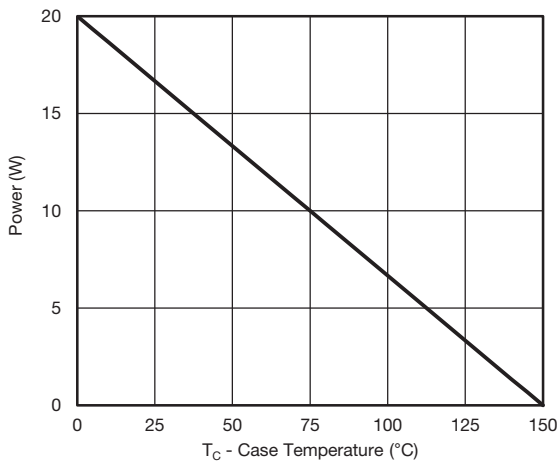


Safe Operating Area, Junction-to-Ambient

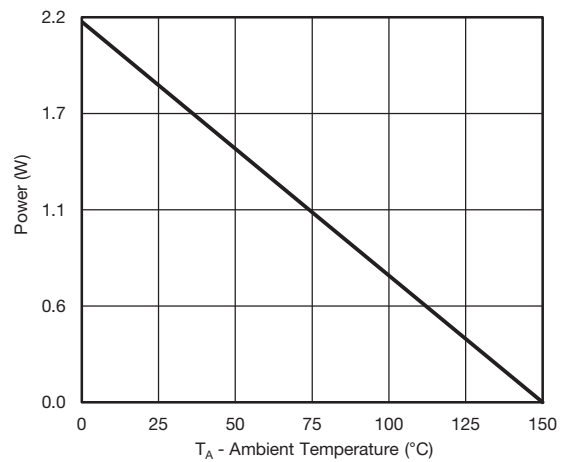
**CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



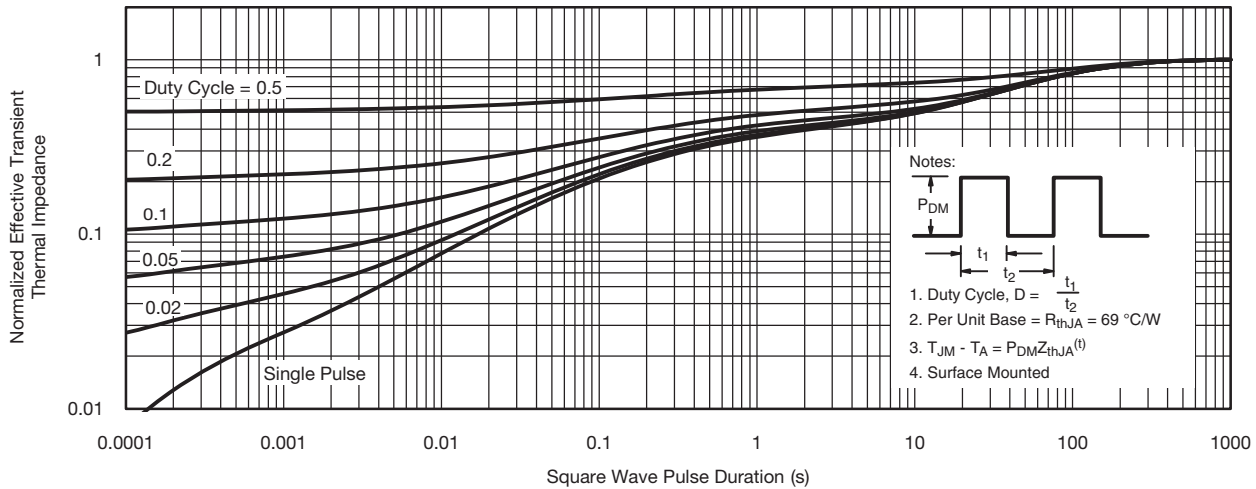
**Power, Junction-to-Case**



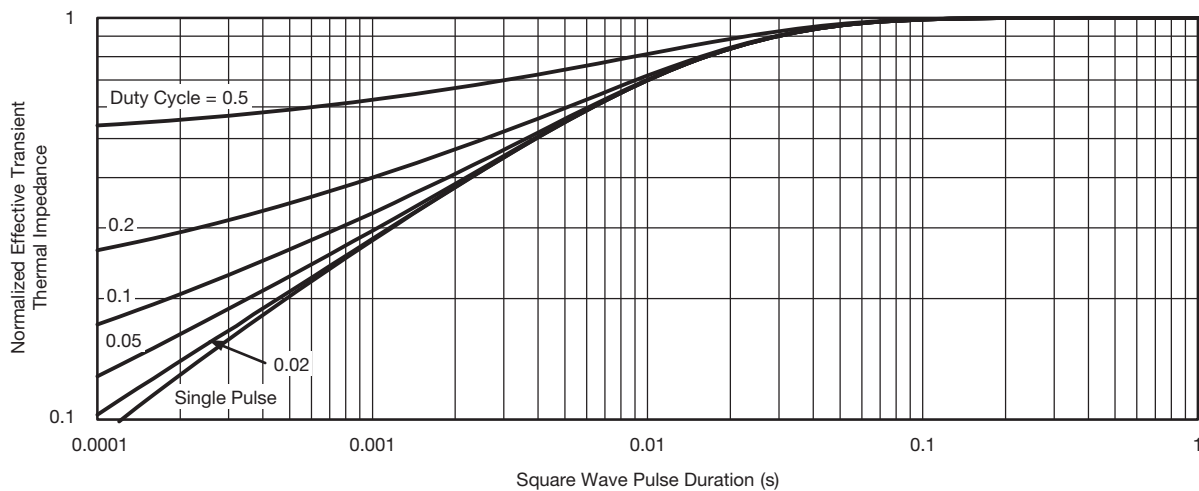
**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-1 AND CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

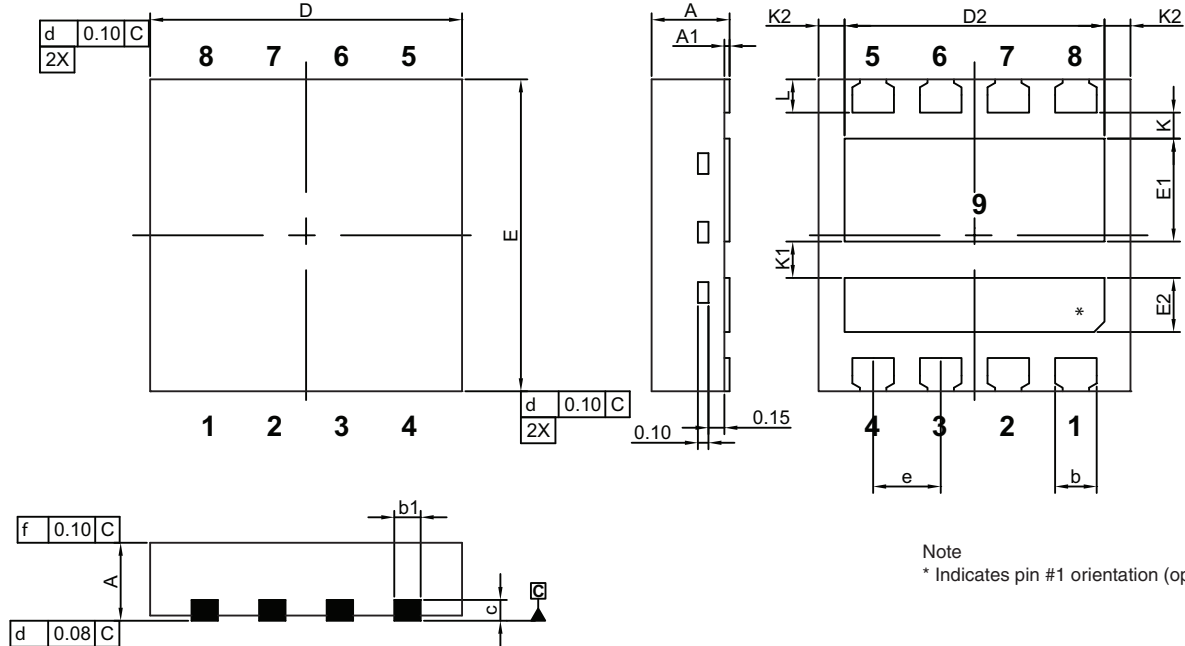


**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62949](http://www.vishay.com/ppg?62949).



PowerPAIR® 3 x 3 Case Outline



Note  
\* Indicates pin #1 orientation (optional)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12						
DWG: 5998						



## RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



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