

Dual N-Channel 25 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ.)
25	0.018 at V _{GS} = 10 V	8	7.8 nC
	0.020 at V _{GS} = 4.5 V	8	
	0.024 at V _{GS} = 2.5 V	7.5	

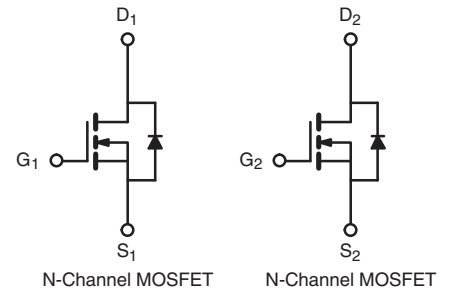
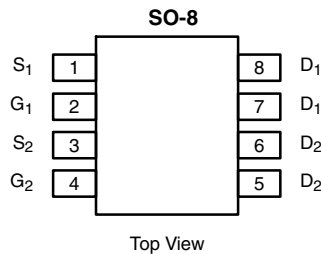
FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
COMPLIANT

APPLICATIONS

- Synchronous Buck Converter
- DC/DC Converter


Ordering Information: Si4228DY-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	25	V	
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	8 ^e	
		T _C = 70 °C	8 ^e	
		T _A = 25 °C	8 ^{b, c, e}	
		T _A = 70 °C	6.9 ^{b, c}	
Pulsed Drain Current	I _{DM}	50	A	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		2.6
		T _A = 25 °C		1.7 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	15		mJ
Avalanche Energy	E _{AS}	11.25		
Maximum Power Dissipation	P _D	T _C = 25 °C	3.1	
		T _C = 70 °C	2	
		T _A = 25 °C	2 ^{b, c}	
		T _A = 70 °C	1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	52	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	30	40	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 110 °C/W.
- Package limited.

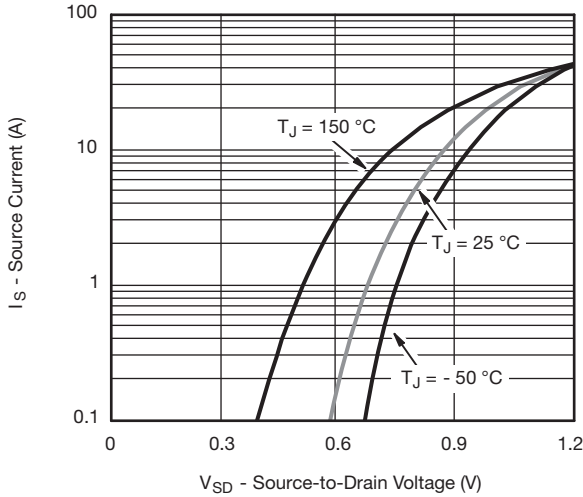
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		20		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-3.2			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$		0.015	0.018	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$		0.016	0.020	
		$V_{GS} = 2.5\text{ V}, I_D = 5\text{ A}$		0.020	0.024	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 7\text{ A}$		68		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 12.5\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		790		pF
Output Capacitance	C_{oss}		146			
Reverse Transfer Capacitance	C_{rss}		76			
Total Gate Charge	Q_g	$V_{DS} = 12.5\text{ V}, V_{GS} = 10\text{ V}, I_D = 8.6\text{ A}$		16.5	25	nC
		$V_{DS} = 12.5\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8.6\text{ A}$		7.8	12	
Gate-Source Charge	Q_{gs}		1.6			
Gate-Drain Charge	Q_{gd}		1.7			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.5	2.5	5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 12.5\text{ V}, R_L = 1.8\text{ }\Omega$ $I_D \cong 6.9\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		7	14	ns
Rise Time	t_r		12	18		
Turn-Off Delay Time	$t_{d(off)}$		21	30		
Fall Time	t_f		10	20		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 12.5\text{ V}, R_L = 1.8\text{ }\Omega$ $I_D \cong 6.9\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		4	8	
Rise Time	t_r		9	18		
Turn-Off Delay Time	$t_{d(off)}$		20	30		
Fall Time	t_f		7	14		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			2.6	A
Pulse Diode Forward Current ^a	I_{SM}				50	
Body Diode Voltage	V_{SD}	$I_S = 6.9\text{ A}$		0.82	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 6.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		15	23	ns
Body Diode Reverse Recovery Charge	Q_{rr}		6	12	nC	
Reverse Recovery Fall Time	t_a		8		ns	
Reverse Recovery Rise Time	t_b		7			

Notes

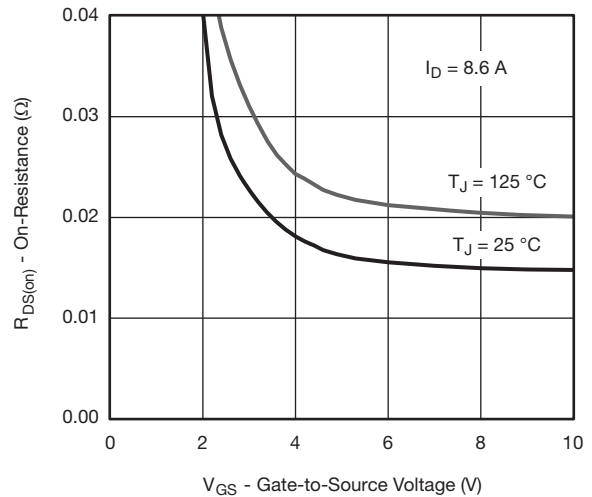
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

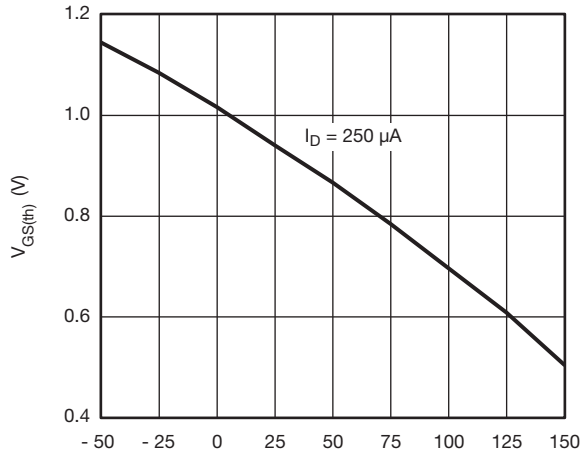
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



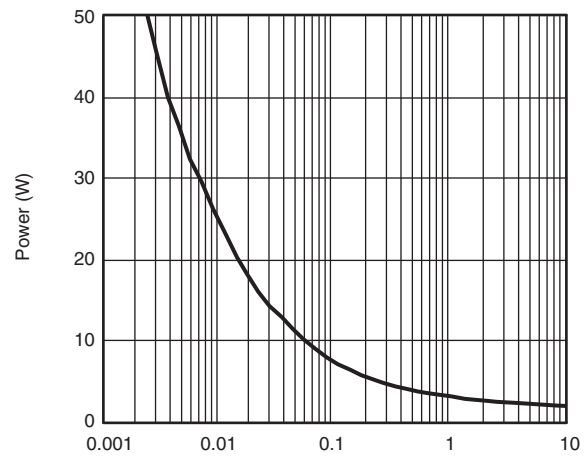
Source-Drain Diode Forward Voltage



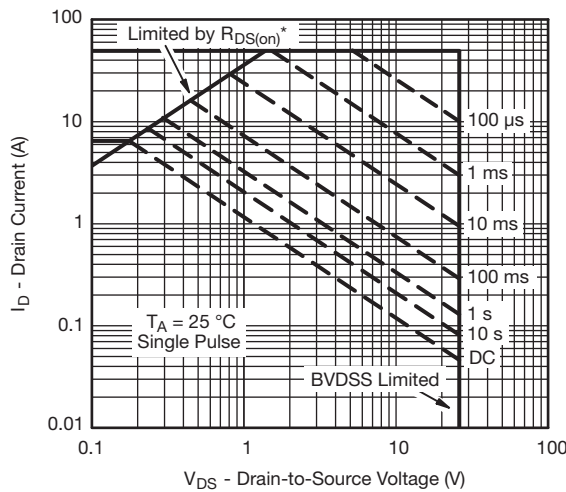
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



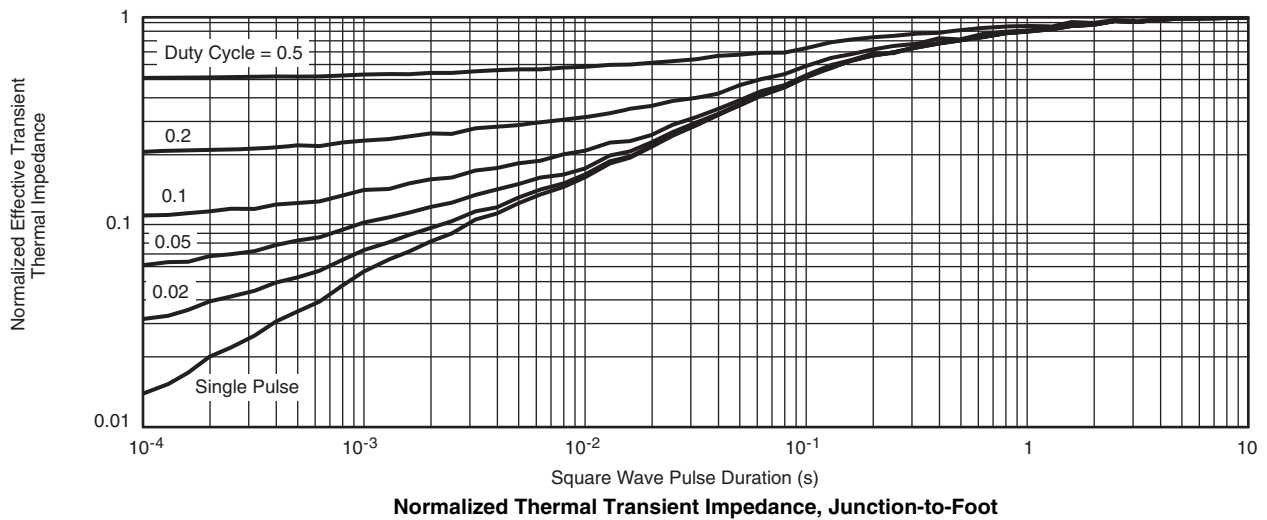
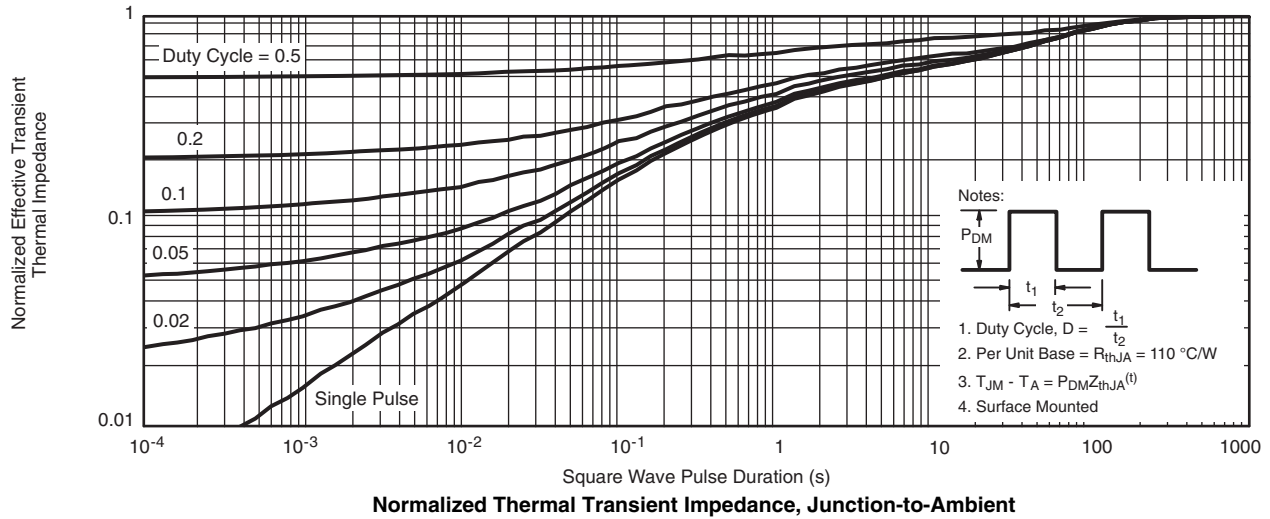
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations.

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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