

Vishay Siliconix

N-Channel 80-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$		Q _g (Typ.)			
80	0.013 at V _{GS} = 10 V	17.3	35 nC			

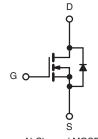
FEATURES

- · Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested

RoHS

APPLICATIONS

- Primary Side Switch
- · Half Bridge
- Intermediate Bus Converter



N-Channel MOSFET

			SO-8			
s s s G	1 2 3 4				8 7 6 5	D D D
		To	p Viev	v		

Ordering Information: Si4110DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATIN	IGS T _A = 25 °C,	unless otherwise	noted	
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	80	V
Gate-Source Voltage		V _{GS}	± 20	
	T _C = 25 °C		17.3	
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	13.9	
Continuous Diain Current (1) = 130 C)	T _A = 25 °C	'D	11.7 ^{b, c}	
	T _A = 70 °C		9.4 ^{b, c}	А
Pulsed Drain Current		I _{DM}	60	^
Continuous Source-Drain Diode Current	T _C = 25 °C		6.5	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	3 ^{b, c}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	35	
Single Pulse Avalanche Energy		E _{AS}	61.3	mJ
	T _C = 25 °C		7.8	
Maximum Power Dissipation	T _C = 70 °C	P _D	5	w
Maximum Fower Dissipation	T _A = 25 °C	' D	3.6 ^{b, c}	VV
	T _A = 70 °C		2.3 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Tempera		260		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	29	35	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	13	16			

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. Maximum under Steady State conditions is 80 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	,			7.			
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V, I}_{D} = 250 \mu\text{A}$	80			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		84			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 9.8		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2		4	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valta va Dvaira Coverant		V _{DS} = 80 V, V _{GS} = 0 V			1	^	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 11.7 \text{ A}$		0.0108	0.0130	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 11.7 A		23		S	
Dynamic ^b							
Input Capacitance	C _{iss}			2205		pF	
Output Capacitance	C _{oss}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		260			
Reverse Transfer Capacitance	C _{rss}			78			
Total Gate Charge	Qg			35	53	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 11.7 \text{ A}$		12.5			
Gate-Drain Charge	Q _{gd}			8			
Gate Resistance	R_{g}	f = 1 MHz	0.22	1.1	2.2	Ω	
Turn-on Delay Time	t _{d(on)}			18	27	ns	
Rise Time	t _r	V_{DD} = 40 V, R_L = 4.3 Ω		10	18		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 9.4$ A, V_{GEN} = 8 V, R_g = 1 Ω		22	33		
Fall Time	t _f			8	16		
Turn-On Delay Time	t _{d(on)}			15	23		
Rise Time	t _r	V_{DD} = 40 V, R_L = 4.3 Ω		9	18		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 9.4 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	33		
Fall Time	t _f			7	14		
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	I _S	$T_C = 25 ^{\circ}C$			6.5	А	
Pulse Diode Forward Current ^a	I _{SM}				60		
Body Diode Voltage	V_{SD}	I _S = 9.4 A		0.80	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			45	68	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 9.4 A, dl/dt = 100 A/μs, T _J = 25 °C		82	123	nC	
Reverse Recovery Fall Time	t _a	i _F = 0.4 Λ, αι/αι = 100 Λ/μδ, 1 _J = 25 °C		34			
Reverse Recovery Rise Time t _b				11		ns	

Notes:

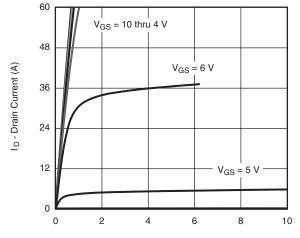
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



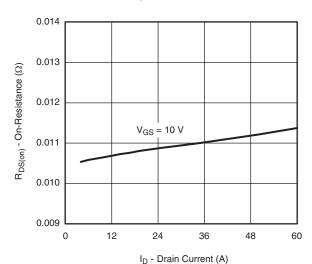
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

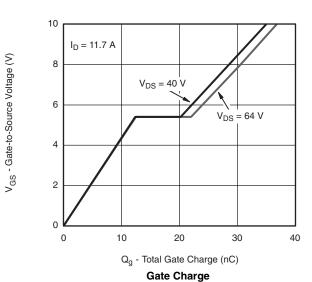


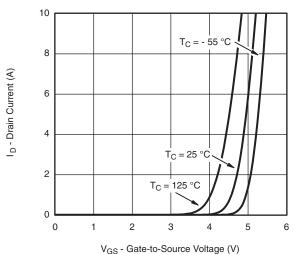
V_{DS} - Drain-to-Source Voltage (V)





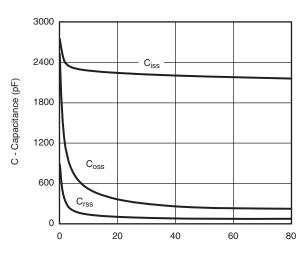
On-Resistance vs. Drain Current





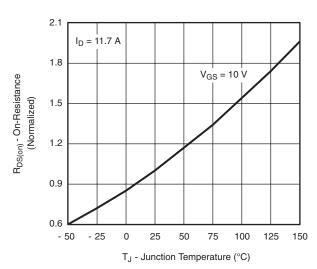
VGS date to bounce voltage (v)

Transfer Characteristics



 $V_{\mbox{\footnotesize DS}}$ - Drain-to-Source Voltage (V)

Capacitance



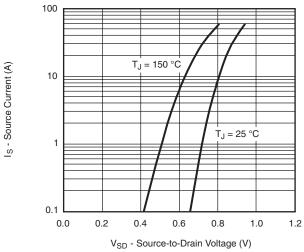
On-Resistance vs. Junction Temperature

Si4110DY

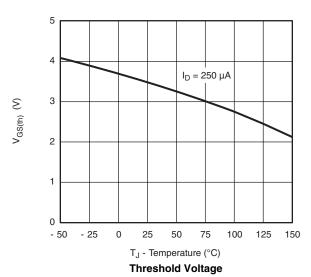
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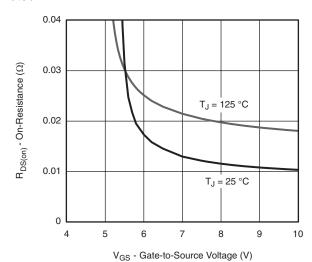
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

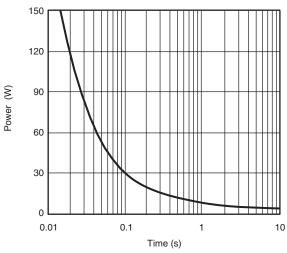


Source-Drain Diode Forward Voltage

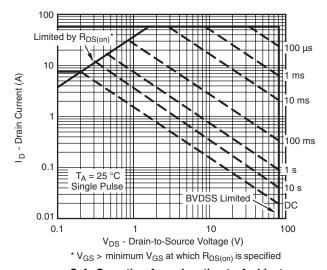




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

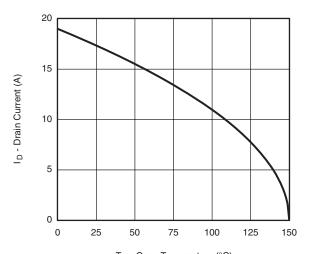


Safe Operating Area, Junction-to-Ambient



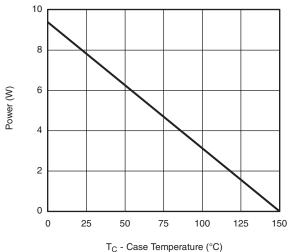
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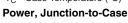
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

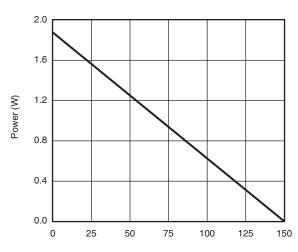


T_C - Case Temperature (°C)

Current Derating*







T_A - Ambient Temperature (°C) **Power, Junction-to-Ambient**

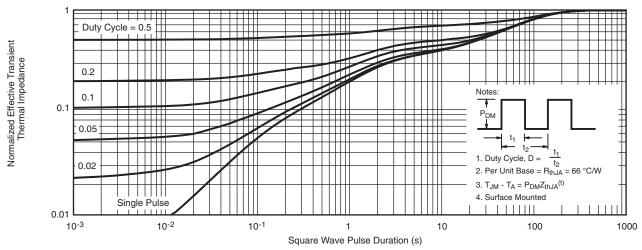
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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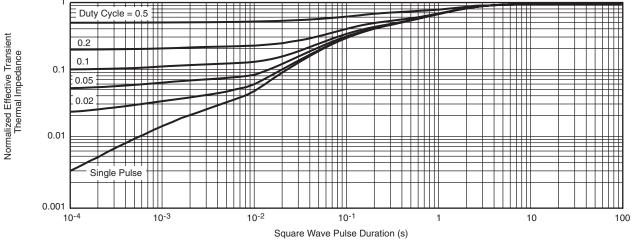
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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