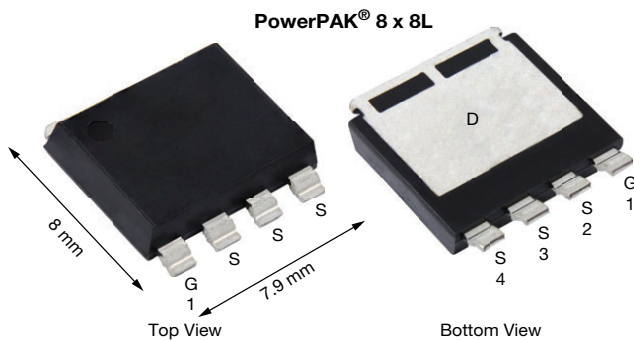


Automotive N-Channel 40 V (D-S) 175 °C MOSFET

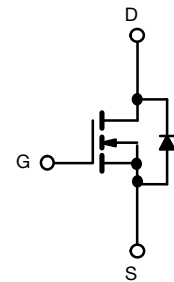


RoHS
COMPLIANT
HALOGEN
FREE



FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



N-Channel MOSFET

PRODUCT SUMMARY

| | |
|--|---------|
| V_{DS} (V) | 40 |
| $R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V | 0.00053 |
| I_D (A) | 701 |
| Configuration | Single |

ORDERING INFORMATION

| | |
|---------------------------------|--|
| Package | PowerPAK 8 x 8L |
| Lead (Pb)-free and halogen-free | SQJQ140E (for detailed order number please see www.vishay.com/doc?79776) |

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|----------------|----------------|------|
| Drain-source voltage | V_{DS} | 40 | V |
| Gate-source voltage | V_{GS} | ± 20 | |
| Continuous drain current | I_D | $T_C = 25$ °C | 701 |
| | | $T_C = 125$ °C | 405 |
| Continuous source current (diode conduction) | I_S | 545 | A |
| Pulsed drain current ^a | I_{DM} | 1820 | |
| Single pulse avalanche current | I_{AS} | 79 | mJ |
| Single pulse avalanche energy | | | |
| Maximum power dissipation | P_D | $T_C = 25$ °C | 600 |
| | | $T_C = 125$ °C | 200 |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +175 | °C |
| Soldering recommendations (peak temperature) ^c | | 260 | |

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | LIMIT | UNIT |
|--------------------------|------------|-------|------|
| Junction-to-ambient | R_{thJA} | 44 | °C/W |
| Junction-to-case (drain) | | | |

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



| SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|--------------|---|---|------|---------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$ | | 40 | - | - | V |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.3 | 2.7 | 3.3 | |
| Gate-source leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero gate voltage drain current | I_{DSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}$ | - | - | 1 | μA |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | - | - | 50 | |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$ | - | - | 150 | |
| On-state drain current ^a | $I_{D(on)}$ | $V_{GS} = 10\text{ V}$ | $V_{DS} \geq 5\text{ V}$ | 100 | - | - | A |
| Drain-source on-state resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 20\text{ A}$ | - | 0.00044 | 0.00053 | Ω |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | - | - | 0.00092 | |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$ | - | - | 0.0013 | |
| Forward transconductance ^b | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 80\text{ A}$ | | - | 160 | - | S |
| Dynamic ^b | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | - | 12 140 | 17 000 | μF |
| Output capacitance | C_{oss} | | | - | 4740 | 6636 | |
| Reverse transfer capacitance | C_{rss} | | | - | 308 | 432 | |
| Total gate charge ^c | Q_g | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 40\text{ A}$ | - | 192 | 288 | nC |
| Gate-source charge ^c | Q_{gs} | | | - | 55 | - | |
| Gate-drain charge ^c | Q_{gd} | | | - | 41 | - | |
| Gate resistance | R_g | f = 1 MHz | | 0.8 | 1.6 | 2.4 | Ω |
| Turn-on delay time ^c | $t_{d(on)}$ | $V_{DD} = 20\text{ V}, R_L = 0.5\text{ }\Omega$ $I_D \equiv 40\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$ | | - | 26 | 39 | ns |
| Rise time ^c | t_r | | | - | 78 | 117 | |
| Turn-off delay time ^c | $t_{d(off)}$ | | | - | 62 | 93 | |
| Fall time ^c | t_f | | | - | 32 | 48 | |
| Source-Drain Diode Ratings and Characteristics ^b | | | | | | | |
| Reverse recovery time | t_{rr} | $V_{DD} = 32\text{ V}, I_{FM} = 20\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}$ | | - | 94 | 188 | ns |
| Reverse recovery charge | Q_{rr} | | | - | 177 | 354 | nC |
| Reverse recovery current | I_{RM} | | | - | -3.2 | - | A |
| Pulsed current ^a | I_{SM} | | | - | - | 1600 | A |
| Forward voltage | V_{SD} | $I_F = 50\text{ A}, V_{GS} = 0$ | | - | 0.8 | 1.1 | V |

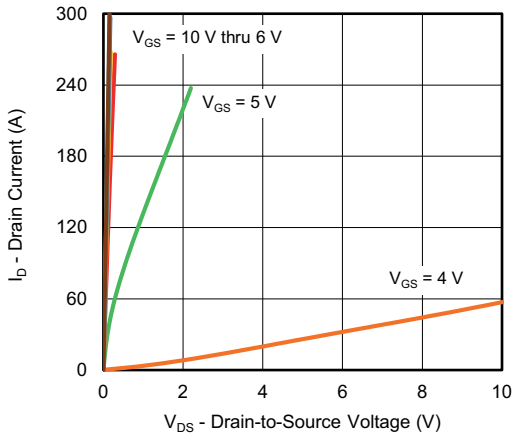
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

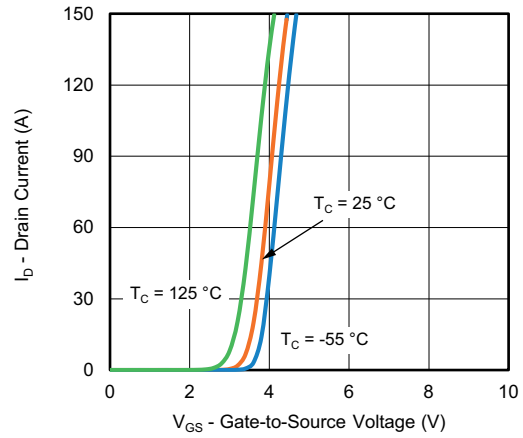
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



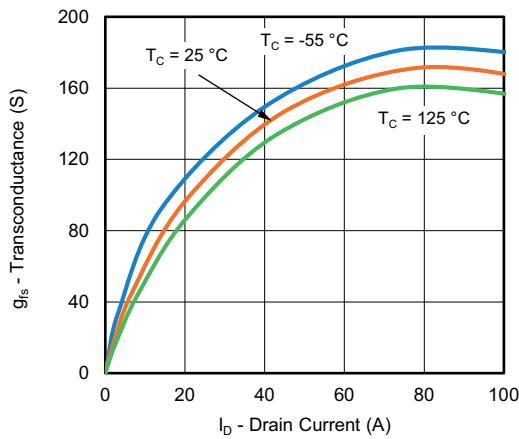
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



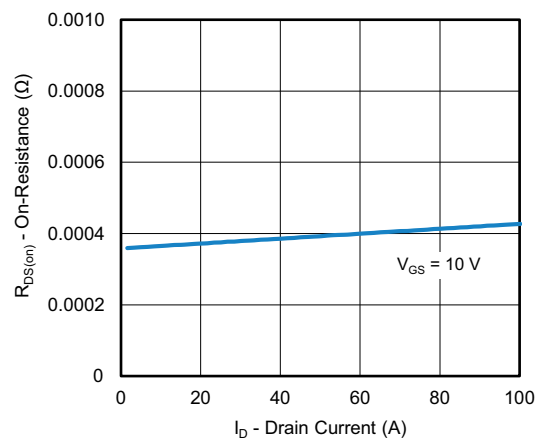
Output Characteristics



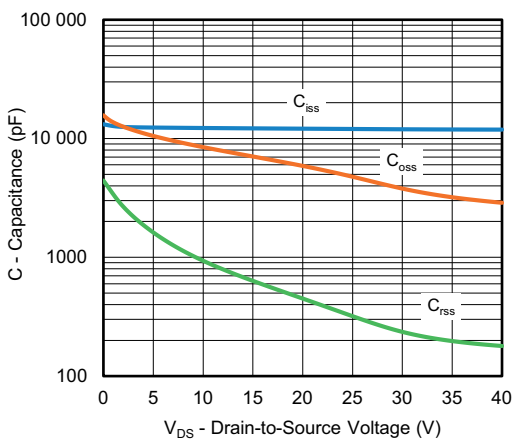
Transfer Characteristics



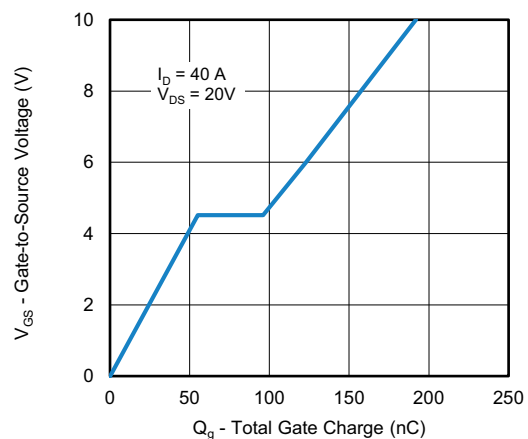
Transconductance



On-Resistance vs. Drain Current

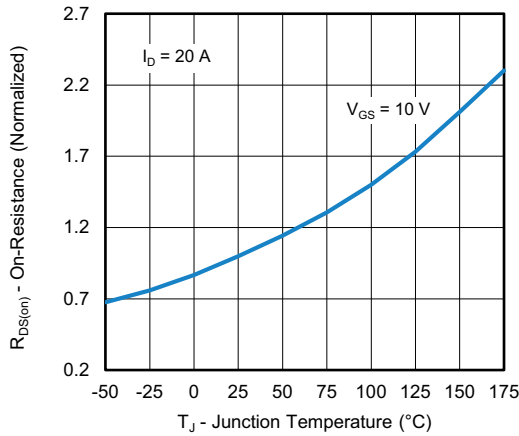


Capacitance

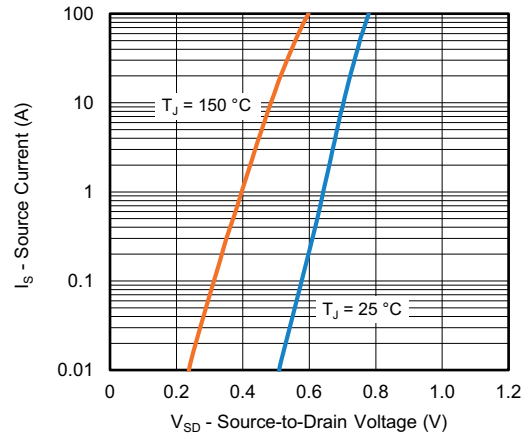


Gate Charge

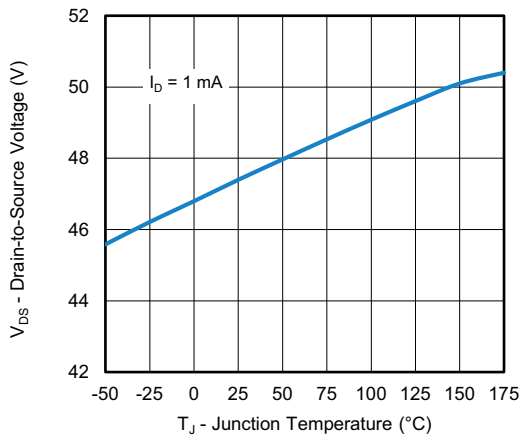
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



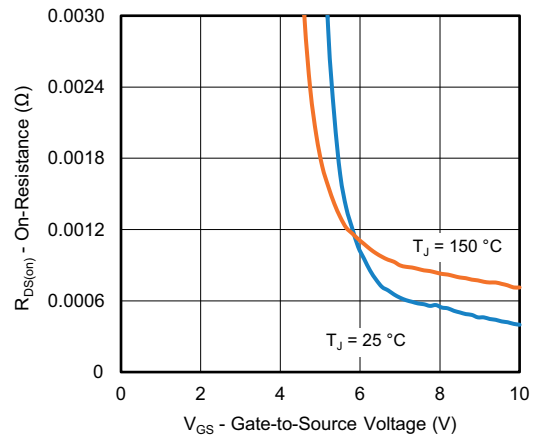
On-Resistance vs. Junction Temperature



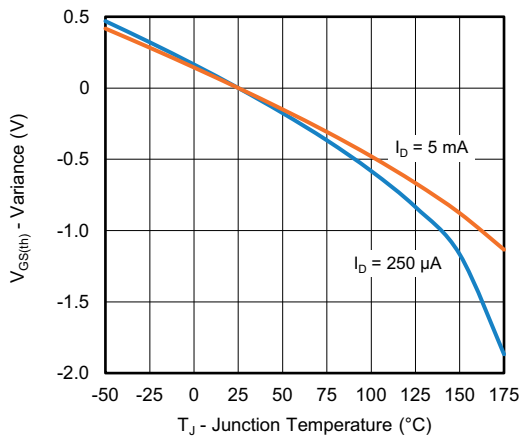
Source Drain Diode Forward Voltage



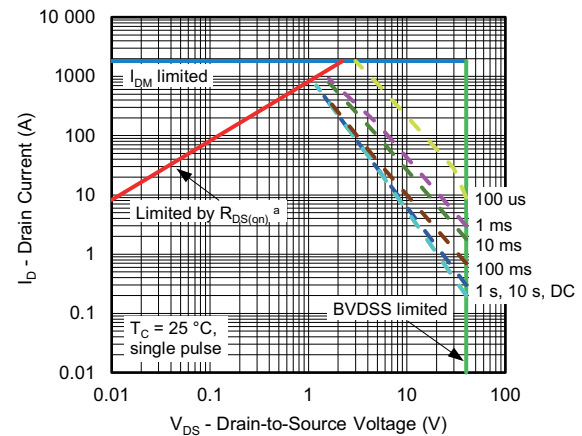
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



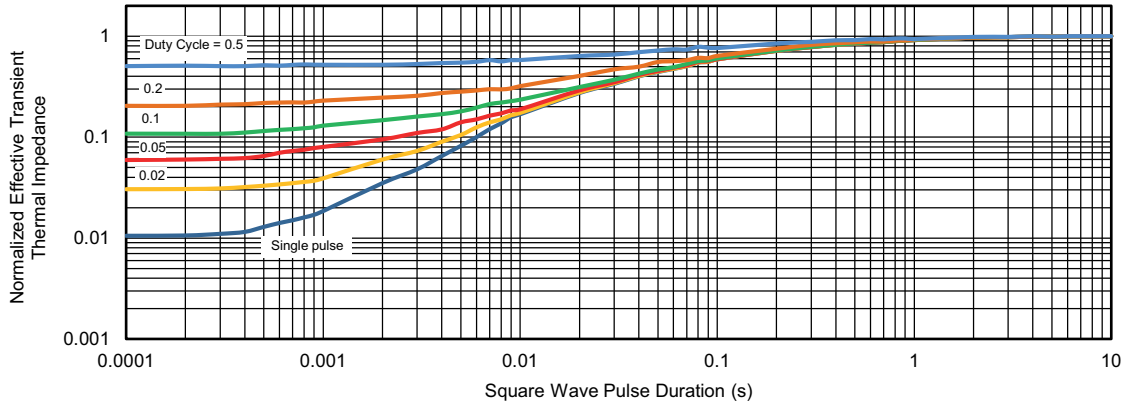
Safe Operating Area

Note

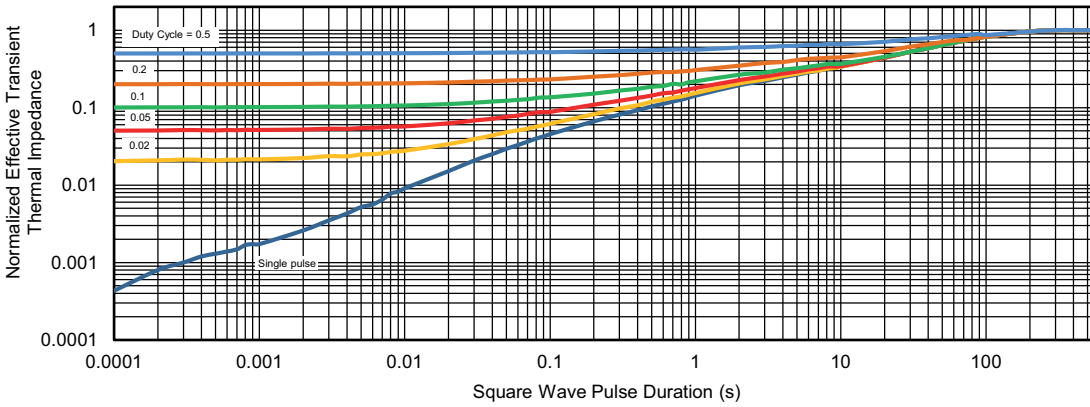
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

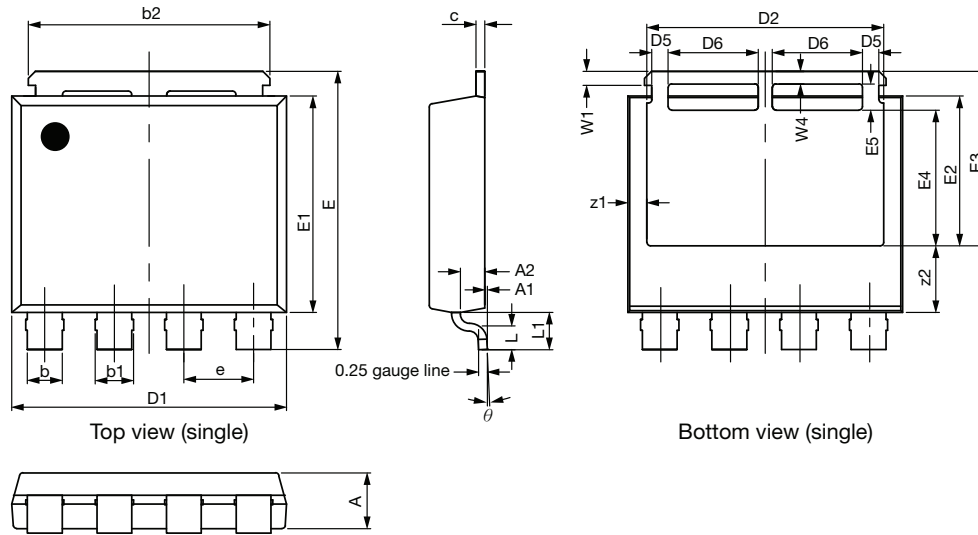


Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® 8 x 8L BWL Case Outline 2



| DIM. | MILLIMETERS | | | INCHES | | |
|------|-------------|-------|-------|--------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.50 | 1.60 | 1.70 | 0.059 | 0.063 | 0.067 |
| A1 | 0.00 | - | 0.127 | 0.000 | - | 0.005 |
| A2 | 0.655 | 0.705 | 0.755 | 0.026 | 0.028 | 0.030 |
| b | 0.92 | 1.00 | 1.08 | 0.036 | 0.039 | 0.043 |
| b1 | 1.02 | 1.10 | 1.18 | 0.040 | 0.043 | 0.046 |
| b2 | 6.84 | 6.94 | 7.04 | 0.269 | 0.273 | 0.277 |
| c | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D1 | 7.80 | 7.90 | 8.00 | 0.307 | 0.311 | 0.315 |
| D2 | 6.70 | 6.80 | 6.90 | 0.264 | 0.268 | 0.272 |
| D5 | 0.37 | 0.47 | 0.57 | 0.015 | 0.019 | 0.022 |
| D6 | 2.49 | 2.59 | 2.69 | 0.098 | 0.102 | 0.106 |
| e | 1.97 | 2.00 | 2.03 | 0.078 | 0.079 | 0.080 |
| E | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| E1 | 6.12 | 6.22 | 6.32 | 0.241 | 0.245 | 0.249 |
| E2 | 4.21 | 4.31 | 4.41 | 0.166 | 0.170 | 0.174 |
| E3 | 4.92 | 5.02 | 5.12 | 0.194 | 0.198 | 0.202 |
| E4 | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| E5 | 0.65 | 0.75 | 0.85 | 0.026 | 0.030 | 0.033 |
| L | 0.61 | 0.68 | 0.75 | 0.024 | 0.027 | 0.030 |
| L1 | 1.00 | 1.07 | 1.15 | 0.039 | 0.042 | 0.045 |
| W1 | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| W4 | 0.32 | 0.37 | 0.42 | 0.013 | 0.015 | 0.017 |
| z1 | 0.45 | 0.55 | 0.65 | 0.018 | 0.022 | 0.026 |
| z2 | 1.81 | 1.91 | 2.01 | 0.071 | 0.075 | 0.079 |
| θ | 0° | - | 5° | 0° | - | 5° |

ECN: S19-0643-Rev. B, 05-Aug-2019
DWG: 6073

Note

- Millimeter will govern



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