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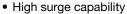
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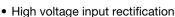
## Thyristor High Voltage, Phase Control SCR, 70 A

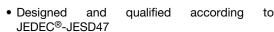


PRIMARY CHARACTERISTICS				
$I_{T(AV)}$	70 A			
$V_{DRM}/V_{RRM}$	1200 V, 1600 V			
$V_{TM}$	1.25 V			
I <sub>GT</sub>	100 mA			
$T_J$	-40 °C to +125 °C			
Package	Super TO-247			
Circuit configuration	Single SCR			

#### **FEATURES**







(e3)

RoHS

 Material categorization: for definitions of compliant compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>

#### **APPLICATIONS**

- AC switches
- High voltage input rectification (soft start)
- · High current crow-bar
- Other phase-control circuits
- Designed to be used with Vishay input diodes, switches, and output rectifiers which are available in identical package outlines

#### **DESCRIPTION**

The VS-70TPS..PbF high voltage series of silicon controlled rectifiers are specifically designed for high and medium power switching, and phase control applications.

MAJOR RATINGS AND CHARACTERISTICS						
PARAMETER	TEST CONDITIONS	VALUES	UNITS			
I <sub>T(AV)</sub>	Sinusoidal waveform	70	۸			
I <sub>RMS</sub>	Lead current limitation	75	Α			
V <sub>RRM</sub> /V <sub>DRM</sub>	Range	1200 to 1600	V			
I <sub>TSM</sub>		1100	Α			
V <sub>T</sub>	100 A, T <sub>J</sub> = 25 °C	1.4	V			
dV/dt		500	V/µs			
dl/dt		150	A/µs			
TJ		-40 to +125	°C			

VOLTAGE RATINGS						
PART NUMBER	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> AT 125 °C mA			
VS-70TPS12PbF	1200	1300	15			
VS-70TPS16PbF	1600	1700	15			



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PARAMETER	SYMBOL	Т	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current	I <sub>T(AV)</sub>	T <sub>C</sub> = 82 °C, 180° cor	nduction half sine wave		70	
Maximum continuous RMS on-state current as AC switch	I <sub>T(RMS)</sub>	Lead current limitation	Lead current limitation		75	А
Maximum peak, one-cycle	L	10 ms sine pulse, rat	ted V <sub>RRM</sub> applied		930	
non-repetitive surge current	I <sub>TSM</sub>	10 ms sine pulse, no	voltage reapplied	LOCALE E	1100	
Maximum 12t for fusing	I <sup>2</sup> t	10 ms sine pulse, rat	ted V <sub>RRM</sub> applied	Initial T <sub>J</sub> = T <sub>J</sub> maximum	4325	A <sup>2</sup> s
Maximum I <sup>2</sup> t for fusing	I-ι	10 ms sine pulse, no	10 ms sine pulse, no voltage reapplied maximum			A-S
Maximum l <sup>2</sup> √t for fusing	I²√t	t = 0.1 ms to 10 ms, no voltage reapplied		61 150	A²√s	
Low level value of threshold voltage	V <sub>T(TO)1</sub>			0.916	V	
High level value of threshold voltage	V <sub>T(TO)2</sub>	T <sub>.1</sub> = 125 °C		1.21	V	
Low level value of on-state slope resistance	r <sub>t1</sub>	11= 125 0		4.138	<b>m</b> 0	
High level value of on-state slope resistance	r <sub>t2</sub>			3.43	mΩ	
Maximum peak on-state voltage	$V_{TM}$	100 A, T <sub>J</sub> = 25 °C			1.4	V
Maximum rate of rise of turned-on current	dl/dt	T <sub>J</sub> = 25 °C		150	A/μs	
Maximum holding current	I <sub>H</sub>	Anode supply = 6 V, resistive load, initial I <sub>T</sub> = 1 A, T <sub>J</sub> = 25 °C		200		
Maximum latching current	ΙL	Anode supply = 6 V, resistive load, T <sub>J</sub> = 25 °C		400	A	
Maximum reverse and direct leakage current	I <sub>RRM</sub> /I <sub>DRM</sub>	T <sub>J</sub> = 25 °C	$V_R = \text{rated } V_{RRM} / V_{DR}$	M	1.0	mA
Maximum reverse and direct leakage current		T <sub>J</sub> = 125 °C				
Maximum rate of rise of off-state voltage	dV/dt	$T_J = 125 ^{\circ}\text{C}$ $V_{DRM} = R_g - k = \text{open}$		500	V/µs	

TRIGGERING					
PARAMETER	SYMBOL		TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P <sub>GM</sub>	T = 30 µs		10	W
Maximum average gate power	P <sub>G(AV)</sub>	ι = 30 μs		2.5	٧٧
Maximum peak gate current	I <sub>GM</sub>			2.5	Α
Maximum peak negative gate voltage	- V <sub>GM</sub>			10	
		T <sub>J</sub> = - 40 °C	Anode supply = 6 V resistive load	1.8	V
Maximum required DC gate voltage to trigger	$V_{\mathrm{GT}}$	T <sub>J</sub> = 25 °C		1.5	v
		T <sub>J</sub> = 125 °C		1.1	
		T <sub>J</sub> = - 40 °C		150	
Maximum required DC gate current to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C	Anode supply = 6 V resistive load	100	mA
		T <sub>J</sub> = 125 °C		80	
Maximum DC gate voltage not to trigger	$V_{GD}$	T 405 %C V		0.25	V
Maximum DC gate current not to trigger	$I_{GD}$	T <sub>J</sub> = 125 °C, V <sub>DRM</sub> = rated value		6	mA

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THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction temperature	range	TJ		-40 to +125	°C
Maximum storage temperature	range	T <sub>Stg</sub>		-40 to +150	
Maximum thermal resistance, junction to case		R <sub>thJC</sub>	DC operation	0.27	
Maximum thermal resistance, junction to ambient		R <sub>thJA</sub>		40	°C/W
Typical thermal resistance, case to heatsink		R <sub>thCS</sub>	Mounting surface, smooth and greased	0.2	
A				6	g
Approximate weight				0.21	OZ.
Mounting torque	minimum			6 (5)	kgf · cm
Modifiling torque	maximum			12 (10)	(lbf · in)
Marking device			Casa stula Super TO 247	70TPS	12
			Case style Super TO-247	70TPS	70TPS16

△R <sub>thJ-hs</sub> CONDUCTION PER JUNCTION											
DEVICE	SINE HALF WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION				UNITS	
DEVICE	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	UNITS
VS-70TPSPbF	0.078	0.092	0.117	0.172	0.302	0.053	0.092	0.125	0.180	0.306	°C/W

#### Note

The table above shows the increment of thermal resistance R<sub>thJ-hs</sub> when devices operate at different conduction angles than DC

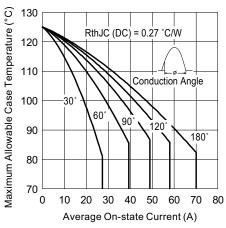


Fig. 1 - Current Rating Characteristics

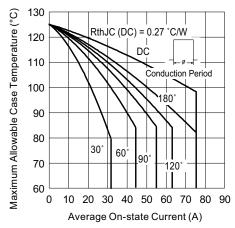


Fig. 2 - Current Rating Characteristics

1000

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At any rated load condition and with

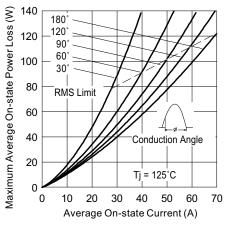
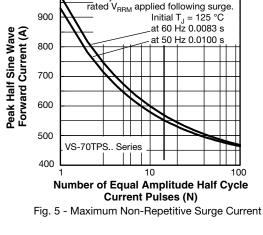


Fig. 3 - On-State Power Loss Characteristics



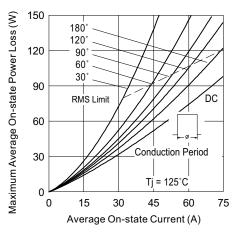


Fig. 4 - On-State Power Loss Characteristics

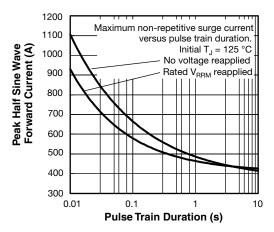


Fig. 6 - Maximum Non-Repetitive Surge Current

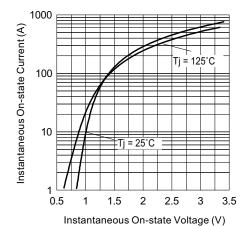
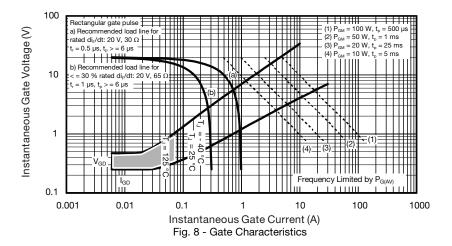


Fig. 7 - On-State Voltage Drop Characteristics

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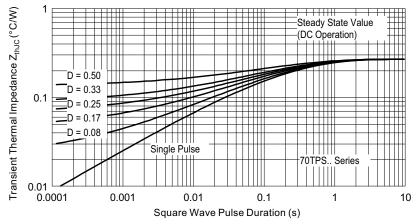


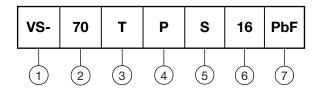
Fig. 9 - Thermal Impedance  $Z_{thJC}$  Characteristics

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#### **ORDERING INFORMATION TABLE**





1 - Vishay Semiconductors product

2 - Current rating (70 = 70 A)

3 - Circuit configuration:

T = thyristor

4 - Package:

P = super TO-247

5 - Type of silicon:

S = standard recovery rectifier

6 - Voltage code x 100 = V<sub>RRM</sub> - 12 = 1200 V 16 = 1600 V

7 - PbF = lead (Pb)-free

ORDERING INFORMATION (example)						
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION			
VS-70TPS12PbF	25	500	Antistatic plastic tube			
VS-70TPS16PbF	25	500	Antistatic plastic tube			

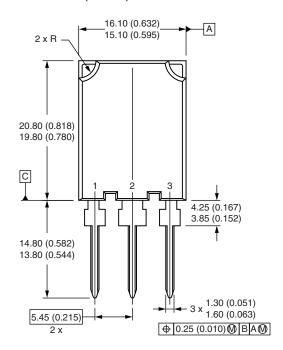
LINKS TO RELATED DOCUMENTS					
Dimensions <u>www.vishay.com/doc?95073</u>					
Part marking information	www.vishay.com/doc?95070				

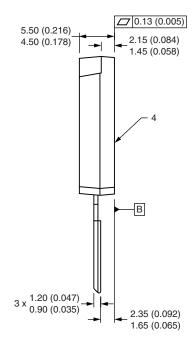


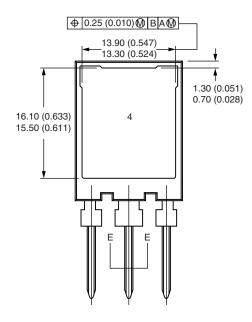
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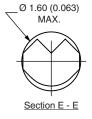
# Super TO-247

### **DIMENSIONS** in millimeters (inches)









#### Lead assignments

MOSFET	<u>IGBT</u>
1 - Gate	1 - Gate
2 - Drain	2 - Collector
3 - Source	3 - Emitter
4 - Drain	4 - Collector

#### Notes

- (1) Dimension and tolerancing per ASME Y14.5M-1994
- (2) Controlling dimension: millimeter
- (3) Outline conforms to JEDEC® outline TO-274AA



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