# Low-Power, High-Speed CMOS Analog Switches

## FEATURES

- 44-V Supply Max Rating
- ±15-V Analog Signal Range
- On-Resistance—$r_{DS(on)}$: 20 Ω
- Low Leakage—$I_{D(on)}$: 40 pA
- Fast Switching—$t_{ON}$: 100 ns
- Ultra Low Power Requirements—$P_D$: 0.35 µW
- TTL, CMOS Compatible
- Single Supply Capability

## BENEFITS

- Wide Dynamic Range
- Break-Before-Make Switching Action
- Simple Interfacing

## APPLICATIONS

- Audio and Video Switching
- Sample-and-Hold Circuits
- Battery Operation
- Test Equipment
- Hi-Rel Systems
- PBX, PABX

## DESCRIPTION

The DG401/403/405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35 µW, typ) with high speed ($t_{ON}$: 100 ns, typ), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Vishay Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

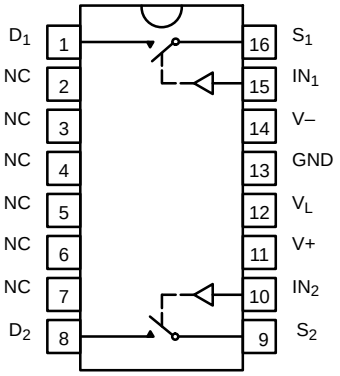
Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ±15-V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG401**

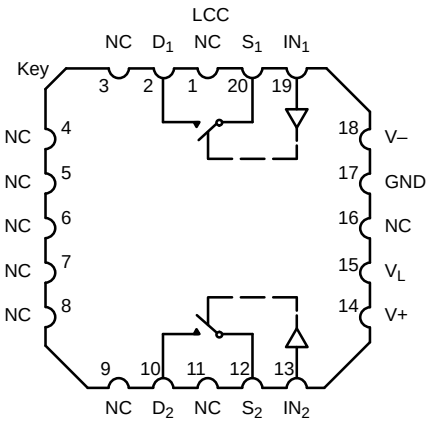
Dual-In-Line and SOIC




Top View

**DG401**

LCC




Top View

Two SPST Switches per Package

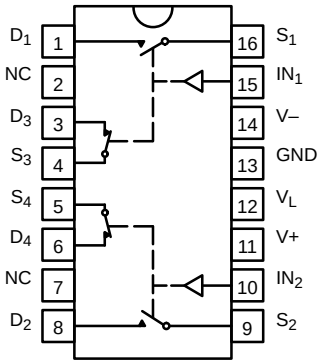
| TRUTH TABLE | |
|---|---|
| **Logic** | **Switch** |
| 0 | OFF |
| 1 | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG403**

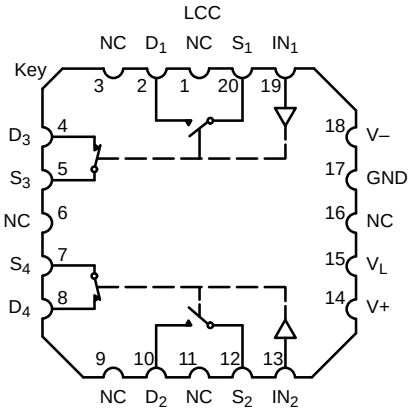
Dual-In-Line and SOIC




Top View

**DG403**

LCC




Top View

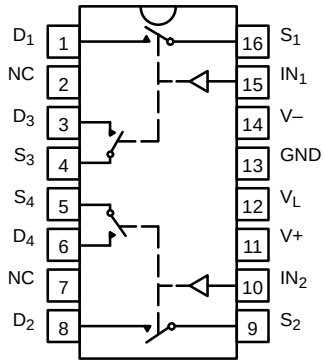
Two SPDT Switches per Package

| TRUTH TABLE | | |
|---|---|---|
| **Logic** | **$SW_1$, $SW_2$** | **$SW_3$, $SW_4$** |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

**DG405**

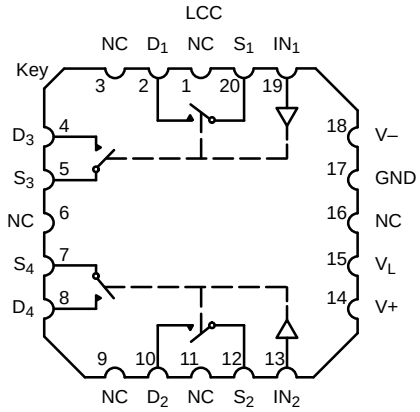
Dual-In-Line and SOIC




Top View

**DG405**

LCC




Top View

Two DPST Switches per Package

| TRUTH TABLE | |
|---|---|
| **Logic** | **Switch** |
| 0 | OFF |
| 1 | ON |

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

| ORDERING INFORMATION | | |
|---|---|---|
| **Temp Range** | **Package** | **Part Number** |
| **DG401** | | |
| –40 to 85°C | 16-Pin Plastic DIP | DG401DJ |
| –55 to 125°C | 16-Pin CerDIP | DG401AK |
| | | DG401AK/883, 5962-9056901MEA |
| | LCC-20 | DG401AZ/883, 5962-9056901M2A |
| **DG403** | | |
| –40 to 85°C | 16-Pin Plastic DIP | DG403DJ |
| | 16-Pin Narrow SOIC | DG403DY |
| –55 to 125°C | 16-Pin CerDIP | DG403AK |
| | | DG403AK/883, 5962-8976301MEA |
| | LCC-20 | 5962-8976301M2A |
| **DG405** | | |
| –40 to 85°C | 16-Pin Plastic DIP | DG405DJ |
| | 16-Pin Narrow SOIC | DG405DY |
| –55 to 125°C | 16-Pin CerDIP | DG405AK/883, 5962-8996101EA |
| | LCC-20 | 5962-89961012A |

## ABSOLUTE MAXIMUM RATINGS

V+ to V– . . . . . 44 V
GND to V– . . . . . 25 V
$V_L$ . . . . . (GND – 0.3 V) to (V+) +0.3 V
Digital Inputs[a] $V_S$, $V_D$ . . . . . (V–) –2 V to (V+ plus 2 V)
or 30 mA, whichever occurs first
Current (Any Terminal) Continuous . . . . . 30 mA
Current, S or D (Pulsed 1 ms 10% duty) . . . . . 100 mA
Storage Temperature (AK, AZ Suffix) . . . . . –65 to 150°C
(DJ, DY Suffix) . . . . . –65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] . . . . . 450 mW
16-Pin CerDIP[d] . . . . . 900 mW
16-Pin SOIC[e] . . . . . 600 mW
LCC-20[f] . . . . . 900 mW

Notes:
a. Signals on $S_X$, $D_X$, or $IN_X$ exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 75°C
e. Derate 7.6 mW/°C above 75°C
f. Derate 13 mW/°C above 75°C

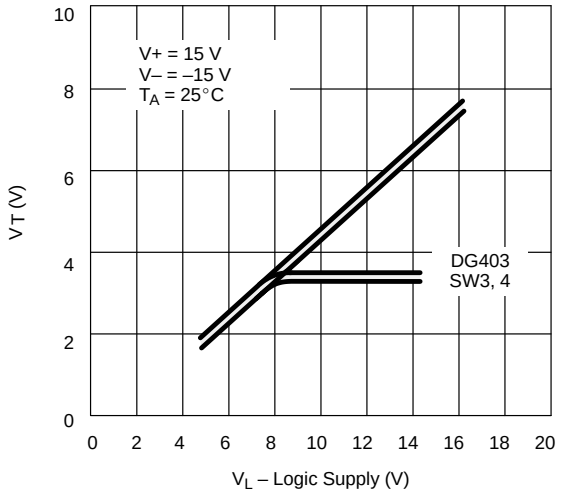
## SPECIFICATIONS[a]

| Parameter | Symbol | Test Conditions Unless Specified<br>V+ = 15 V, V– = –15 V<br>$V_L$ = 5 V, $V_{IN}$ = 2.4 V, 0.8 V[f] | Temp[b] | Typ[c] | A Suffix –55 to 125°C<br>Min[d] | A Suffix –55 to 125°C<br>Max[d] | D Suffix –40 to 85°C<br>Min[d] | D Suffix –40 to 85°C<br>Max[d] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog Signal Range[e] | $V_{ANALOG}$ | | Full | | –15 | 15 | –15 | 15 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $I_S$ = –10 mA, $V_D$ = ±10 V<br>V+ = 13.5 V, V– = –13.5 V | Room<br>Full | 20 | | 35<br>45 | | 45<br>55 | Ω |
| Δ Drain-Source On-Resistance | $\Delta r_{DS(on)}$ | $I_S$ = –10 mA, $V_D$ = ±5 V, 0 V<br>V+ = 16.5 V, V– = –16.5 V | Room<br>Full | 3 | | 3<br>5 | | 3<br>5 | Ω |
| Switch Off Leakage Current | $I_{S(off)}$ | V+ = 16.5, V– = –16.5 V<br>$V_D$ = ±15.5 V, $V_S$ = ∓15.5 V | Room<br>Hot | –0.01 | –0.25<br>–20 | 0.25<br>20 | –0.5<br>–5 | 0.5<br>5 | nA |
| | $I_{D(off)}$ | | Room<br>Hot | –0.01 | –0.25<br>–20 | 0.25<br>20 | –0.5<br>–5 | 0.5<br>5 | |
| Channel On Leakage Current | $I_{D(on)}$ | V+ = 16.5 V, V– = –16.5 V<br>$V_S$ = $V_D$ = ±15.5 V | Room<br>Hot | –0.04 | –0.4<br>–40 | 0.4<br>40 | –1<br>–10 | 1<br>10 | |
| **Digital Control** | | | | | | | | | |
| Input Current $V_{IN}$ Low | $I_{IL}$ | $V_{IN}$ under test = 0.8 V<br>All Other = 2.4 V | Full | 0.005 | –1 | 1 | –1 | 1 | µA |
| Input Current $V_{IN}$ High | $I_{IH}$ | $V_{IN}$ under test = 2.4 V<br>All Other = 0.8 V | Full | 0.005 | –1 | 1 | –1 | 1 | |
| **Dynamic Characteristics** | | | | | | | | | |
| Turn-On Time | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF<br>See Figure 2 | Room | 100 | | 150 | | 150 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room | 60 | | 100 | | 100 | |
| Break-Before-Make Time Delay (DG403) | $t_D$ | $R_L$ = 300 Ω, $C_L$ = 35 pF | Room | 12 | 5 | | 5 | | |
| Charge Injection | Q | $C_L$ = 10,000 pF<br>$V_{gen}$ = 0 V, $R_{gen}$ = 0 Ω | Room | 60 | | | | | pC |
| Off Isolation Reject Ratio | OIRR | $R_L$ = 100 Ω, $C_L$ = 5 pF<br>f = 1 MHz | Room | 72 | | | | | dB |
| Channel-to-Channel Crosstalk | $X_{TALK}$ | | Room | 90 | | | | | |
| Source Off Capacitance | $C_{S(off)}$ | f = 1 MHz, $V_S$ = 0 V | Room | 12 | | | | | pF |
| Drain Off Capacitance | $C_{D(off)}$ | | Room | 12 | | | | | |
| Channel On Capacitance | $C_D$, $C_{S(on)}$ | | Room | 39 | | | | | |
| **Power Supplies** | | | | | | | | | |
| Positive Supply Current | I+ | V+ = 16.5 V, V– = –16.5 V<br>$V_{IN}$ = 0 or 5 V | Room<br>Full | 0.01 | | 1<br>5 | | 1<br>5 | µA |
| Negative Supply Current | I– | | Room<br>Full | –0.01 | –1<br>–5 | | –1<br>–5 | | |
| Logic Supply Current | $I_L$ | | Room<br>Full | 0.01 | | 1<br>5 | | 1<br>5 | |
| Ground Current | $I_{GND}$ | | Room<br>Full | –0.01 | –1<br>–5 | | –1<br>–5 | | |

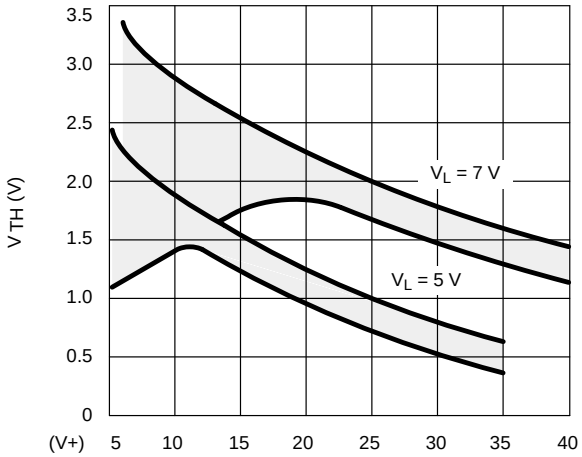
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

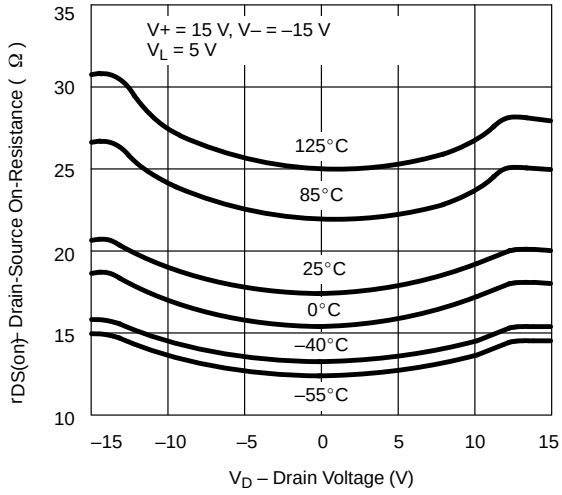
**Input Switching Threshold vs. Logic Supply Voltage**



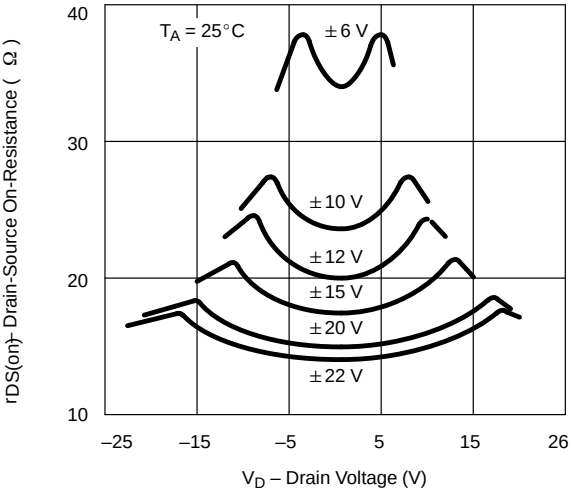

**Input Switching Threshold vs. Supply Voltages**



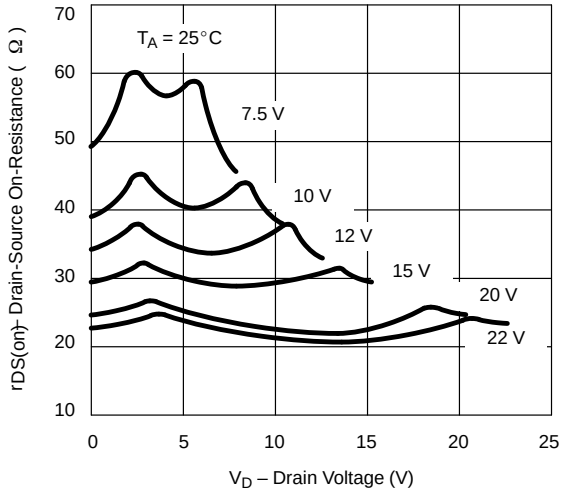

**$r_{DS(on)}$ vs. $V_D$ and Temperature**



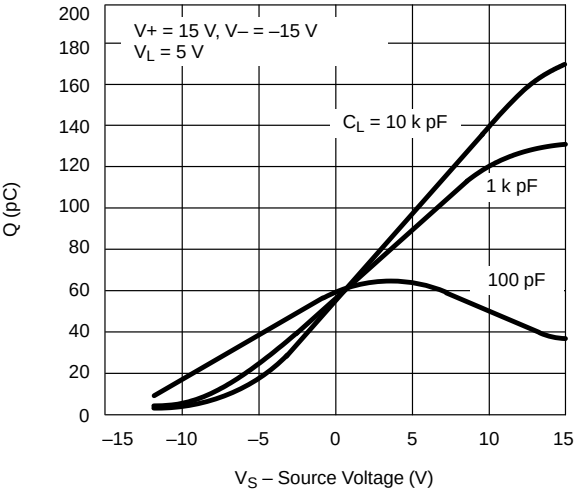

**$r_{DS(on)}$ vs. $V_D$ and Power Supply Voltage**




**$r_{DS(on)}$ vs. $V_D$ and Power Supply Voltage (V– = 0 V)**

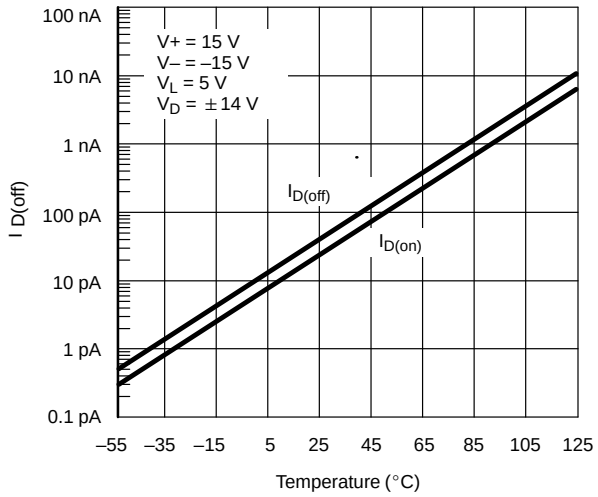



**Charge Injection vs. Analog Voltage**

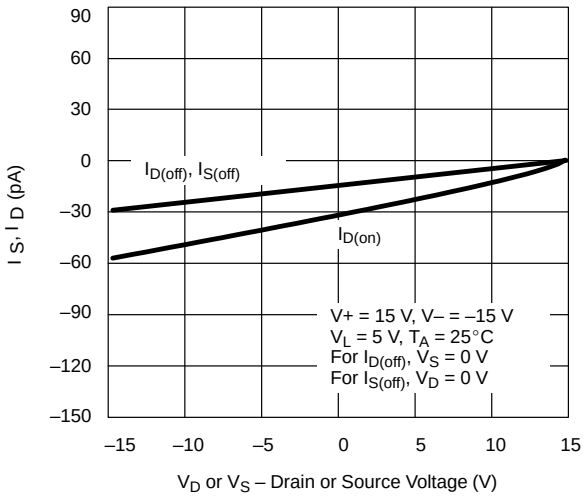


## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

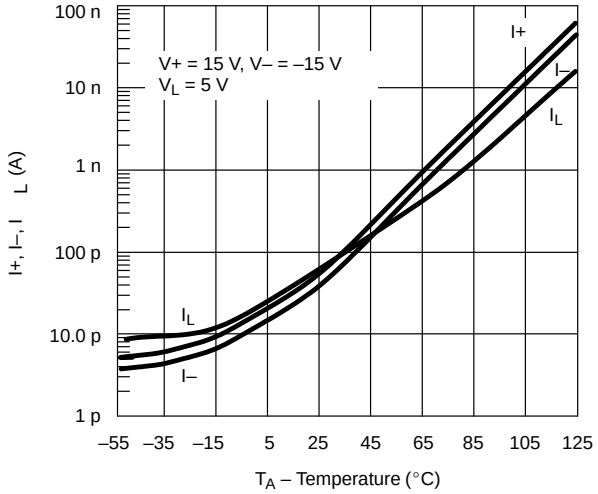
**Leakage Current vs. Temperature**



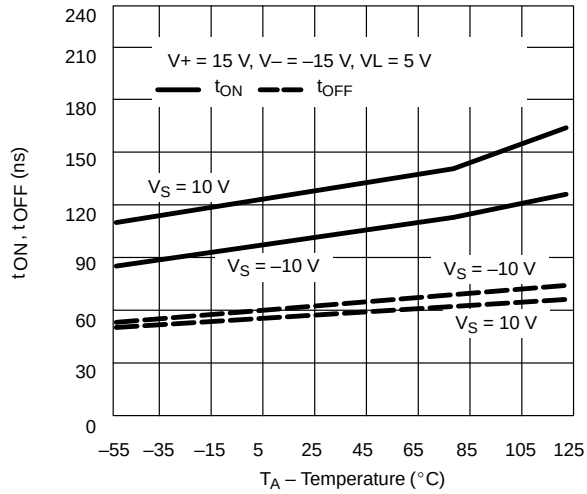

**Leakage Current vs. Analog Voltage**



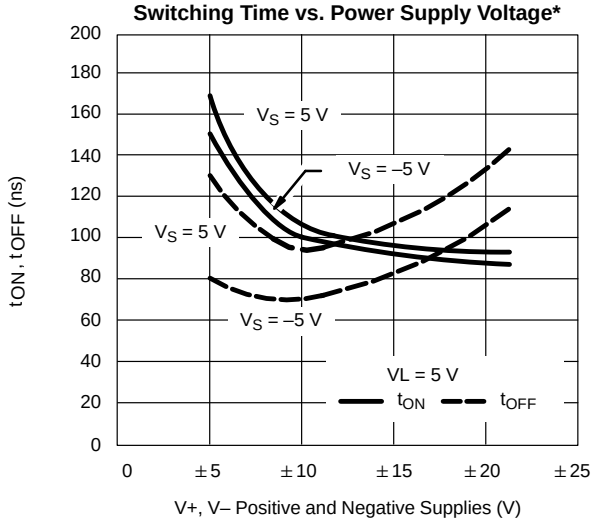

**Supply Current vs. Temperature**



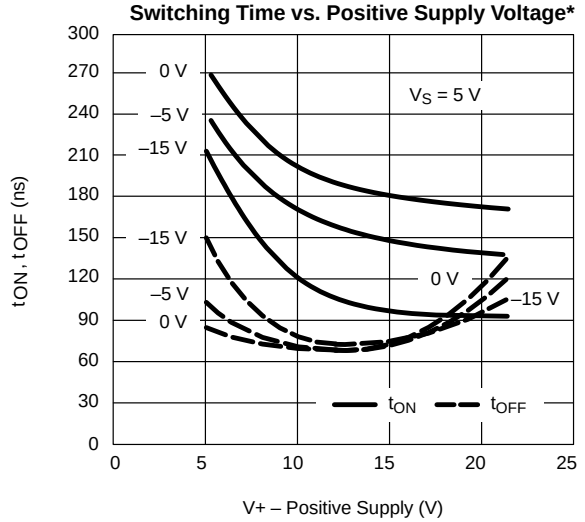

**Switching Time vs. Temperature***




**Switching Time vs. Power Supply Voltage***




**Switching Time vs. Positive Supply Voltage***




*Refer to Figure 2 for test conditions.

## SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

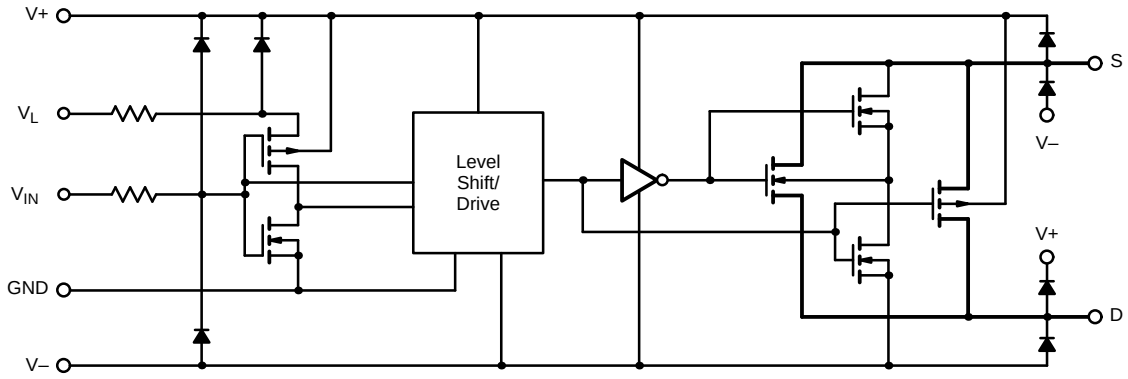
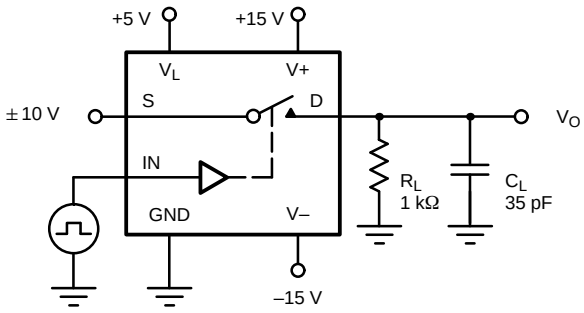



**FIGURE 1.**

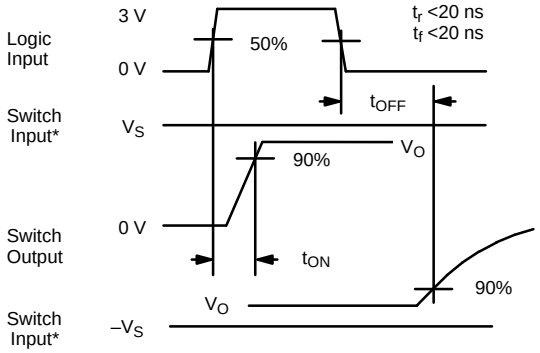
## TEST CIRCUITS

$V_O$ is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.




$C_L$ (includes fixture and stray capacitance)

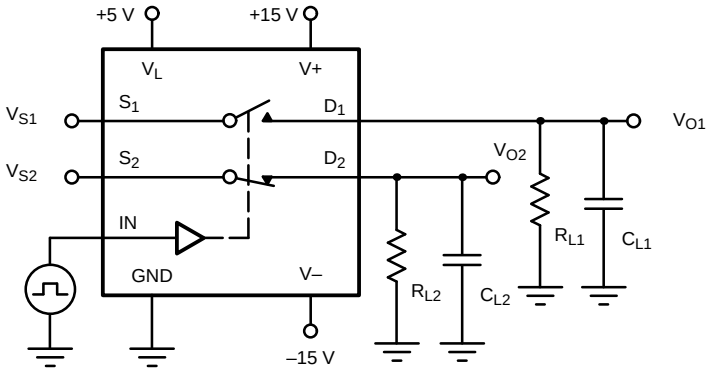
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$




*$V_S$ = 10 V for $t_{ON}$, $V_S$ = –10 V for $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

**FIGURE 2.** Switching Time




$C_L$ (includes fixture and stray capacitance)

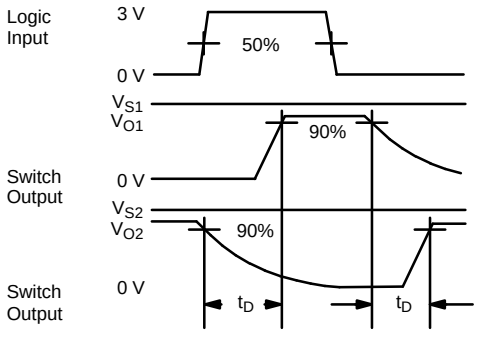
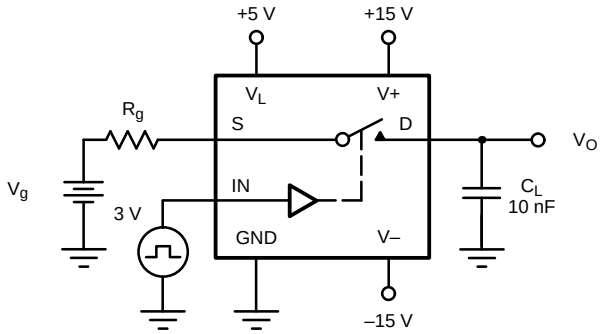



**FIGURE 3.** Break-Before-Make

## TEST CIRCUITS



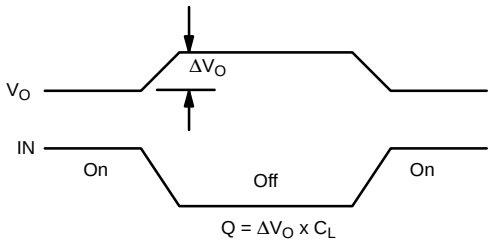




**FIGURE 4.** Charge Injection

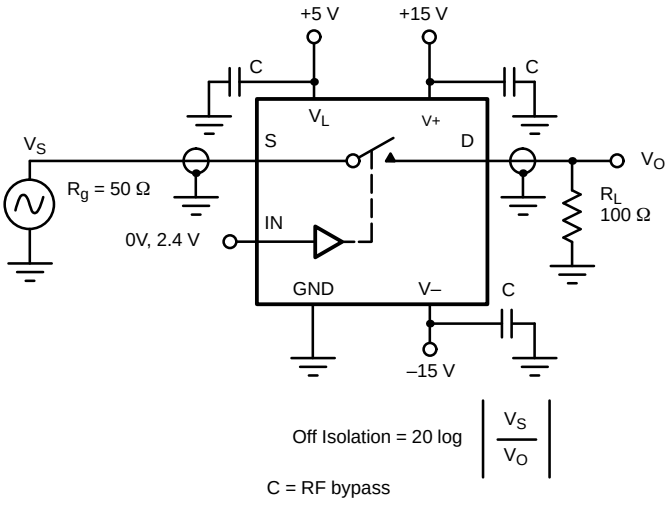



**FIGURE 5.** Off Isolation

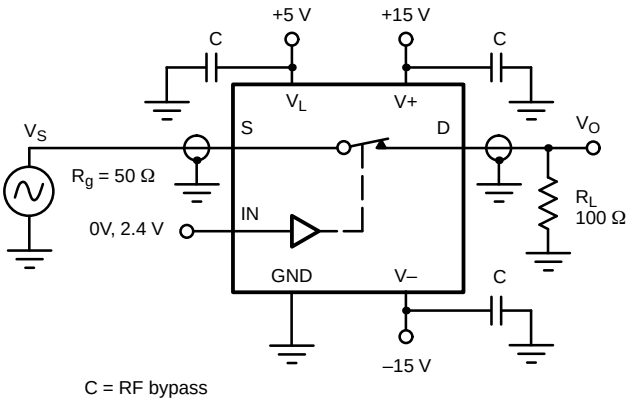



**FIGURE 6.** Insertion Loss

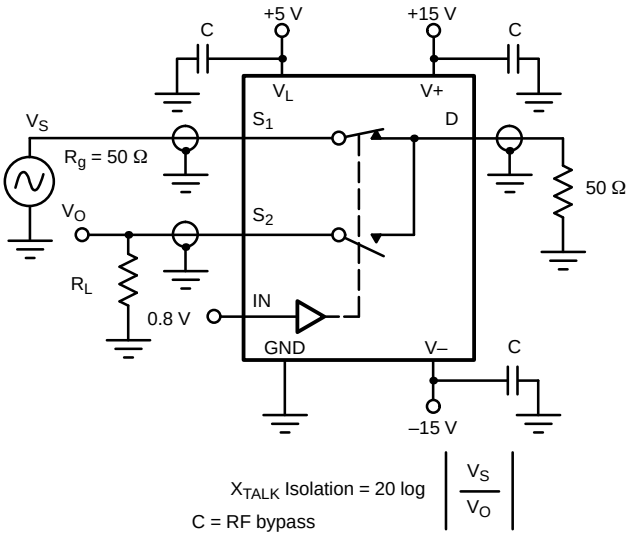



**FIGURE 7.** Crosstalk

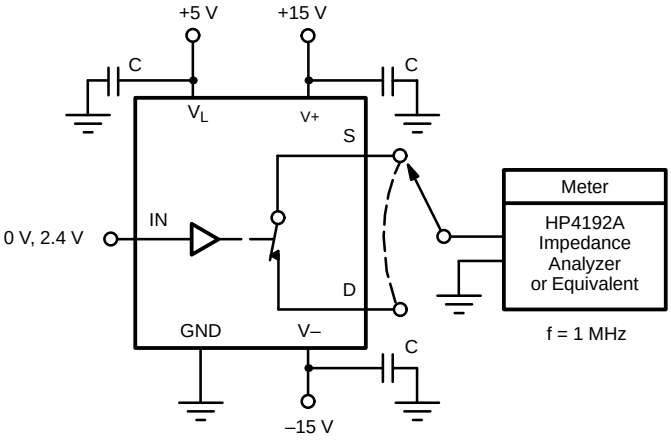



**FIGURE 8.** Capacitances

## APPLICATIONS

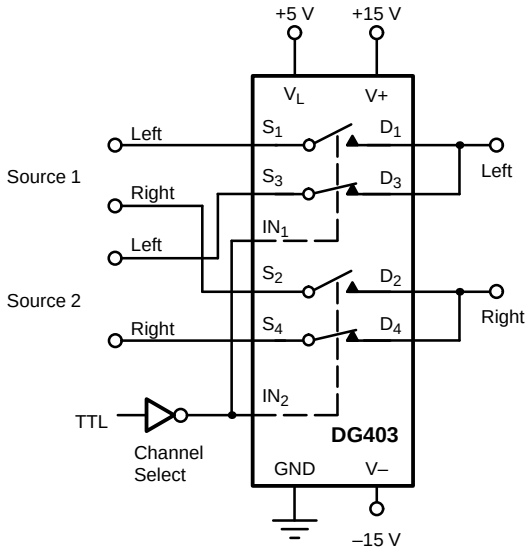



**FIGURE 9.** Stereo Source Selector

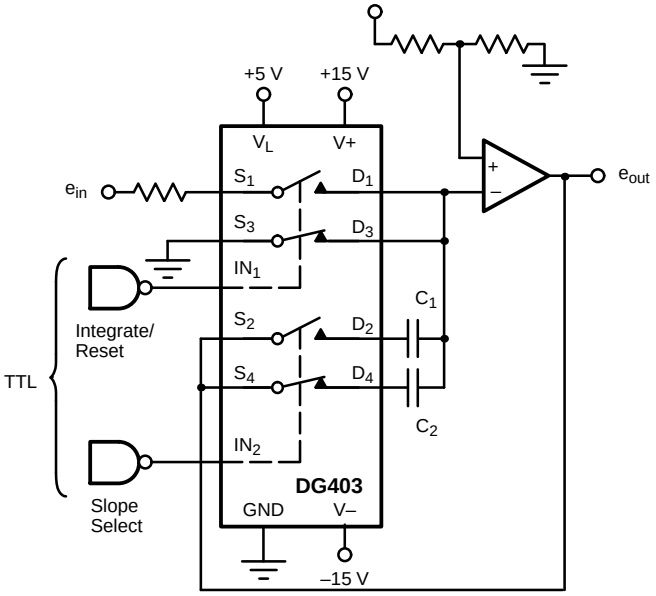



**FIGURE 10.** Dual Slope Integrator

**Dual Slope Integrators:**

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor $C_1$ or $C_2$. Another one selects $e_{in}$ or discharges the capacitor in preparation for the next integration cycle.

**Band-Pass Switched Capacitor Filter:**

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

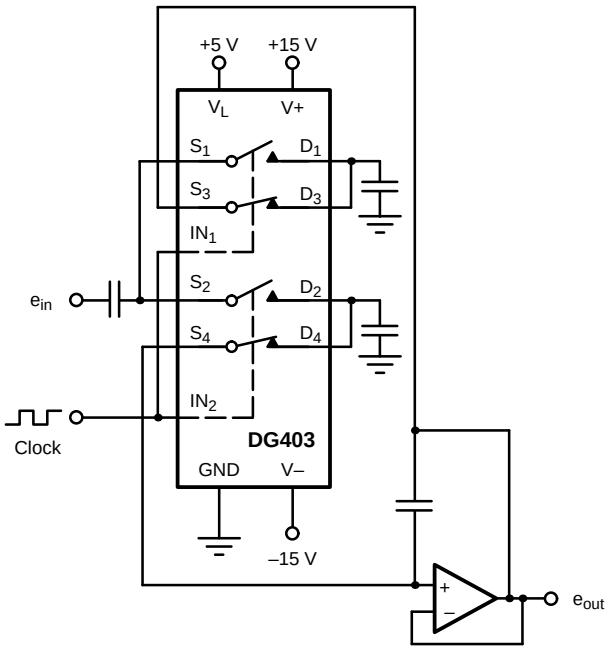



**FIGURE 11.** Band-Pass Switched Capacitor Filter

## APPLICATIONS

# Peak Detector:

$A_3$ acting as a comparator provides the logic drive for operating $SW_1$. The output of $A_2$ is fed back to $A_3$ and compared to the analog input $e_{in}$. If $e_{in} > e_{out}$ the output of $A_3$ is high keeping $SW_1$ closed. This allows $C_1$ to charge up to the analog input voltage. When $e_{in}$ goes below $e_{out}$ $A_3$ goes negative, turning $SW_1$ off. The system will therefore store the most positive analog input experienced.

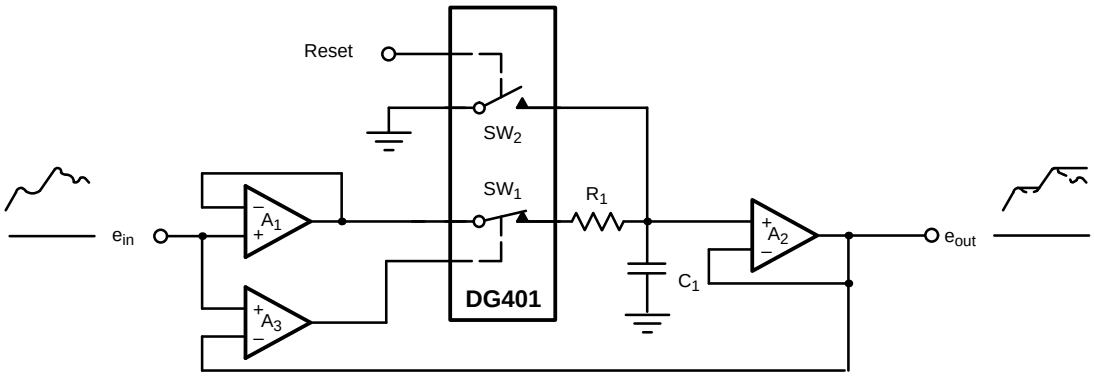



**FIGURE 12.** Positive Peak Detector

# Notice

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