HALOGEN

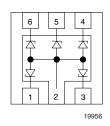
FREE

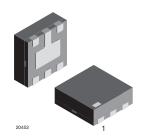
**GREEN** 



### Vishay Semiconductors

## 5-Line ESD Protection Diode Array in LLP75





#### **MARKING** (example only)



Dot = pin 1 marking XX = date code YY = type code (see table below)

#### **DESIGN SUPPORT TOOLS**

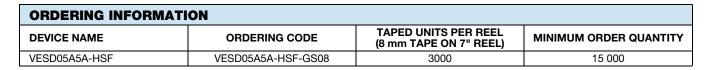
Models

click logo to get started



#### **FEATURES**

- Ultra compact LLP75-6L package
- Low profile < 0.6 mm</li>
- 5-line ESD protection
- Low leakage current  $I_R < 0.1 \mu A$
- Low load capacitance C<sub>D</sub> = 13 pF
- ESD immunity acc. IEC 61000-4-2 ± 15 kV contact discharge ± 15 kV air discharge
- Working voltage range V<sub>RWM</sub> = 5 V
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



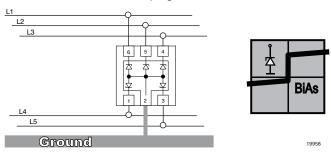
PACKAGE DA	PACKAGE DATA							
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS		
VESD05A5A-HSF	LLP75-6L	AR	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C		

ABSOLUTE MAXI	MUM RATINGS VESD05A5A-HSF				
PARAMETER	TEST CONDITIONS			VALUE	UNIT
Peak pulse current	BiAs-mode: each input (pin 1 to pin 6) to ground (pin acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	- I <sub>PPM</sub>	2.5	Α	
	BiSy-mode: each input (pin 1 to pin 6) to any other input Pin 2 not connected. Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; sing		2.5	Α	
Peak pulse power	BiAs-mode: each input (pin 1 to pin 6) to ground (pin acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	- P <sub>PP</sub>	33	W	
	BiSy-mode: each input (pin 1 - pin 6) to any other input Pin 2 not connected. Acc. IEC 61000-4-5; $t_p$ = 8/20 $\mu$ s; sing		43	W	
ESD immunity	acc. IEC61000-4-2; 10 pulses BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2)	Contact discharge	- V <sub>ESD</sub>	± 15	kV
		Air discharge		± 15	kV
ESD immunity	acc. IEC 61000-4-2; 10 pulses BiSy-mode: each input (pin 1 to pin 6) to any other input pin.		- V <sub>ESD</sub>	± 10	kV
	Pin 2 not connected.	Air discharge	VESD	± 10	kV
Operating temperature	Junction temperature			-40 to +125	°C
Storage temperature				-55 to +150	°C

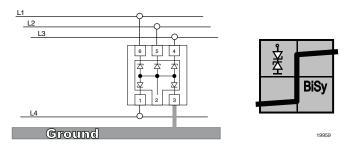


#### **APPLICATION NOTE:**

a. With the VESD05A5A-HSF 5 different signal or data lines can be clamped to ground. Due to the different clamping levels in forward and reverse direction the VESD05A5A-HSF clamping behavior is bidirectional and asymmetrical (BiAs).



b. If symmetrical clamping behaviour is required the VESD05A5A-HSF can also be used as a bidirectional symmetrical protection device protecting up to 4 lines. In this case pin no. 2 must not be connected.



<b>ELECTRICAL CHARACTERISTICS VESD05A5A-HSF</b> (Between pin 1, 3, 4, 5 or 6, and pin 2) (T <sub>amb</sub> = 25 °C, unless otherwise specified)								
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT		
Protection paths	Number of lines which can be protected	N <sub>channel</sub>	-	-	5	lines		
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	5	V		
Reverse voltage	at I <sub>R</sub> = 0.1 μA	$V_{R}$	5	-	-	V		
Max. reverse current	at V <sub>R</sub> = 5 V	I <sub>R</sub>	-	< 0.01	0.1	μΑ		
Reverse breakdown voltage	at I <sub>R</sub> = 1 mA	$V_{BR}$	6	6.7	7.5	V		
Reverse clamping voltage	at I <sub>PP</sub> = 1 A	V <sub>C</sub>	-	9	10	V		
	at I <sub>PP</sub> = I <sub>PPM</sub> = 2.5 A	$V_{C}$	-	12	13	V		
Forward clamping voltage	at I <sub>PP</sub> = 1 A	V <sub>F</sub>	-	2	2.5	V		
	at I <sub>PP</sub> = I <sub>PPM</sub> = 2.5 A	V <sub>F</sub>	-	3.2	4	V		
12	at V <sub>R</sub> = 0 V; f = 1 MHz	C <sub>D</sub>	-	13	15	pF		
Line capacitance	at V <sub>R</sub> = 2.5 V; f = 1 MHz	C <sub>D</sub>	-	8	-	pF		

### TYPICAL CHARACTERISTICS (T<sub>amb</sub> = 25 °C, unless otherwise specified)

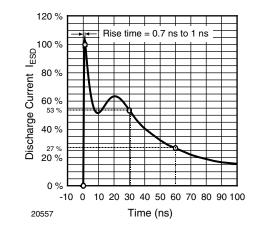


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

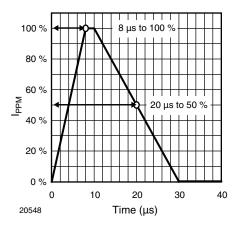


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

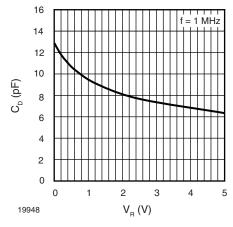


Fig. 3 - Typical Capacitance  $C_{\text{D}}$  vs. Reverse Voltage  $V_{\text{R}}$ 

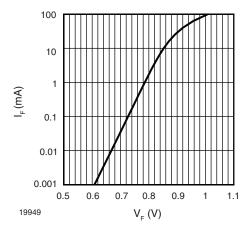


Fig. 4 - Typical Forward Current  $I_{\text{F}}$  vs. Forward Voltage  $V_{\text{F}}$ 

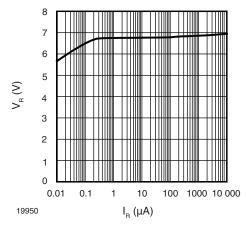


Fig. 5 - Typical Reverse Voltage  $V_{\text{R}}$  vs. Reverse Current  $I_{\text{R}}$ 

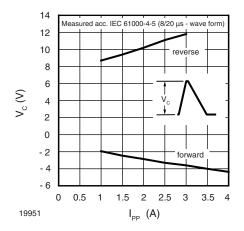


Fig. 6 - Typical Peak Clamping Voltage  $V_{C}$  vs. Peak Pulse Current  $I_{PP}$ 

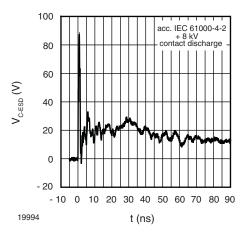


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

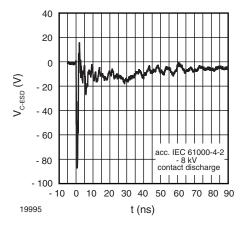


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

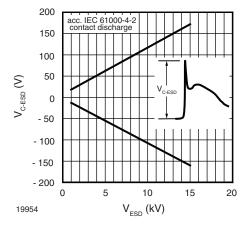
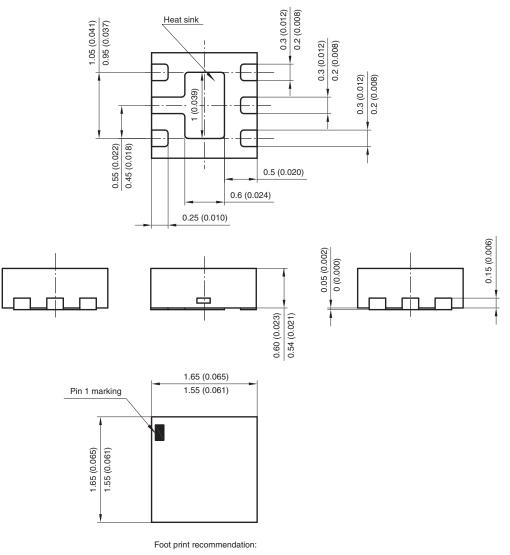
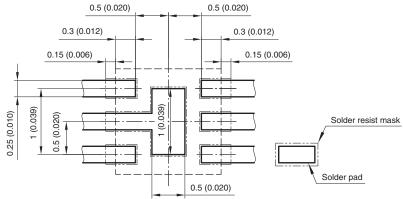


Fig. 9 - Typical max. Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

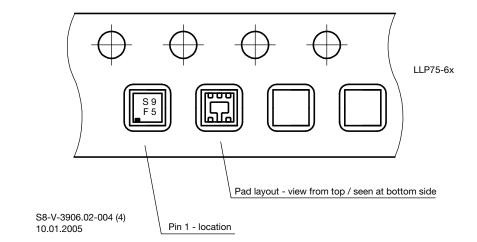
### PACKAGE DIMENSIONS in millimeters (Inches): LLP75-6L





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