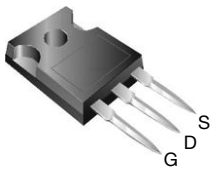
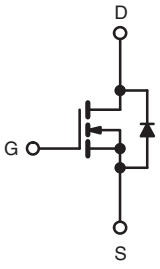
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 500 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.28 |
| $Q_g$ (Max.) (nC) | 130 | |
| $Q_{gs}$ (nC) | 33 | |
| $Q_{gd}$ (nC) | 59 | |
| Configuration | Single | |

TO-247AC




N-Channel MOSFET

## FEATURES

- SuperFast Body Diode Eliminates the Need For External Diodes in ZVS Applications
- Low Gate Charge Results in Simple Drive Requirement
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC

Available

RoHS* COMPLIANT

## APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supply
- Motor Control applications

| ORDERING INFORMATION | |
|---|---|
| Package | TO-247AC |
| Lead (Pb)-free | IRFP17N50LPbF |
| | SiHFP17N50L-E3 |
| SnPb | IRFP17N50L |
| | SiHFP17N50L |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 500 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 16 | A |
| | | $T_C$ = 100 °C | | 11 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 64 | |
| Linear Derating Factor | | | | 1.8 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 390 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | 16 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 22 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 220 | W |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 13 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |
| Mounting Torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting $T_J$ = 25 °C, L = 3.0 mH, $R_g$ = 25 Ω, $I_{AS}$ = 16 A (see fig. 12).
c. $I_{SD}$ ≤ 16 A, dI/dt ≤ 347 A/µs, $V_{DD}$ ≤ $V_{DS}$, $T_J$ ≤ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply



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| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 62 | °C/W |
| Case-to-Sink, Flat, Greased Surface | $R_{thCS}$ | 0.50 | - | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 0.56 | |

**SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | | 500 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA[d] | | - | 0.60 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 3.0 | - | 5.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | | - | - | 50 | µA |
| | | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 2.0 | mA |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 9.9 A[b] | - | 0.28 | 0.32 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 9.9 A[b] | | 11 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 2760 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 325 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 37 | - | |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | $V_{DS}$ = 1.0 V , f = 1.0 MHz | - | 3690 | - | |
| | | | $V_{DS}$ = 400 V , f = 1.0 MHz | - | 84 | - | |
| Effective Output Capacitance | $C_{oss}$ eff. | | $V_{DS}$ = 0 V to 400 V | - | 159 | - | |
| Effective Output Capacitance (Energy Related) | $C_{oss}$ eff. (ER) | | | - | 120 | - | |
| Internal Gate Resistance | $R_g$ | f = 1 MHz, open drain | | - | 1.4 | - | Ω |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V | $I_D$ = 16 A, $V_{DS}$ = 400 V see fig. 7 and 15[b] | - | - | 130 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 33 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 59 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 250 V, $I_D$ = 16 A, $R_G$ = 7.5 Ω, $V_{GS}$ = 10 V see fig. 14a and 14b[b] | | - | 21 | - | ns |
| Rise Time | $t_r$ | | | - | 51 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 50 | - | |
| Fall Time | $t_f$ | | | - | 28 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode |  | - | - | 16 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 64 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 16 A, $V_{GS}$ = 0 V[b] | | - | - | 1.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C | $I_F$ = 16 A, dI/dt = 100 A/µs[b] | - | 170 | 250 | ns |
| | | $T_J$ = 125 °C | | - | 220 | 330 | |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | $T_J$ = 25 °C | | - | 470 | 710 | µC |
| | | $T_J$ = 125 °C | | - | 810 | 1210 | |
| Reverse Recovery Current | $I_{RRM}$ | $T_J$ = 25 °C | | - | 7.3 | 11 | |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. $C_{OSS}$ eff. is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising fom 0 % to 80 % $V_{DS}$.
$C_{OSS}$ eff. (ER) is a fixed capacitance that stores the same energy as $C_{OSS}$ while $V_{DS}$ is rising fom 0 % to 80 % $V_{DS}$.




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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

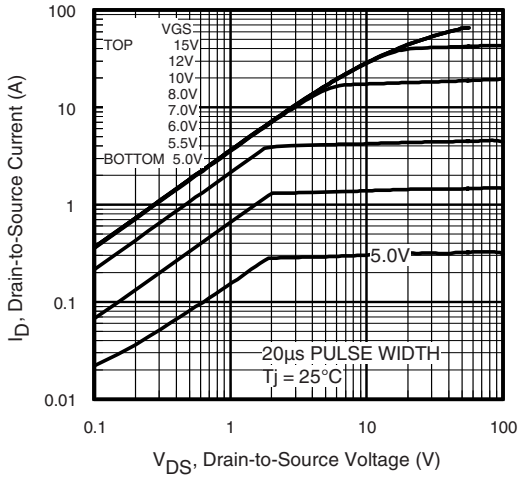


**Fig. 1 - Typical Output Characteristics**

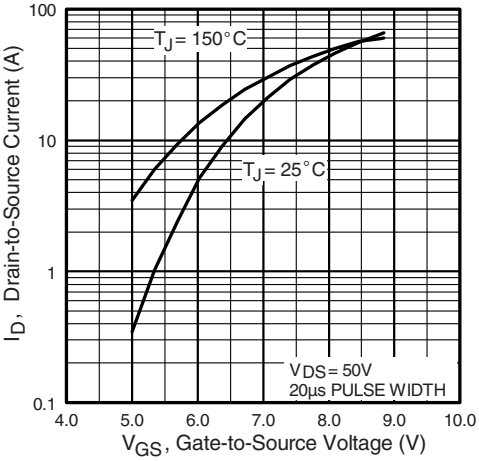


**Fig. 3 - Typical Transfer Characteristics**

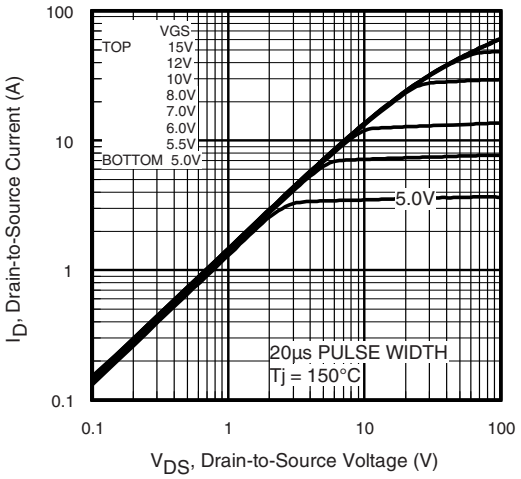


**Fig. 2 - Typical Output Characteristics**

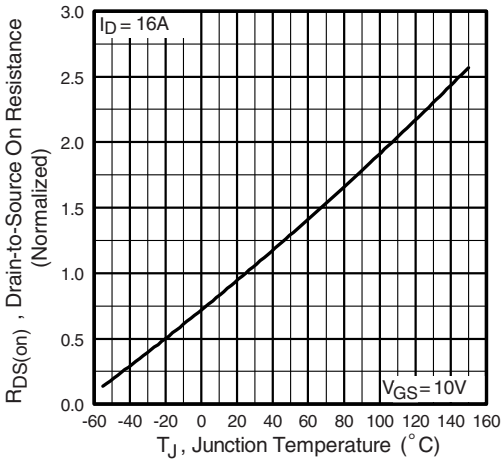


**Fig. 4 - Normalized On-Resistance vs. Temperature**



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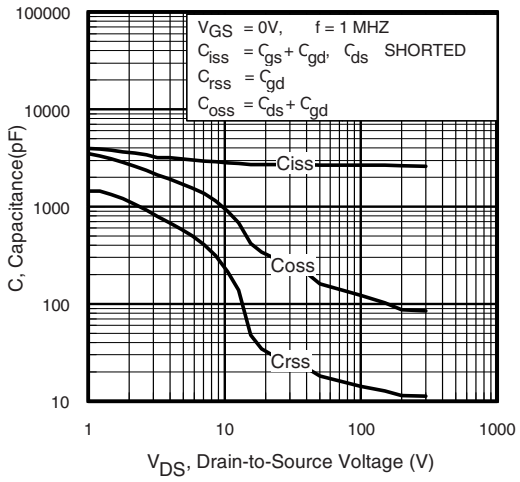


**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

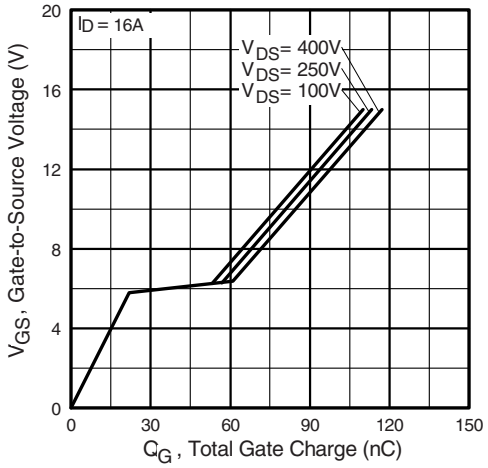


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

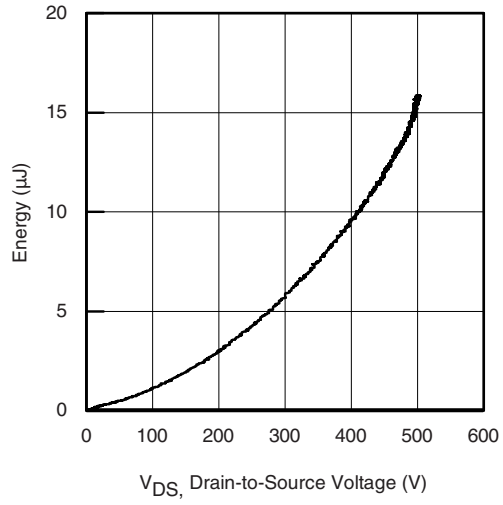


**Fig. 6 - Typ. Output Capacitance Stored Energy vs. $V_{DS}$**

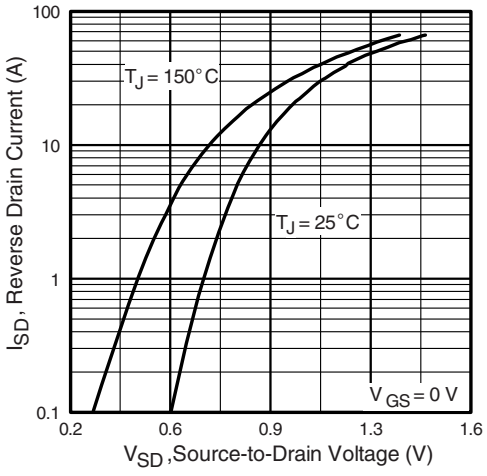


**Fig. 8 - Typical Source-Drain Diode Forward Voltage**




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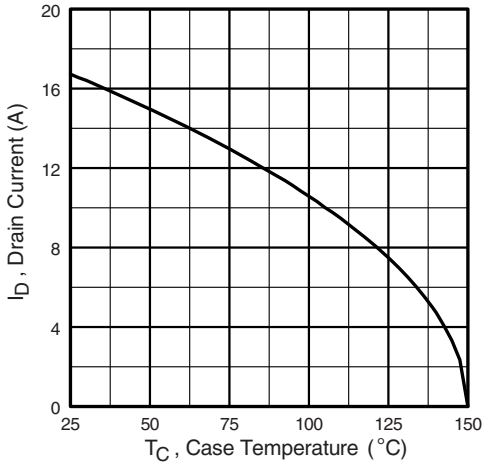


**Fig. 9 - Maximum Drain Current vs. Case Temperature**

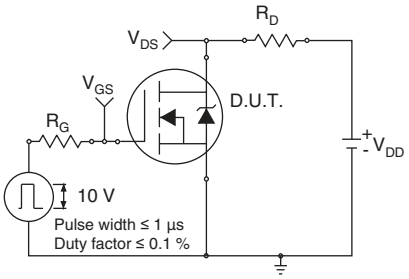


**Fig. 10a - Switching Time Test Circuit**

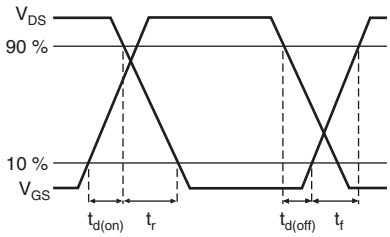


**Fig. 10b - Switching Time Waveforms**

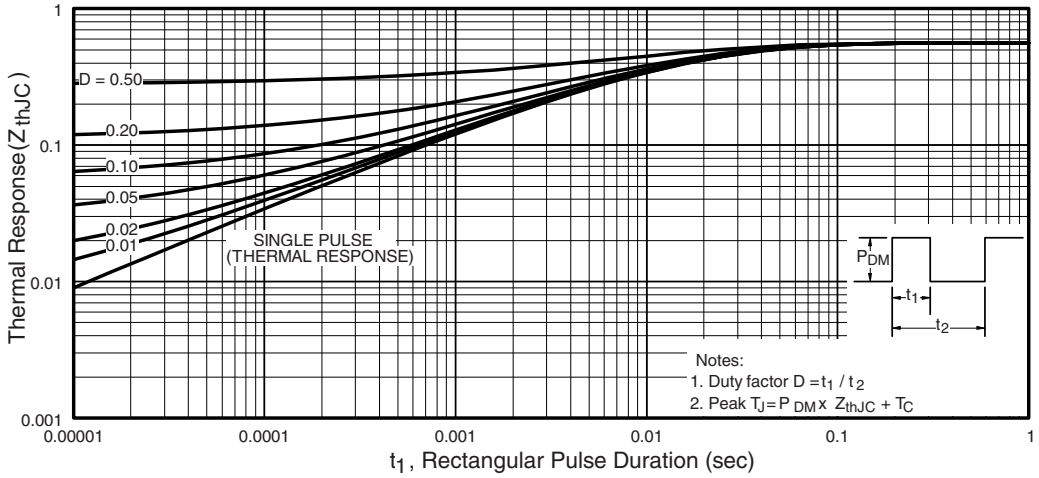


**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



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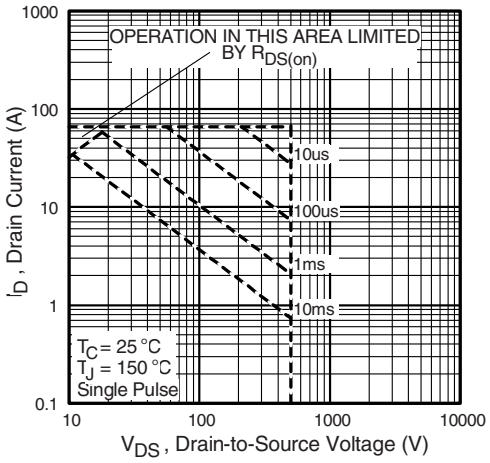


**Fig. 12 - Maximum Safe Operating Area**

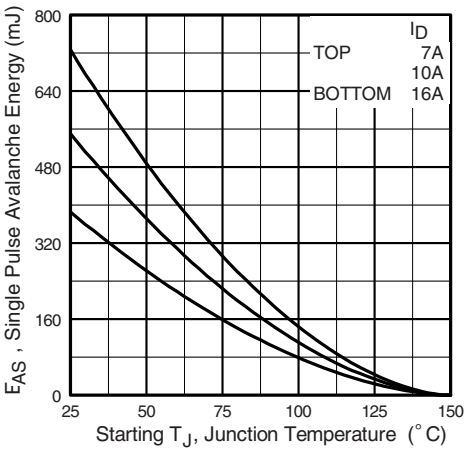


**Fig. 13 - Maximum Avalanche Energy vs. Drain Current**

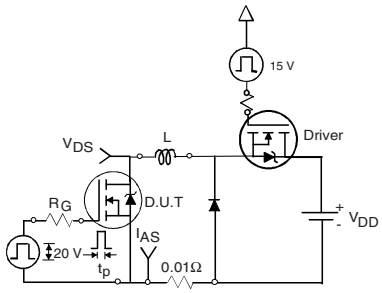


**Fig. 14a - Unclamped Inductive Test Circuit**

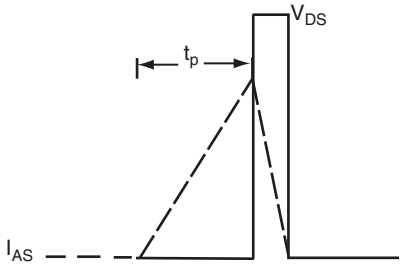


**Fig. 14b - Unclamped Inductive Waveforms**

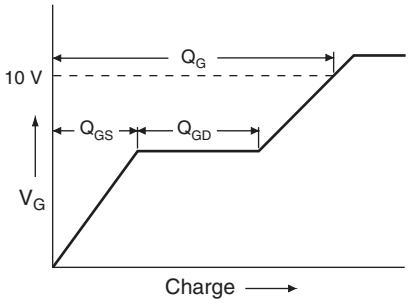


**Fig. 15a - Basic Gate Charge Waveform**

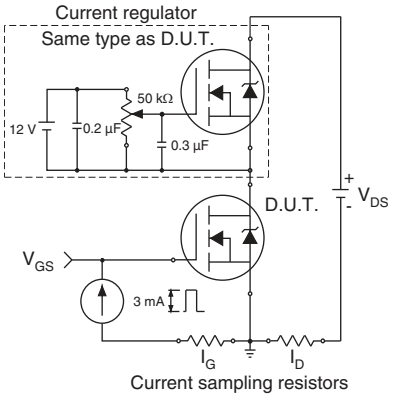


**Fig. 15b - Gate Charge Test Circuit**




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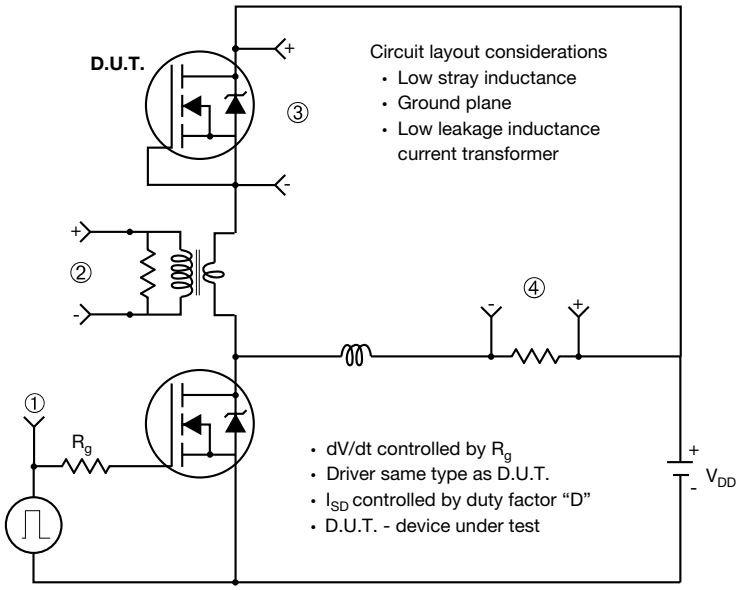
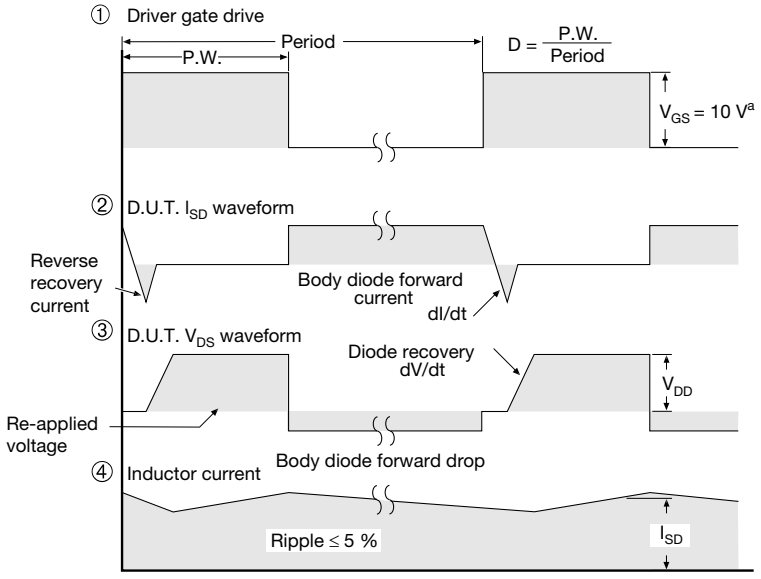
**Peak Diode Recovery dV/dt Test Circuit**




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 16. For N-Channel**

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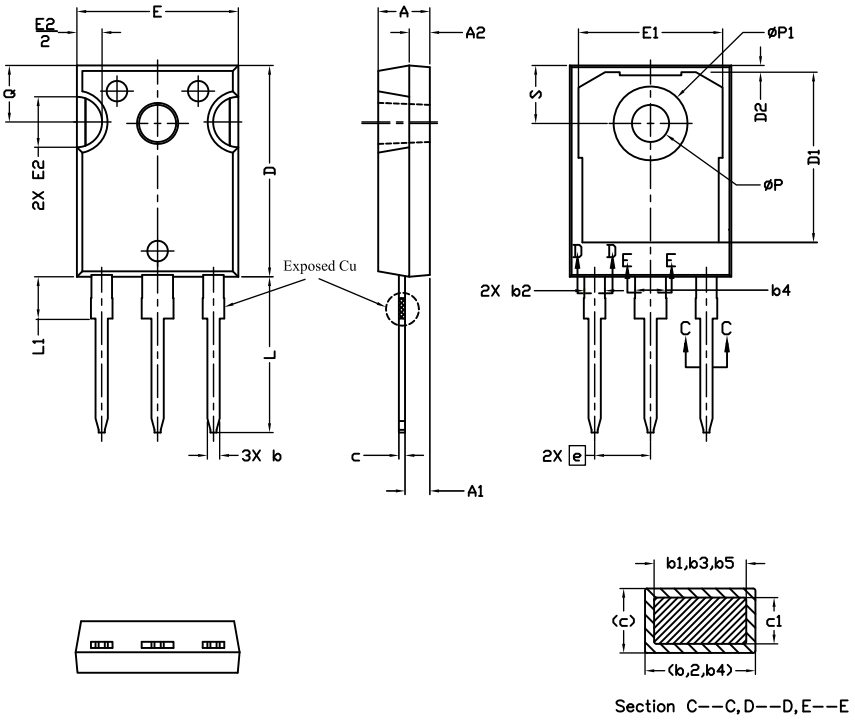
# TO-247AC (High Voltage)

## VERSION 1: FACILITY CODE = 9









Section C--C, D--D, E--E

| | MILLIMETERS | | |
|---|---|---|---|
| DIM. | MIN. | MAX. | NOTES |
| A | 4.83 | 5.21 | |
| A1 | 2.29 | 2.55 | |
| A2 | 1.50 | 2.49 | |
| b | 1.12 | 1.33 | |
| b1 | 1.12 | 1.28 | |
| b2 | 1.91 | 2.39 | 6 |
| b3 | 1.91 | 2.34 | |
| b4 | 2.87 | 3.22 | 6, 8 |
| b5 | 2.87 | 3.18 | |
| c | 0.55 | 0.69 | 6 |
| c1 | 0.55 | 0.65 | |
| D | 20.40 | 20.70 | 4 |

| | MILLIMETERS | | |
|---|---|---|---|
| DIM. | MIN. | MAX. | NOTES |
| D1 | 16.25 | 16.85 | 5 |
| D2 | 0.56 | 0.76 | |
| E | 15.50 | 15.87 | 4 |
| E1 | 13.46 | 14.16 | 5 |
| E2 | 4.52 | 5.49 | 3 |
| e | 5.44 BSC | | |
| L | 14.90 | 15.40 | |
| L1 | 3.96 | 4.16 | 6 |
| Ø P | 3.56 | 3.65 | 7 |
| Ø P1 | 7.19 ref. | | |
| Q | 5.31 | 5.69 | |
| S | 5.54 | 5.74 | |

**Notes**

(1) Package reference: JEDEC® TO247, variation AC
(2) All dimensions are in mm
(3) Slot required, notch may be rounded
(4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
(5) Thermal pad contour optional with dimensions D1 and E1
(6) Lead finish uncontrolled in L1
(7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
(8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



For technical questions, contact: hvm@vishay.com

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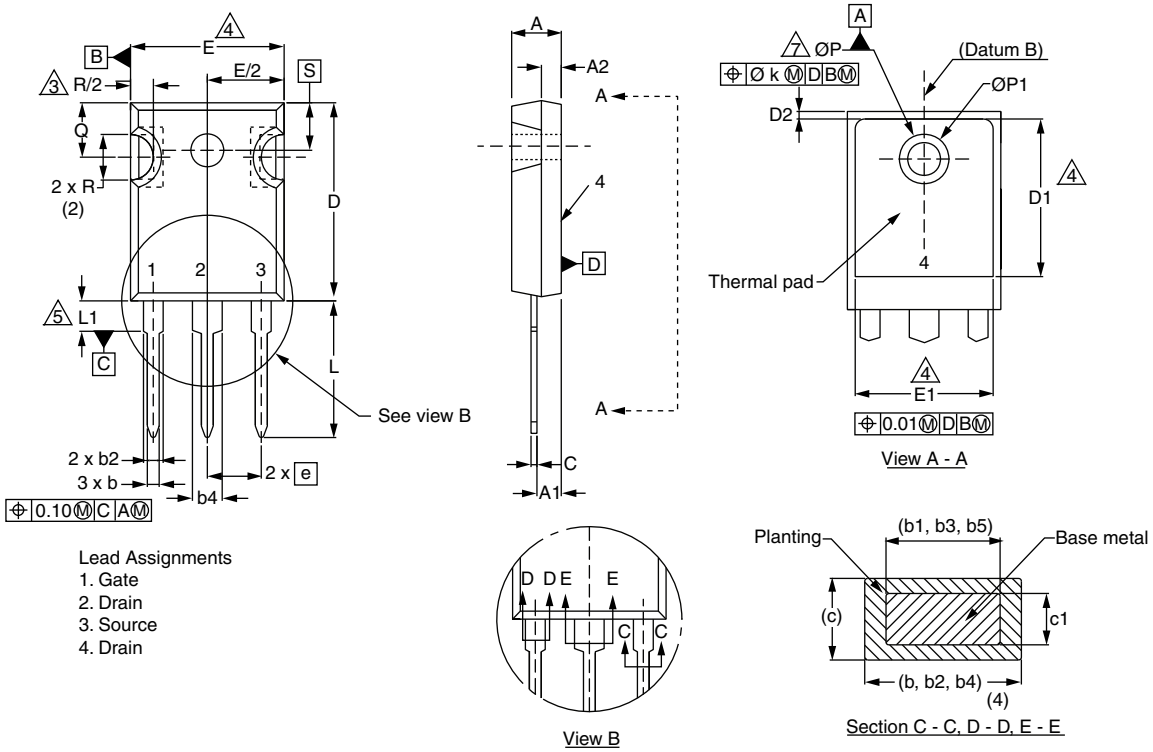
## VERSION 2: FACILITY CODE = Y




Lead Assignments
1. Gate
2. Drain
3. Source
4. Drain

| | MILLIMETERS | | |
|---|---|---|---|
| DIM. | MIN. | MAX. | NOTES |
| A | 4.58 | 5.31 | |
| A1 | 2.21 | 2.59 | |
| A2 | 1.17 | 2.49 | |
| b | 0.99 | 1.40 | |
| b1 | 0.99 | 1.35 | |
| b2 | 1.53 | 2.39 | |
| b3 | 1.65 | 2.37 | |
| b4 | 2.42 | 3.43 | |
| b5 | 2.59 | 3.38 | |
| c | 0.38 | 0.86 | |
| c1 | 0.38 | 0.76 | |
| D | 19.71 | 20.82 | |
| D1 | 13.08 | - | |

| | MILLIMETERS | | |
|---|---|---|---|
| DIM. | MIN. | MAX. | NOTES |
| D2 | 0.51 | 1.30 | |
| E | 15.29 | 15.87 | |
| E1 | 13.72 | - | |
| e | 5.46 BSC | | |
| Ø k | 0.254 | | |
| L | 14.20 | 16.25 | |
| L1 | 3.71 | 4.29 | |
| Ø P | 3.51 | 3.66 | |
| Ø P1 | - | 7.39 | |
| Q | 5.31 | 5.69 | |
| R | 4.52 | 5.49 | |
| S | 5.51 BSC | | |
| | | | |

**Notes**

(1) Dimensioning and tolerancing per ASME Y14.5M-1994
(2) Contour of slot optional
(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
(4) Thermal pad contour optional with dimensions D1 and E1
(5) Lead finish uncontrolled in L1
(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
(7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



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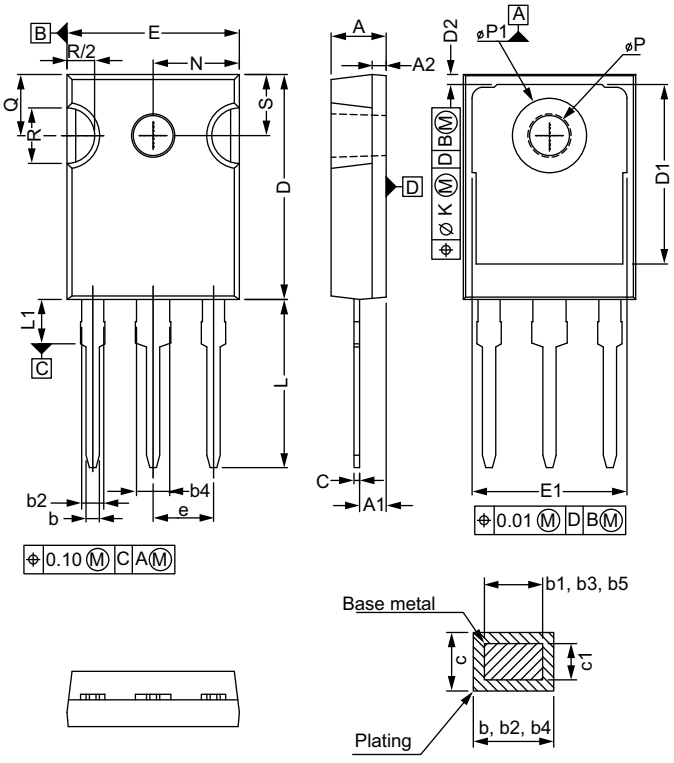
## VERSION 3: FACILITY CODE = N




| | MILLIMETERS | |
|---|---|---|
| DIM. | MIN. | MAX. |
| A | 4.65 | 5.31 |
| A1 | 2.21 | 2.59 |
| A2 | 1.17 | 1.37 |
| b | 0.99 | 1.40 |
| b1 | 0.99 | 1.35 |
| b2 | 1.65 | 2.39 |
| b3 | 1.65 | 2.34 |
| b4 | 2.59 | 3.43 |
| b5 | 2.59 | 3.38 |
| c | 0.38 | 0.89 |
| c1 | 0.38 | 0.84 |
| D | 19.71 | 20.70 |
| D1 | 13.08 | - |

| | MILLIMETERS | |
|---|---|---|
| DIM. | MIN. | MAX. |
| D2 | 0.51 | 1.35 |
| E | 15.29 | 15.87 |
| E1 | 13.46 | - |
| e | 5.46 BSC | |
| k | 0.254 | |
| L | 14.20 | 16.10 |
| L1 | 3.71 | 4.29 |
| N | 7.62 BSC | |
| P | 3.56 | 3.66 |
| P1 | - | 7.39 |
| Q | 5.31 | 5.69 |
| R | 4.52 | 5.49 |
| S | 5.51 BSC | |

ECN: E20-0545-Rev. F, 19-Oct-2020
DWG: 5971

**Notes**

(1) Dimensioning and tolerancing per ASME Y14.5M-1994
(2) Contour of slot optional
(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
(4) Thermal pad contour optional with dimensions D1 and E1
(5) Lead finish uncontrolled in L1
(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



For technical questions, contact: hvm@vishay.com
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