International Rectifier

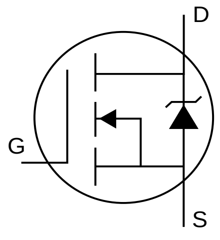
PD - 9.1697

PRELIMINARY

IRL3402

HEXFET® Power MOSFET

- Advanced Process Technology
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching



V_{DSS} = 20V

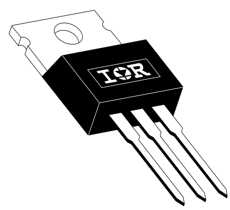
$R_{DS(on)}$ = 0.01Ω

I_D = 85A⑤

Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

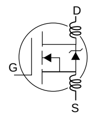
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 5.0V	85⑤	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 5.0V	54	
I_{DM}	Pulsed Drain Current ①	340	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
V_{GSM}	Gate-to-Source Voltage (Start Up Transient, tp = 100µs)	14	V
E_{AS}	Single Pulse Avalanche Energy②	290	mJ
I_{AR}	Avalanche Current①	51	A
E_{AR}	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

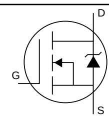
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

10/31/97

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.02	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.010	Ω	V_{GS} = 4.5V, I_D = 51A ④
		——	——	0.008		V_{GS} = 7.0V, I_D = 51A ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	——	——	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	65	——	——	S	V_{DS} = 10V, I_D = 51A
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 20V, V_{GS} = 0V
		——	——	250		V_{DS} = 16V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 10V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -10V
Q_g	Total Gate Charge	——	——	78	nC	I_D = 51A
Q_{gs}	Gate-to-Source Charge	——	——	18		V_{DS} = 10V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	30		V_{GS} = 4.5V, See Fig. 6 ④
$t_{d(on)}$	Turn-On Delay Time	——	10	——	ns	V_{DD} = 10V
t_r	Rise Time	——	140	——		I_D = 51A
$t_{d(off)}$	Turn-Off Delay Time	——	80	——		R_G = 5.0Ω, V_{GS} = 4.5V
t_f	Fall Time	——	120	——		R_D = 0.19Ω, ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	——	7.5	——		from package and center of die contact
C_{iss}	Input Capacitance	——	3300	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	1400	——		V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	——	510	——		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	85⑤	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	340		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 51A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	72	110	ns	T_J = 25°C, I_F = 51A
Q_{rr}	Reverse RecoveryCharge	——	160	240	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 220µH R_G = 25Ω, I_{AS} = 51A.

③ $I_{SD} \leq$ 51A, di/dt ≤ 82A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

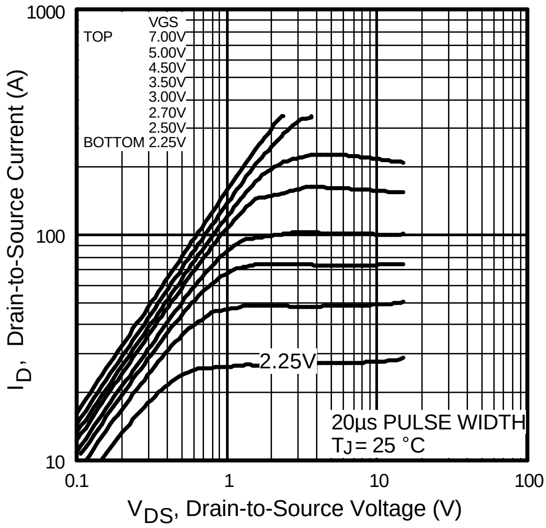


Fig 1. Typical Output Characteristics

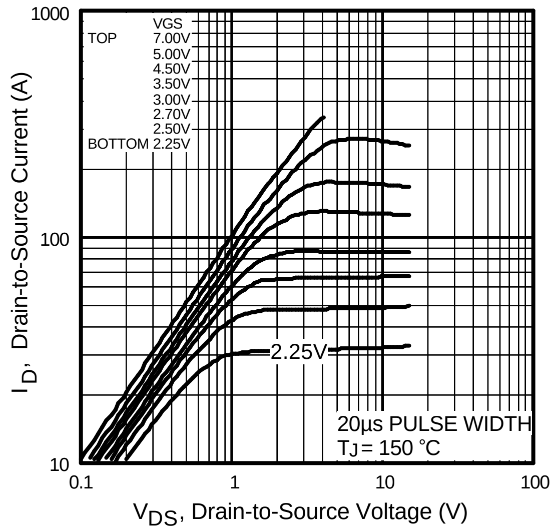


Fig 2. Typical Output Characteristics

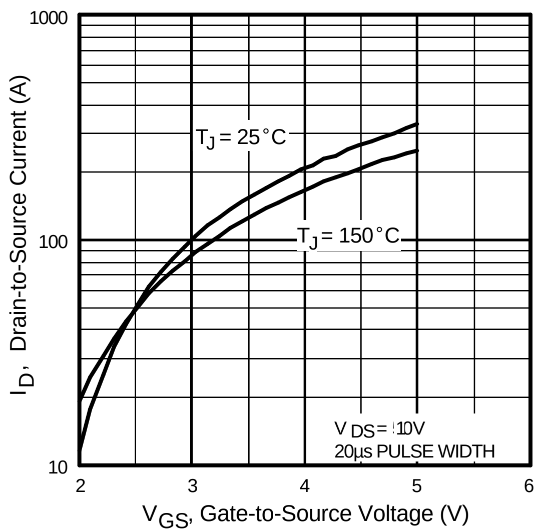


Fig 3. Typical Transfer Characteristics

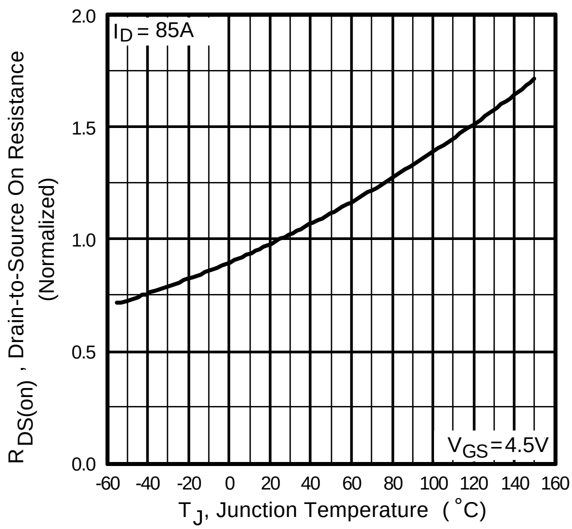


Fig 4. Normalized On-Resistance Vs. Temperature

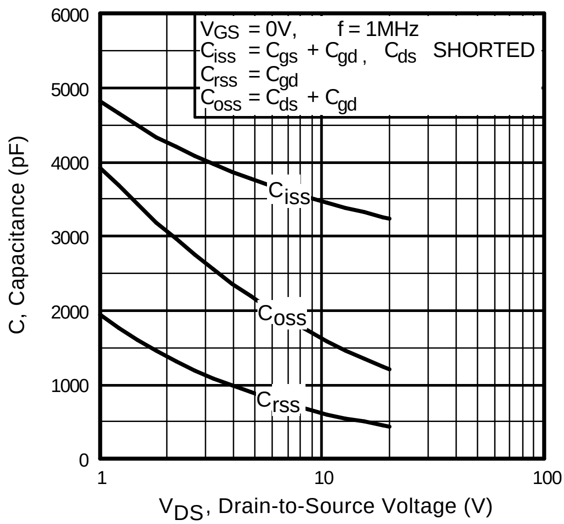


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

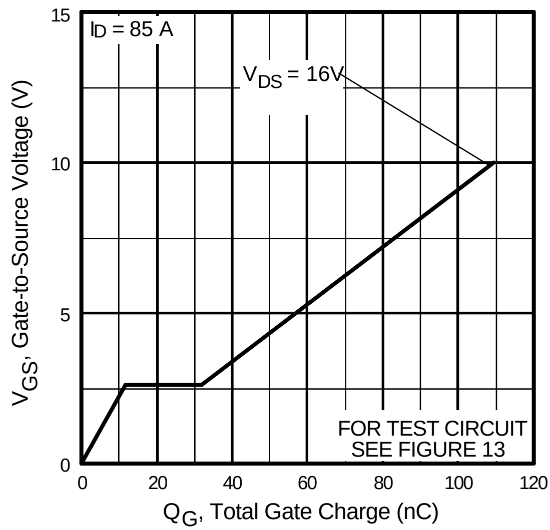


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

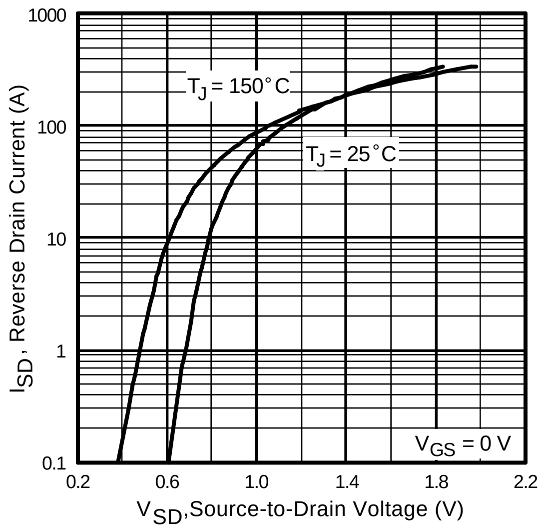


Fig 7. Typical Source-Drain Diode Forward Voltage

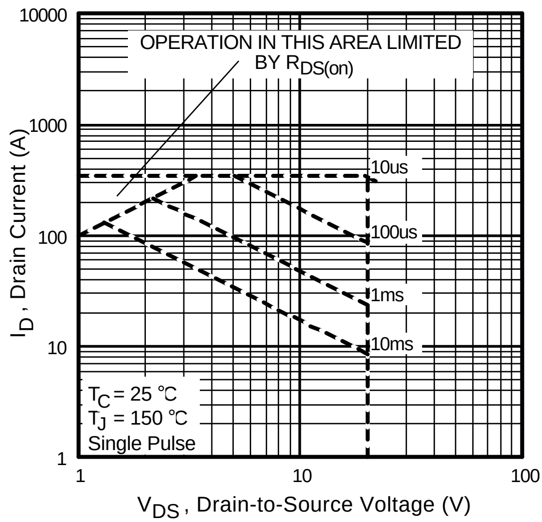


Fig 8. Maximum Safe Operating Area

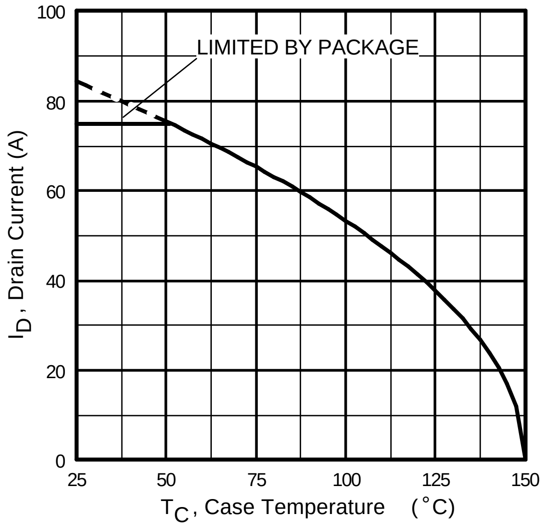


Fig 9. Maximum Drain Current Vs. Case Temperature

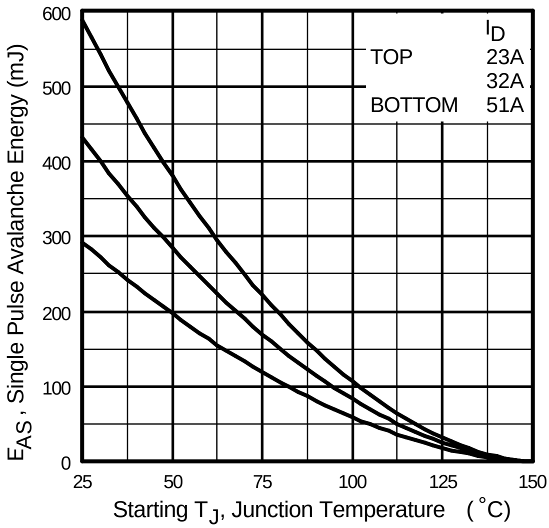


Fig 10. Maximum Avalanche Energy Vs. Drain Current

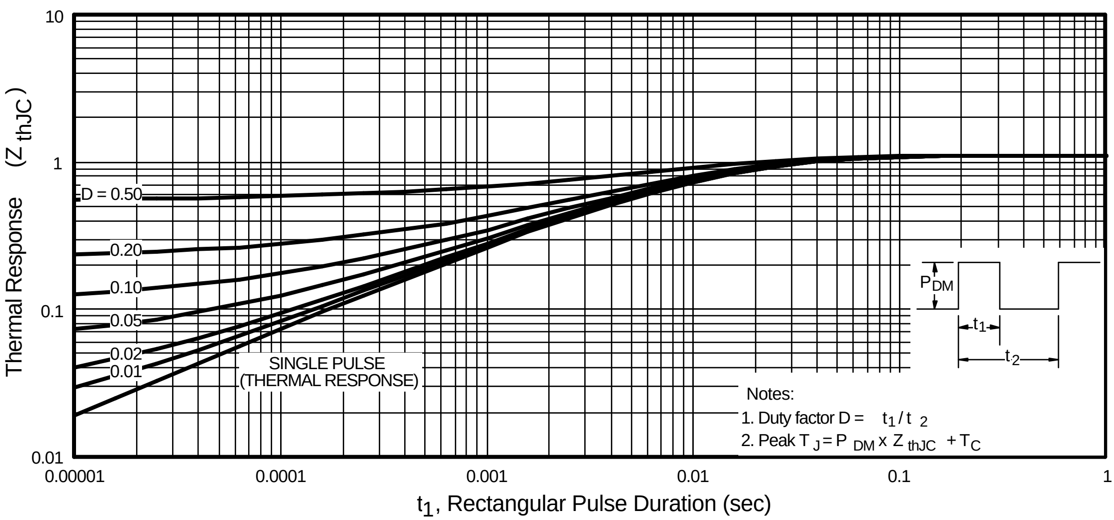


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

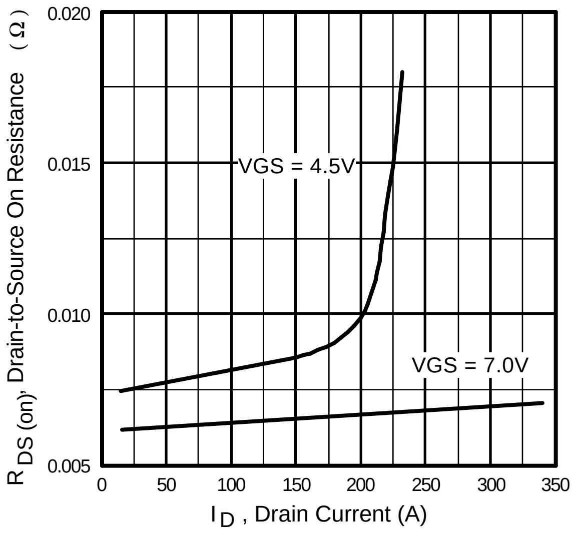


Fig 12. On-Resistance Vs. Drain Current

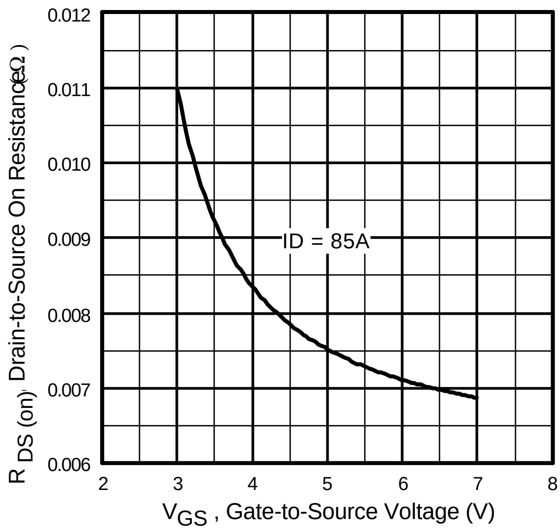
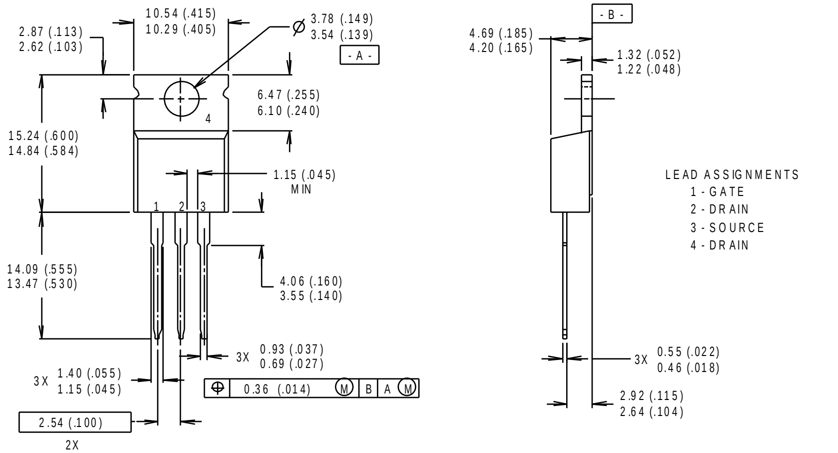


Fig 13. On-Resistance Vs. Gate Voltage

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)

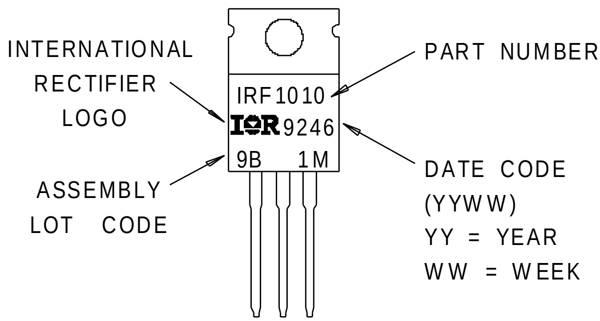


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010 WITH ASSEMBLY LOT CODE 9B1M



International
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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
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http://www.irf.com/   *Data and specifications subject to change without notice.*   *10/97*

单击下面可查看定价，库存，交付和生命周期等信息

[>>Vishay(威世)]