HALOGEN

FREE





Complementary N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
	V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (mA)		
		$0.70 \text{ at V}_{GS} = 4.5 \text{ V}$	600		
N-Channel	20	0.85 at V _{GS} = 2.5 V	500		
		1.25 at V _{GS} = 1.8 V	350		
		1.2 at V _{GS} = - 4.5 V	- 400		
P-Channel	- 20	1.6 at V _{GS} = - 2.5 V	- 300		
		2.7 at V _{GS} = - 1.8 V	- 150		

SOT-563 SC-89 D₁ 5 G_2 Marking Code: A S₂ D_2 Top View

Ordering Information: Si1016X-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 **Definition**
- TrenchFET® Power MOSFETs
- 2000 V ESD Protection
- Very Small Footprint
- High-Side Switching
- Low On-Resistance: N-Channel, 0.7Ω P-Channel, 1.2 Ω
- Low Threshold: ± 0.8 V (Typ.)
- Fast Switching Speed: 14 ns
- 1.8 V Operation
- Compliant to RoHS Directive 2002/95/EC

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- **High-Speed Circuits**
- Low Battery Voltage Operation

APPLICATIONS

- Replace Digital Transistor, Level-Shifter
- **Battery Operated Systems**
- Power Supply Converter Circuits

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)							
			N-Channel		P-Channel		
Parameter		Symbol	5 s	Steady State	5 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		- 20		V
Gate-Source Voltage		V_{GS}	± 6]
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	I _D	515	485	- 390	- 370	A
	T _A = 85 °C		370	350	- 280	- 265	
Pulsed Drain Current ^b		I _{DM}	650		- 650		mA
Continuous Source Current (Diode Conduction) ^a		I _S	450	380	- 450	- 380	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	280	250	280	250	- mW
waximum Fower Dissipation	T _A = 85 °C		145	130	145	130	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000				V

- a. Surface mounted on FR4 board.
- b. Pulse width limited by maximum junction temperature.

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Test Conditions		Min.	Тур.	Max.	Unit	
Static								
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS, I_D} = 250 \mu A$	N-Ch	0.45		1	V	
		$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	P-Ch	- 0.45		- 1		
Gate Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$	N-Ch		± 0.5	± 1.0	μА	
date body Leakage			P-Ch		± 1.0	± 2.0		
Zero Gate Voltage Drain	1	V _{DS} = 16 V, V _{GS} = 0 V	N-Ch		0.3	100	nA	
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch		- 0.3	- 100		
Current	I _{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$	N-Ch			5		
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$	P-Ch			- 5	μΑ	
On State Drain Current ^a		$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	700			mA	
On State Drain Current	$I_{D(on)}$	V _{DS} = - 5 V, V _{GS} = - 4.5 V	P-Ch	- 700				
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 600 \text{ mA}$	N-Ch		0.41	0.70	Ω	
		V _{GS} = - 4.5 V, I _D = - 350 mA	P-Ch		0.80	1.2		
Drain-Source On-State		V _{GS} = 2.5 V, I _D = 500 mA	N-Ch		0.53	0.85		
Resistance ^a		V _{GS} = - 2.5 V, I _D = - 300 mA	P-Ch		1.20	1.6		
		V _{GS} = 1.8 V, I _D = 350 mA	N-Ch		0.70	1.25		
		V _{GS} = - 1.8 V, I _D = - 150 mA	P-Ch		1.80	2.7		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 400 mA	N-Ch		1.0			
		V _{DS} = - 10 V, I _D = - 250 mA	P-Ch		0.4		S	
	V _{SD}	I _S = 150 mA, V _{GS} = 0 V	N-Ch		0.8	1.2		
Diode Forward Voltage ^a		I _S = - 150 mA, V _{GS} = 0 V	P-Ch		- 0.8	- 1.2	V	
Dynamic ^b								
•	Qg		N-Ch		750			
Total Gate Charge		N-Channel	P-Ch		1500			
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 250 \text{ mA}$	N-Ch		75		nC	
		P-Channel	P-Ch		150		pC	
Gate-Drain Charge	Q _{gd}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -250 \text{ mA}$	N-Ch		225			
			P-Ch		450			
Turn-On Time	t _{ON}	N-Channel	N-Ch		5			
		$V_{DD} = 10 \text{ V}, R_L = 47 \Omega$ $I_D \cong 200 \text{ mA}, V_{GEN} = 4.5 \text{ V}, R_q = 10 \Omega$	P-Ch		5			
	t _{OFF}	$I_D = 200 \text{ mA}, V_{GEN} = 4.3 \text{ V}, H_g = 10.32$ P-Channel	N-Ch		25		ns	
Turn-Off Time		$V_{DD} = -10 \text{ V}, R_L = 47 \Omega$	P-Ch		35			
		$I_D \cong$ - 200 mA, V_{GEN} = - 4.5 V, R_g = 10 Ω						

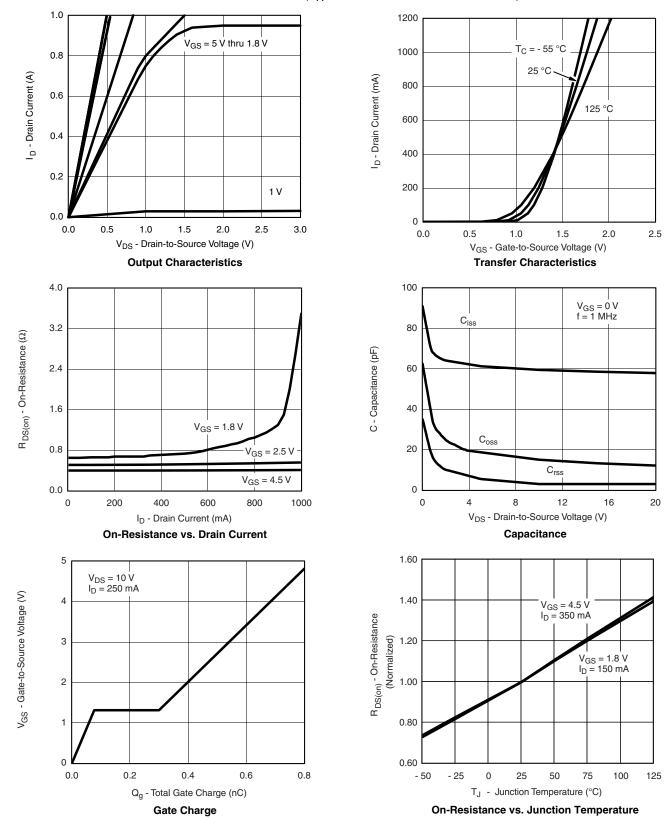
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



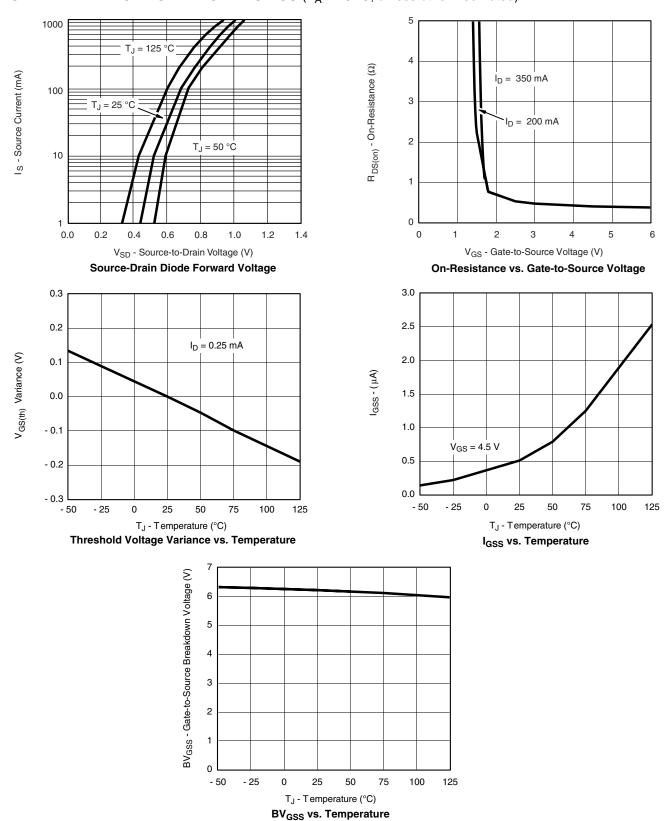
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25 \, ^{\circ}C$, unless otherwise noted)



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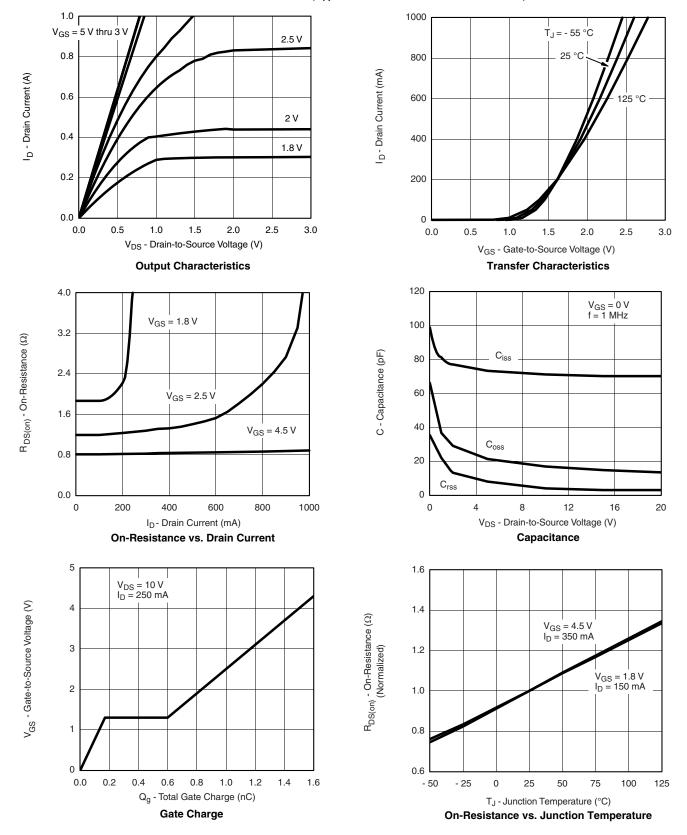


N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25~^{\circ}C$, unless otherwise noted)





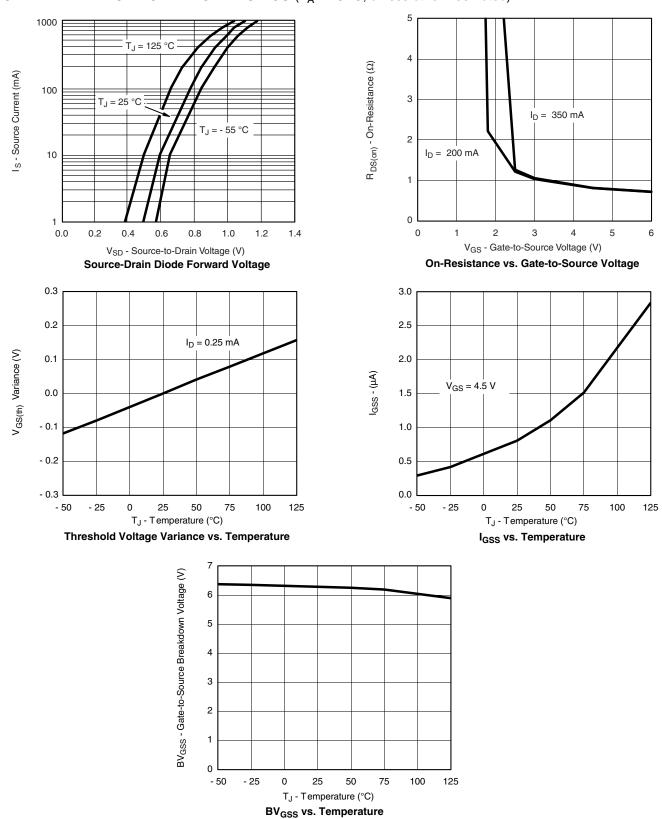
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25~^{\circ}C$, unless otherwise noted)



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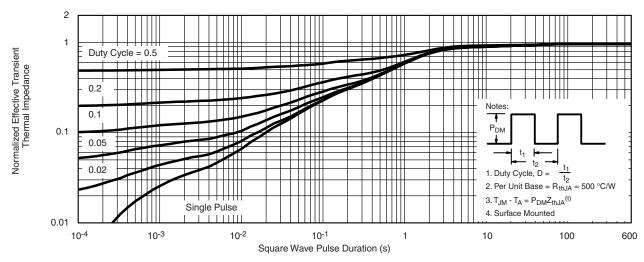
VISHAY.

P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)





N- OR P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25~^{\circ}C$, unless otherwise noted)

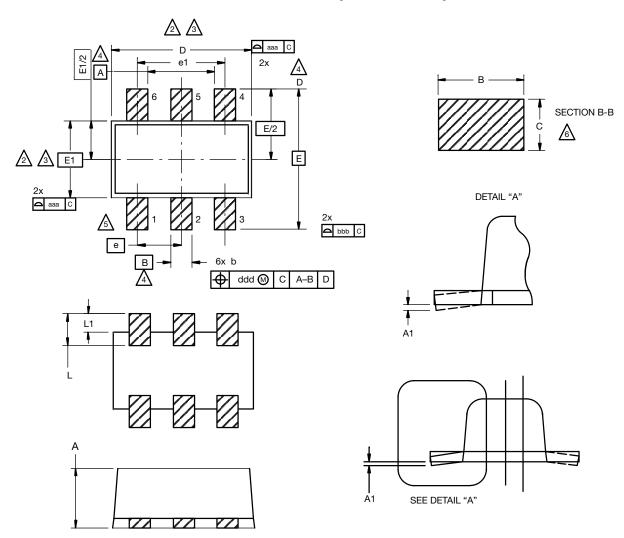


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71168.



SC-89 6-Leads (SOT-563F)



Notes

1. Dimensions in millimeters.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

⚠ Datums A, B and D to be determined 0.10 mm from the lead tip.

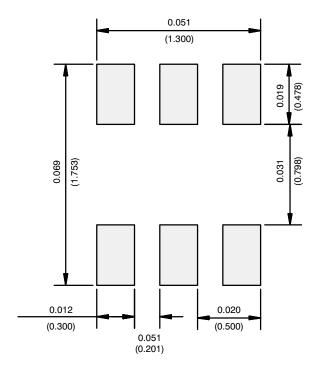
 Δ Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.		MILLIMETERS		
	MIN.	NOM.	MAX.	
Α	0.56	0.58	0.60	
A1	0	0.02	0.10	
b	0.15	0.22	0.30	
С	0.10	0.14	0.18	
D	1.50	1.60	1.70	
E	1.50	1.60	1.70	
E1	1.15	1.20	1.25	
е	0.45	0.50	0.55	
e1	0.95	1.00	1.05	
L	0.25	0.35	0.50	
L1	0.10	0.20	0.30	
C14-0439-Rev. C, 11-Aug-14 DWG: 5880				



RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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