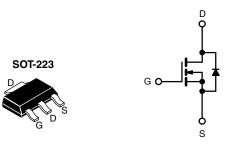
Vishay Siliconix

COMPLIANT

HALOGEN

FREE

Power MOSFET



N-Channel MOSFET

Marking code: LA

PRODUCT SUMMA	ODUCT SUMMARY				
V _{DS} (V)	60				
$R_{DS(on)}(\Omega)$	$V_{GS} = 5.0 \text{ V}$	0.20			
Q _g max. (nC)	8.4				
Q _{gs} (nC)	3.5				
Q _{gd} (nC)	6.0				
Configuration	Sing	le			

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Logic-level gate drive
- R_{DS(on)} specified at V_{GS} = 4 V and 5 V
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Lead (Pb)-free and halogen-free	SiHLL014TR-GE3
Lead (Pb)-free and halogen-free	IRLL014TRPbF-BE3 a, b
Lead (Pb)-free	IRLL014TRPbF ^a

Notes

- a. See device orientation
- b. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	60	V		
Gate-source voltage		V_{GS}	± 10	7 v		
Continuous drain current	\/ at 10 \/	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	1	2.7		
Continuous drain current	V _{GS} at 10 V	T _C = 100 °C	I _D	1.7	А	
Pulsed drain current ^a	Divi					
Linear derating factor				0.025	W/°C	
Linear derating factor (PCB mount) e				0.017	- W/ C	
Single pulse avalanche energy b			E _{AS}	100	mJ	
Avalanche current ^a		I _{AR}	2.7	А		
Repetitive avalanche energy a	petitive avalanche energy ^a		E _{AR}	0.31	mJ	
Maximum power dissipation	T _C = 25 °C		Б	3.1	W	
Maximum power dissipation (PCB mount) e	T _A =	25 °C	P_D	2.0	- vv	
Peak diode recovery dv/dt c	ak diode recovery dv/dt ^c		dV/dt	4.5	V/ns	
perating junction and storage temperature range T _J , T _{stg} -55 to +150		°C				
Soldering recommendations (peak temperature) d	o,			300		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. $V_{DD} = 25 \text{ V}$, starting $T_J = 25 \,^{\circ}\text{C}$, $L = 16 \,^{\circ}\text{mH}$, $R_g = 25 \,^{\circ}\Omega$, $I_{AS} = 2.7 \,^{\circ}\text{A}$ (see fig. 12)
- c. $I_{SD} \le 10$ A, $dI/dt \le 90$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case
- e. When mounted on 1" square PCB (FR-4 or G-10 material)

S21-0322-Rev. G, 05-Apr-2021



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THERMAL RESISTANCE RAT	INGS				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	-	60	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	-	40	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static				L	L			
Drain-source breakdown voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 250 μA	60	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 1 mA	-	0.073	-	V/°C	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	1.0	-	2.0	V	
Gate-source leakage	I _{GSS}	,	V _{GS} = ± 10 V	-	-	± 100	nA	
Zana mata walta na dunin ayumant	I _{DSS}	V _{DS} :	V _{DS} = 60 V, V _{GS} = 0 V		-	25	1	
Zero gate voltage drain current		V _{DS} = 48 V	V _{GS} = 0 V, T _J = 125 °C	-	-	250	μA	
Duning and an adult and interest	Б	V _{GS} = 5.0 V	I _D = 1.6 A ^b	-	-	0.20		
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 4.0 V	I _D = 1.4 A ^b	-	-	0.28	Ω	
Forward transconductance	9 _{fs}	V _{DS} :	= 25 V, I _D = 1.6 A	3.2	-	-	S	
Dynamic								
Input capacitance	C _{iss}	$V_{GS} = 0 V$,		-	400	-		
Output capacitance	C _{oss}		$V_{DS} = 25 \text{ V},$	-	170	-	pF	
Reverse transfer capacitance	C _{rss}	f = 1.	0 MHz, see fig. 5	-	42	-		
Total gate charge	Qg			-	-	8.4		
Gate-source charge	Q _{gs}	$V_{GS} = 5.0 \text{ V}$	$I_D = 10 \text{ A}, V_{DS} = 48 \text{ V},$ see fig. 6 and 13 b	-	-	3.5	nC	
Gate-drain charge	Q _{gd}		See fig. 6 and 16	-	-	6.0		
Turn-on delay time	t _{d(on)}			-	9.3	-		
Rise time	t _r	V _{DD} :	= 30 V, I _D = 10 A,	-	110	-	1	
Turn-off delay time	t _{d(off)}	$R_{\rm g} = 12 \ \Omega, \ R_{\rm D} = 2.8 \ \Omega, \ {\rm see \ fig. \ 10 \ b}$		-	ns			
Fall time	t _f			-	26	-		
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from		-	الم			
Internal source inductance	L _S	package and die contact	center of	-	6.0	-	nH	
Drain-Source Body Diode Characteristic	es							
Continuous source-drain diode current	I _S	showing the	MOSFET symbol showing the		-	2.7	A	
Pulsed diode forward current ^a	I _{SM}	integral revers p - n junction		-	-	22	7 ^	
Body diode voltage	V _{SD}	T _J = 25 °C	, I _S = 2.7 A, V _{GS} = 0 V ^b	-	-	1.6	V	
Body diode reverse recovery time	t _{rr}	T 05 °C !	10 A all/at 100 A/: h	-	65	130	ns	
Body diode reverse recovery charge	Q _{rr}	$I_{\rm J} = 25 {\rm ^{\circ}C}, I_{\rm F}$	= 10 A, dl/dt = 100 A/µs b	-	0.33	0.65	μC	
Forward turn-on time	t _{on}	Intrinsic tu	rn-on time is negligible (turn	on is dor	ninated b	y L _S and	L _D)	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

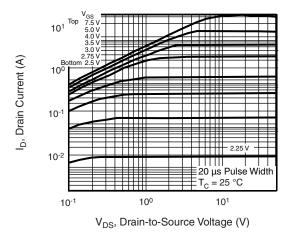


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

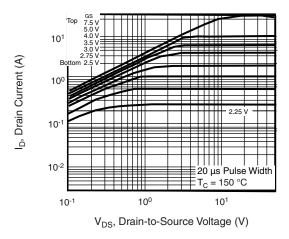


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

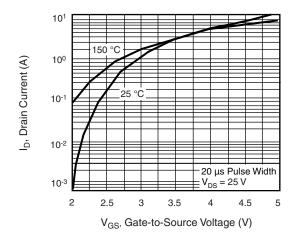


Fig. 3 - Typical Transfer Characteristics

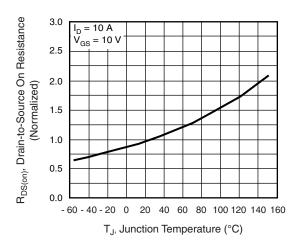


Fig. 4 - Normalized On-Resistance vs. Temperature

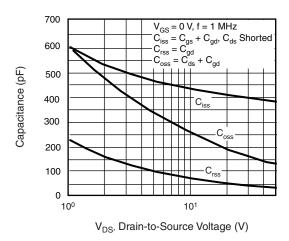


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

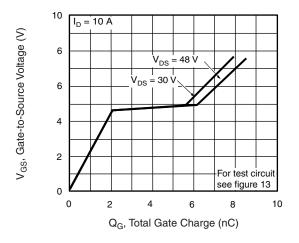


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



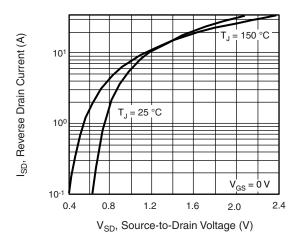


Fig. 7 - Typical Source-Drain Diode Forward Voltage

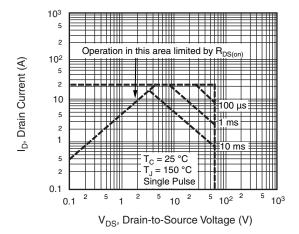


Fig. 8 - Maximum Safe Operating Area

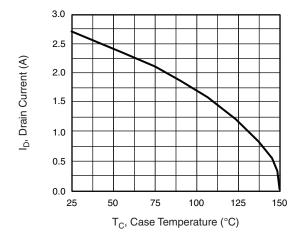


Fig. 9 - Maximum Drain Current vs. Case Temperature

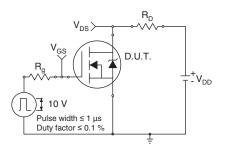


Fig. 10a - Switching Time Test Circuit

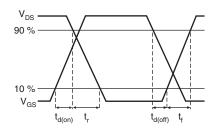


Fig. 10b - Switching Time Waveforms



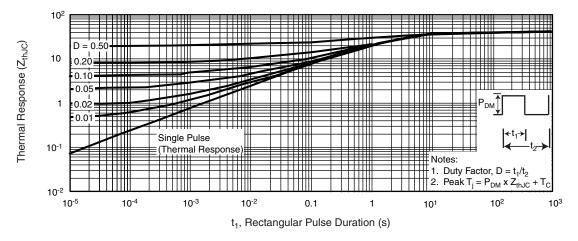


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

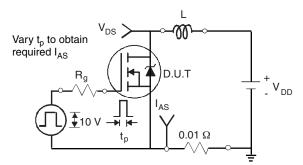


Fig. 12a - Unclamped Inductive Test Circuit

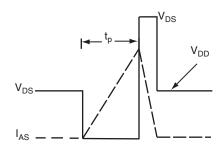


Fig. 12b - Unclamped Inductive Waveforms

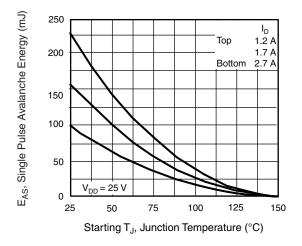


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



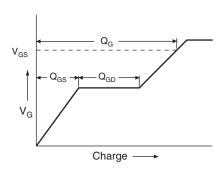


Fig. 13a - Basic Gate Charge Waveform

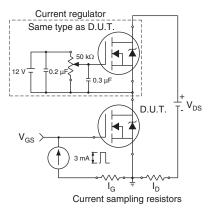
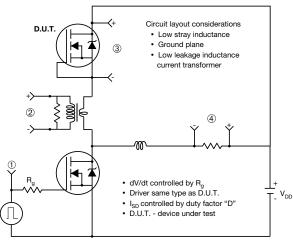


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



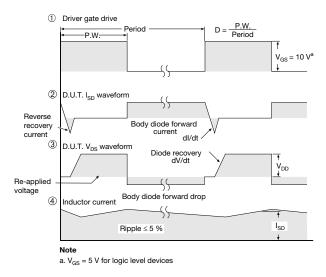


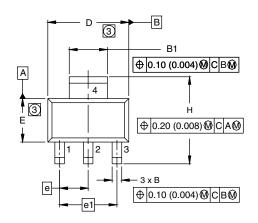
Fig. 14 - For N-Channel

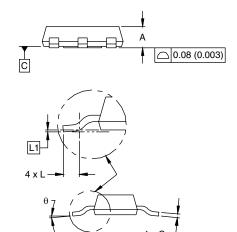
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SOT-223 (HIGH VOLTAGE)





DIM.	MILLII	METERS	INCHES		
	MIN.	MAX.	MIN.	MAX.	
Α	1.55	1.80	0.061	0.071	
В	0.65	0.85	0.026	0.033	
B1	2.95	3.15	0.116	0.124	
С	0.25	0.35	0.010	0.014	
D	6.30	6.70	0.248	0.264	
E	3.30	3.70	0.130	0.146	
е	2.30	2.30 BSC		BSC	
e1	4.60	BSC	0.181	BSC	
Н	6.71	7.29	0.264		
L	0.91	-	0.036	-	
L1	0.061 BSC		0.0024	BSC	
θ	-	10'	-	10'	

ECN: S-82109-Rev. A, 15-Sep-08

DWG: 5969

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension do not include mold flash.
- 4. Outline conforms to JEDEC outline TO-261AA.

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Revision: 15-Sep-08 1



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