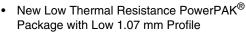


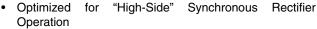
N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
30	0.012 at V _{GS} = 10 V	15.7		
	0.020 at V _{GS} = 4.5 V	12.1		

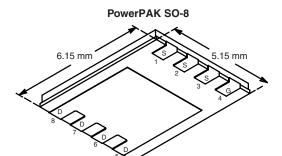
FEATURES

- · Halogen-free available
- TrenchFET[®] Power MOSFET





100 % R_g Tested



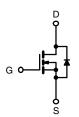
Bottom View

Ordering Information: Si7888DP-T1-E3 (Lead (Pb)-free)

Si7888DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

· DC/DC Converters



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V_{DS}	30		V	
Gate-Source Voltage		V_{GS}	± 20			
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	I _D	15.7	9.4		
Continuous Diain Current (1) = 150 °C)	T _A = 70 °C		12.5	7.5		
Pulsed Drain Current		I _{DM}	± 50		Α	
Continuous Source Current (Diode Conduction) ^a		I _S	4.1	1.5		
Avalanche Current	L = 0.1 mH	I _{AS}	20 20			
Single Pulse Avalanche Energy	L = 0.111111	E _{AS}			mJ	
Mariana Darra Dissination	T _A = 25 °C	P _D	5.0	1.8	W	
Maximum Power Dissipation ^a	T _A = 70 °C		3.2	1.1	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}			260		C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum lunction to Ambient (MOCFFT)8	t ≤ 10 s	R _{thJA}	21	25	°C/W
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State		55	70	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.4	3.0	

Notes

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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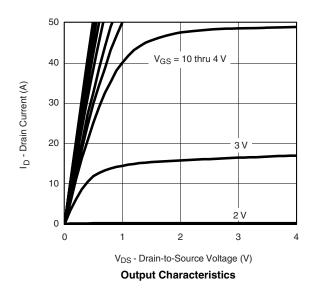


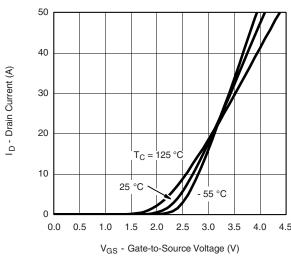
SPECIFICATIONS T _J = 25 °C, unless otherwise noted									
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static									
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	0.80		2	V			
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA			
Zoro Coto Voltago Droin Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V		1					
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			5	μΑ			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	50			Α			
D : 0	R _{DS(on)}	V _{GS} = 10 V, I _D = 12.4 A		0.010	0.012				
Drain-Source On-State Resistance ^a		$V_{GS} = 4.5 \text{ V}, I_D = 9.6 \text{ A}$	V _{GS} = 4.5 V, I _D = 9.6 A 0.016		0.020	Ω			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 12.4 A		27		S			
Diode Forward Voltage ^a	V _{SD}	$I_S = 2.6 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.2	V			
Dynamic ^b									
Total Gate Charge	Qg			8.7	10.5				
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 5.0 \text{ V}, I_D = 12.4 \text{ A}$		2.4		nC			
Gate-Drain Charge	Q _{gd}			3.5					
Gate Resistance	R_{g}		0.2	1	1.5	Ω			
Turn-On Delay Time	t _{d(on)}			10	20				
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		11	20				
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		24	50	ns			
Fall Time	t _f			10	20				
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.6 A, di/dt = 100 A/μs		50	75				

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





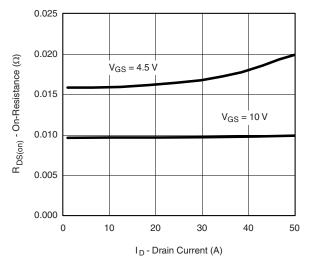
Transfer Characteristics

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

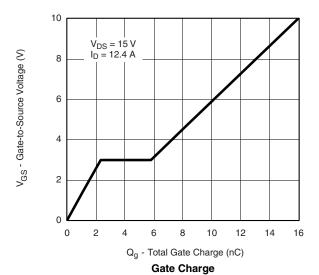
b. Guaranteed by design, not subject to production testing.

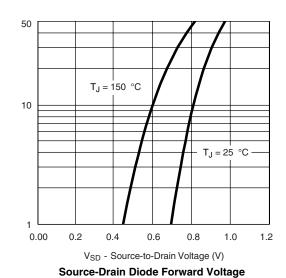


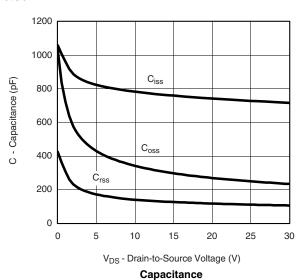
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

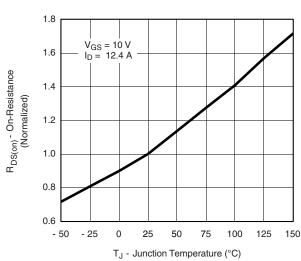


On-Resistance vs. Drain Current

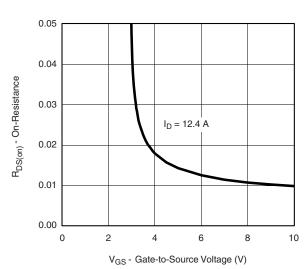








On-Resistance vs. Junction Temperature



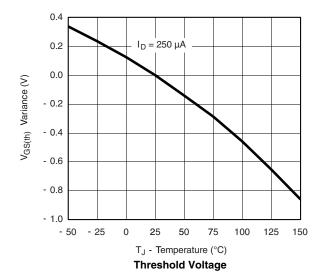
On-Resistance vs. Gate-to-Source Voltage

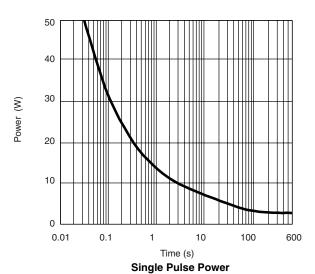
Is - Source Current (A)

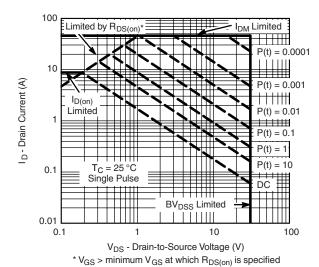
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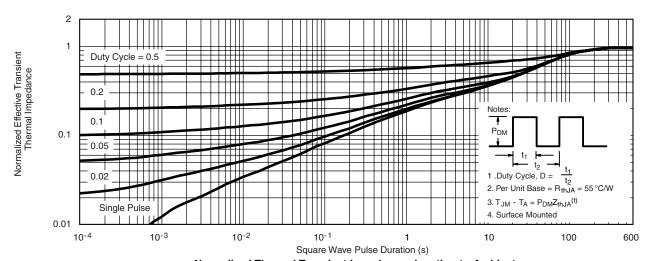
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







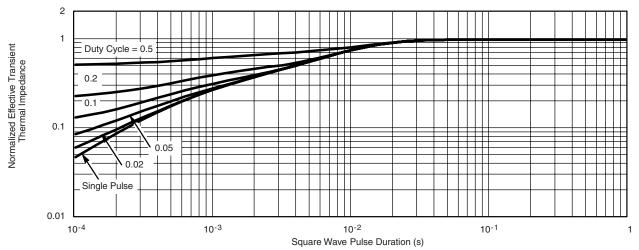
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71876.

Document Number: 71876 www.vishay.com S-80440-Rev. D, 03-Mar-08 5



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