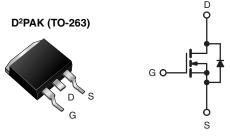
Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	250					
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.45					
Q _g (Max.) (nC)	41					
Q _{gs} (nC)	6.5					
Q _{gd} (nC)	22					
Configuration	Single					



N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- · Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION						
Package	D ² PAK (TO-263)	D ² PAK (TO-263)				
Lead (Pb)-free and Halogen-free	SiHF634S-GE3	SiHF634STRR-GE3 ^a				
Lead (Pb)-free	IRF634SPbF	IRF634STRRPbF ^a				
	SiHF634S-E3	SiHF634STR-E3ª				

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage			V _{DS}	250		
Gate-Source Voltage			V _{GS}	± 20	V	
Continuous Drain Current	V at 10 V	T _C = 25 °C T _C = 100 °C		8.1		
Continuous Drain Current	V _{GS} at 10 V		ID	5.1	А	
Pulsed Drain Current ^a			I _{DM}	32		
Linear Derating Factor		0.59	- W/°C			
Linear Derating Factor (PCB Mount) ^e		0.025				
Single Pulse Avalanche Energy ^b	E _{AS}	300	mJ			
Avalanche Current ^a	I _{AR}	8.1	А			
Repetitive Avalanche Energy ^a	E _{AR}	7.4	mJ			
Maximum Power Dissipation	р	74	w			
Maximum Power Dissipation (PCB Mount) ^e	T _A = 25 °C		PD	3.1	vv	
Peak Diode Recovery dV/dt ^c	dV/dt	4.8	V/ns			
Operating Junction and Storage Temperature Rang	T _J , T _{stg}	- 55 to + 150	°C			
Soldering Recommendations (Peak Temperature)	for	10 s		300 ^d		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 50 \text{ V}$, starting $T_J = 25 \text{ °C}$, L = 7.3 mH, $R_g = 25 \Omega$, $I_{AS} = 8.1 \text{ A}$ (see fig. 12).

c. $I_{SD} \le 8.1$ A, dI/dt ≤ 120 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

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COMPLIANT HALOGEN

FREE

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THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYP.	MAX.	UNIT			
Maximum Junction-to-Ambient	R _{thJA}	-	62				
Maximum Junction-to-Ambient (PCB Mount) ^a	R _{thJA}	-	40	°C/W			
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.7				

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	250	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 1 mA	-	0.37	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	- V _{GS} , I _D = 250 μΑ	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	,	V _{GS} = ± 20 V	-	-	± 100	nA
	_	V _{DS} =	= 250 V, V _{GS} = 0 V	-	-	25	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 200 V	′, V _{GS} = 0 V, T _J = 125 °C	-	-	250	μA
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 10 V$	I _D = 5.1 A ^b	-	-	0.45	Ω
Forward Transconductance	g fs	V _{DS} =	50 V, I _D = 5.1 A ^b	1.6	-	-	S
Dynamic					•	•	
Input Capacitance	C _{iss}		$V_{GS} = 0 V,$	-	770	-	
Output Capacitance	C _{oss}	1	$V_{DS} = 25 V,$	-	190	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1.	0 MHz, see fig. 5	-	52	-	
Total Gate Charge	Qg			-	-	41	1
Gate-Source Charge	Q _{gs}	$V_{GS} = 10 V$	$I_{GS} = 10 \text{ V}$ $I_D = 5.6 \text{ A}, V_{DS} = 200 \text{ V},$ see fig. 6 and 13 ^b		-	6.5	nC
Gate-Drain Charge	Q _{gd}	1			-	22	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 125 V, I _D = 5.6 A, R _g = 12 Ω, R _D = 22 Ω, see fig. 10 ^b		-	9.6	-	- ns
Rise Time	t _r			-	21	-	
Turn-Off Delay Time	t _{d(off)}			-	42	-	
Fall Time	t _f	1				-	1
Internal Drain Inductance	L _D	6 mm (0.25") f	Between lead, 6 mm (0.25") from		4.5	-	nH
Internal Source Inductance	L _S	package and die contact	-	7.5	-		
Drain-Source Body Diode Characteristic	S						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the		-	-	8.1	А
Pulsed Diode Forward Current ^a	I _{SM}	0	p - n junction diode		-	32	
Body Diode Voltage	V_{SD}	T _J = 25 °C	$T_J = 25 \ ^{\circ}C, \ I_S = 8.1 \ A, \ V_{GS} = 0 \ V^b$		-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 5.6 A, dl/dt = 100 A/µs ^b		-	220	440	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$J = 25 \text{ C}, I_{\text{F}}$	$= 5.0 \text{ A}, \text{ u/ut} = 100 \text{ A/}\mu\text{S}^{\circ}$	-	1.2	2.4	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	-on is dor	ninated b	$v L_s$ and	L _D)	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width \leq 300 µs; duty cycle \leq 2 %.

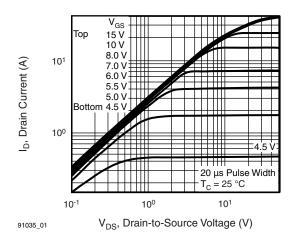
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



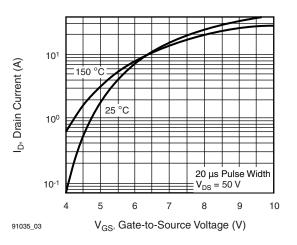


Fig. 3 - Typical Transfer Characteristics

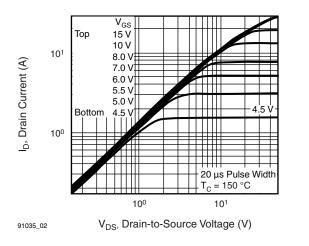


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

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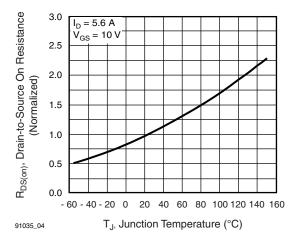


Fig. 4 - Normalized On-Resistance vs. Temperature

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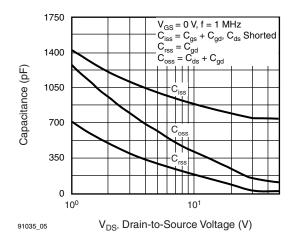


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

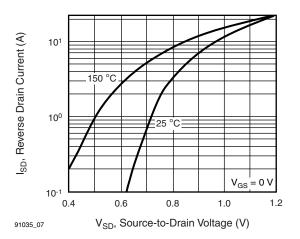


Fig. 7 - Typical Source-Drain Diode Forward Voltage

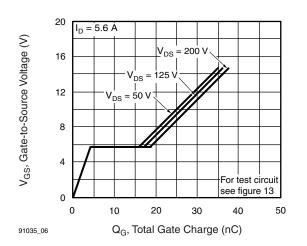


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

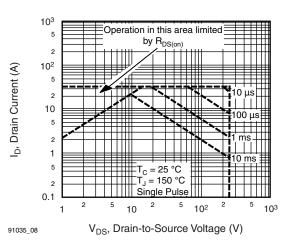


Fig. 8 - Maximum Safe Operating Area

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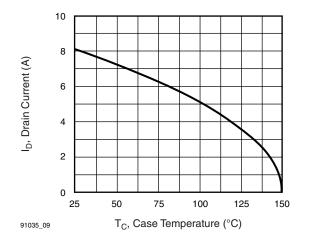


Fig. 9 - Maximum Drain Current vs. Case Temperature

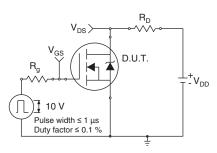


Fig. 10a - Switching Time Test Circuit

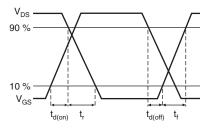


Fig. 10b - Switching Time Waveforms

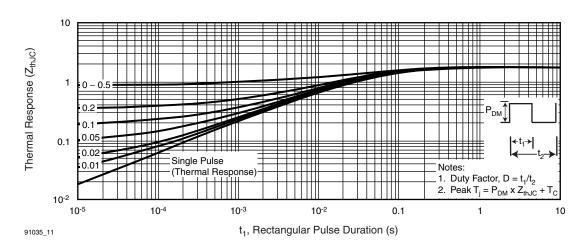


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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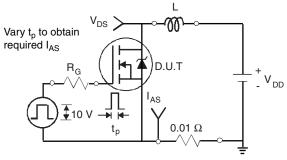


Fig. 12a - Unclamped Inductive Test Circuit

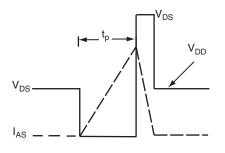


Fig. 12b - Unclamped Inductive Waveforms

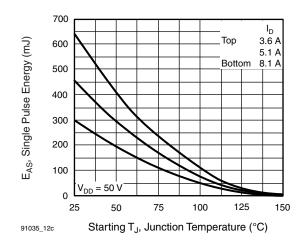


Fig. 13 - Maximum Avalanche Energy vs. Drain Current

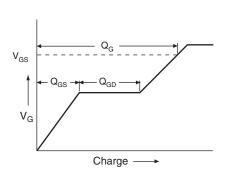


Fig. 13a - Basic Gate Charge Waveform

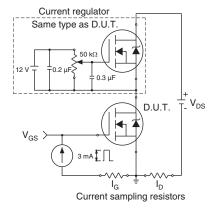
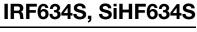


Fig. 13b - Gate Charge Test Circuit

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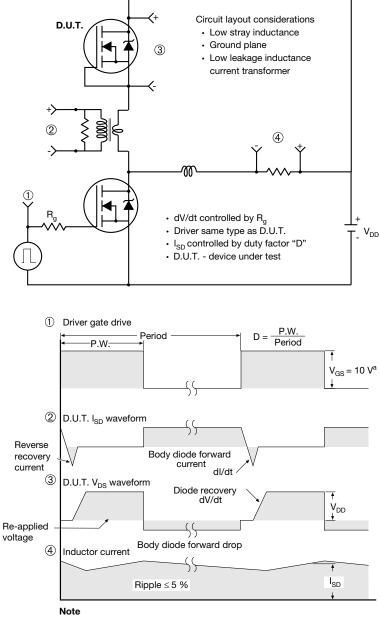
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Peak Diode Recovery dV/dt Test Circuit



a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)

/3 ⁄4

2 x 🗗

A

н

-2 x b2 <−2 x b

Plating

ł

Detail A

(Datum A)

D

 $\underline{4}$ 11

		Lead tip		(c) $(b, b2) \rightarrow$ <u>Section B - B and C - C</u> Scale: none			$E1 \rightarrow 4$			
	MILLIMETERS		INCHES				MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.		DIM.	MIN.	MAX.	MIN.	MAX.
А	4.06	4.83	0.160	0.190		D1	6.86	-	0.270	-
A1	0.00	0.25	0.000	0.010		Е	9.65	10.67	0.380	0.420
b	0.51	0.99	0.020	0.039		E1	6.22	-	0.245	-
b1	0.51	0.89	0.020	0.035		е	2.54 BSC		0.100 BSC	
b2	1.14	1.78	0.045	0.070		Н	14.61	15.88	0.575	0.625
b3	1.14	1.73	0.045	0.068		L	1.78	2.79	0.070	0.110
С	0.38	0.74	0.015	0.029		L1	-	1.65	-	0.066
c1	0.38	0.58	0.015	0.023		L2	-	1.78	-	0.070
c2	1.14	1.65	0.045	0.065		L3	0.25	BSC	0.010	BSC
D	8.38	9.65	0.330	0.380		L4	4.78	5.28	0.188	0.208

Α

Δ

// ± 0.004 M B

b1, b3

Base metal

- Notes
- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.



H

B

A1

D1 4

Gauge plane

. Ŀ3

Detail "A" Rotated 90° CW scale 8:1

0° to 8° **Vishay Siliconix**

Seating plane



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