

Low Voltage, 0.6 Ω , Dual SPDT Analog Switch

DESCRIPTION

The DG2735, DG2736 are low voltage, low on-resistance, dual single-pole/double-throw (SPDT) monolithic CMOS analog switches designed for high performance switching of analog signals. Combining low-power, high speed, low on-resistance, and small package size, the DG2735, DG2736 are ideal for portable and battery power applications.

The DG2735, DG2736 have an operation range from 1.65 V to 4.3 V single supply. The DG2735 has two separate control pins with for the separated two SPDT switched. The DG2736 has an EN pin. All switches are at high impedance mode when the EN is high.

The DG2735, DG2736 are guaranteed 1.65 V logic compatible, allowing the easy interface with low voltage DSP or MCU control logic and ideal for one cell Li-ion battery direct power.

The switch conducts signals within power rails equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make is guaranteed.

The DG2735, DG2736 are built on Vishay Siliconix's sub micron CMOS low voltage process technology and provides greater than 300 mA latch-up protection, as tested per JESD78.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG2735, DG2736 are offered in a miniQFN package. The miniQFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

- Low voltage operation (1.65 V to 4.3 V)
- Low on-resistance - R_{ON} : 0.6 Ω at 2.7 V
- Fast switching: t_{ON} = 55 ns at 2.7 V
- T_{OFF} = 40 ns at 2.7 V
- Latch-up current > 300 mA (JESD78)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

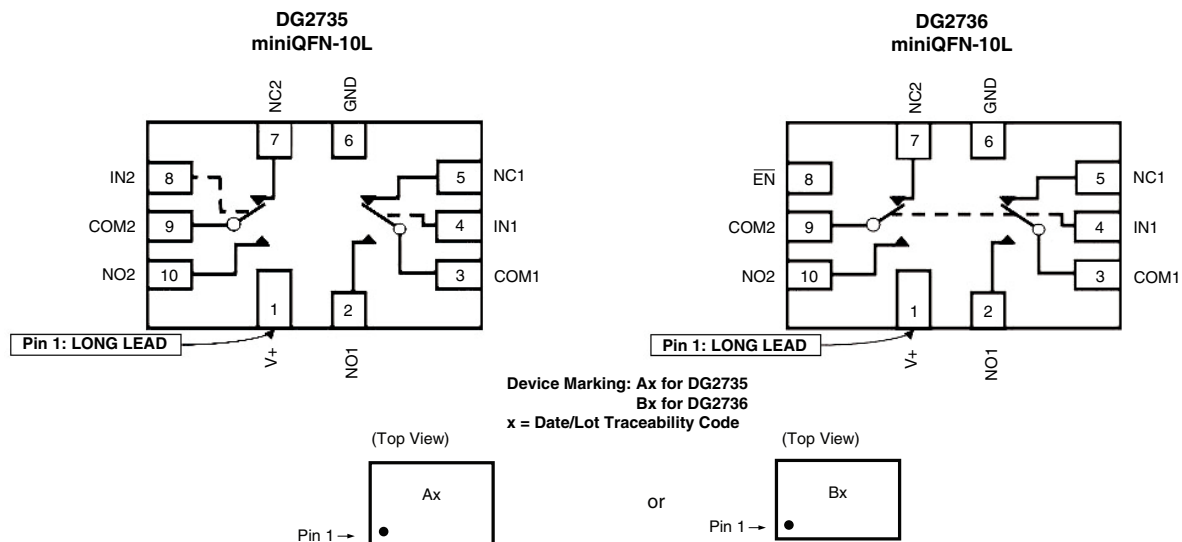
BENEFITS

- Reduced power consumption
- High accuracy
- Reduce board space
- TTL/1.65 V logic compatible

APPLICATIONS

- Cellular phones
- Speaker headset switching
- Audio and video signal routing
- PCMCIA cards
- Battery operated systems
- Portable media player Handheld test instruments

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE			
Logic	EN (DG2736 only)	NC1, 2	NO1, 2
0	1	OFF	OFF
1	1	OFF	OFF
0	0	ON	OFF
1	0	OFF	ON

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85°C	miniQFN10	DG2735DN-T1-E4 DG2736DN-T1-E4

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Reference to GND	V+	- 0.3 to 5	V	
	IN, COM, NC, NO ^a	- 0.3 to (V+ + 0.3)		
Current (Any terminal except NO, NC or COM)		30	mA	
Continuous Current (NO, NC, or COM)		± 250		
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500		
Storage Temperature (D Suffix)		- 65 to 150	°C	
Power Dissipation (Packages) ^b	miniQFN10 ^c	208	mW	

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 4 mW/C above 70 °C.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3 V, ± 10 %, V _{IN} = 0.4 V or 1.65 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	V _{analog}	R _{DS(on)}	Full	0		V+	V
On-Resistance	R _{DS(on)}	V+ = 2.7 V, I _{NO/NC} = 100 mA, V _{COM} = 0.5 V	Room		0.5	0.6	Ω
		V+ = 2.7 V, I _{NO/NC} = 100 mA, V _{COM} = 1.5 V	Room				
		V+ = 2.7 V, I _{NO/NC} = 100 mA, V _{COM} = 0.5 V	Full		0.5		
		V+ = 2.7 V, I _{NO/NC} = 100 mA, V _{COM} = 1.5 V	Full				
		V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.9 V	Room		0.4	0.5	
		V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 2.5 V	Room		0.3		
		V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.9 V	Full		0.5		
		V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 2.5 V	Full				
R _{ON} Match ^d	ΔR _{ON}	V+ = 2.7 V, I _{NO/NC} = 100 mA, V _{COM} = 0.5 V, 1.5 V V+ = 4.3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.9 V, 2.5 V	Room		0.06	0.08	
R _{ON} resistance flatness ^d	R _{ON} flatness	V+ = 2.7 V, I _{NO/NC} = 100 mA, V _{COM} = 0.5 V, 1.5 V	Room			0.15	
Switch Off Leakage Current	I _{NO/NC(off)}	V+ = 4.3 V, V _{NO/NC} = 0.3 V/4 V, V _{COM} = 4 V/0.3 V	Room	- 2		2	nA
			Full	- 10		10	
	Room		- 2		2		
	Full		- 10		10		
Channel-On Leakage Current	I _{COM(on)}	V+ = 4.3 V, V _{NO/NC} = V _{COM} = 4 V/0.3 V	Room	- 5		5	
			Full	- 20		20	



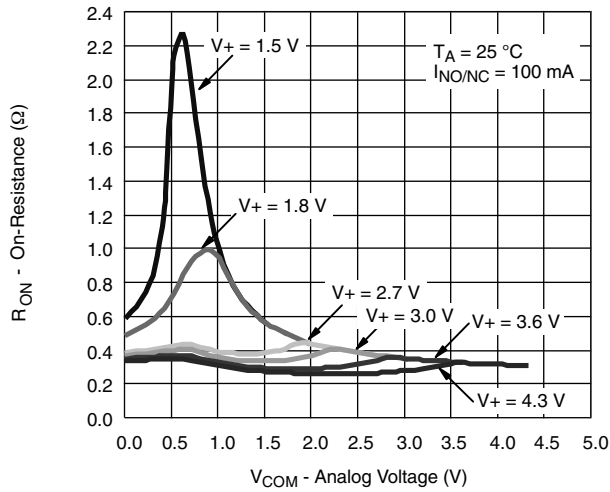
SPECIFICATIONS (V ₊ = 3 V)								
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 3 V, ± 10 %, V _{IN} = 0.4 V or 1.65 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit	
				Min. ^b	Typ. ^c	Max. ^b		
Digital Control								
Input High Voltage	V _{INH}		Full	1.65			V	
Input Low Voltage	V _{INL}		Full			0.4		
Input Capacitance	C _{IN}		Full		6		pF	
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V ₊	Full	- 1		1	μA	
Dynamic Characteristics								
Break-Before-Make Time ^e	t _{BBM}	V ₊ = 3.6 V, V _{NO} , V _{NC} = 1.5 V, R _L = 50 Ω, C _L = 35 pF	Room	1	5		ns	
Turn-On Time ^e	t _{ON}		Room		50	78		
			Full			80		
Turn-Off Time ^e	t _{OFF}		Room		35	58		
			Full			60		
Enable Turn-On Time ^e DG2736 (EN)	t _{ON(EN)}		Room		50	78		
			Full			80		
Enable Turn-Off Time ^e DG2736 (EN)	t _{OFF(EN)}		Room		35	58		
		Full			60			
Off-Isolation ^d	O _{IRR}	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz	Room		- 70		dB	
Crosstalk ^d	X _{TALK}				- 70			
3dB bandwidth ^d		R _L = 50 Ω, C _L = 5 pF	Room		50		MHz	
NO, NC Off Capacitance ^d	C _{NO(off)}	V _{IN} = 0 V, or V ₊ , f = 1 MHz	Room		55		pF	
	C _{NC(off)}				55			
Channel On Capacitance ^d	C _{NO(on)}					130		
	C _{NC(on)}					130		
Power Supply								
Power Supply Range	V ₊			1.65		4.3	V	
Power Supply Current	I ₊	V _{IN} = 0 or V ₊	Full			1	μA	

Notes:

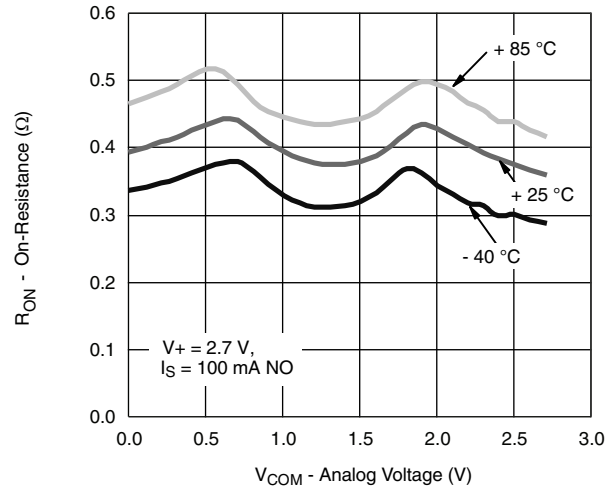
- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, not subjected to production test.
- e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

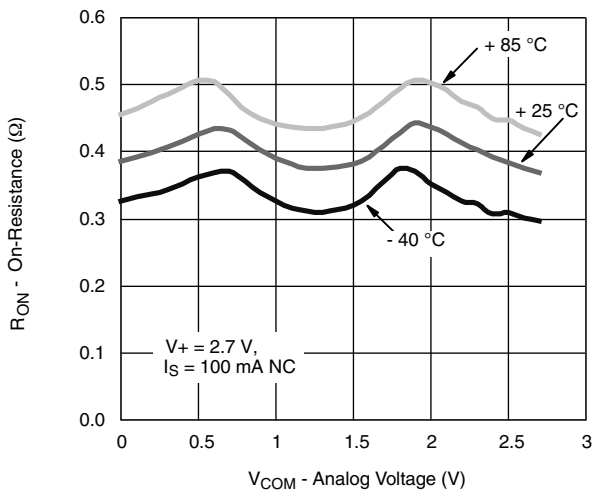
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



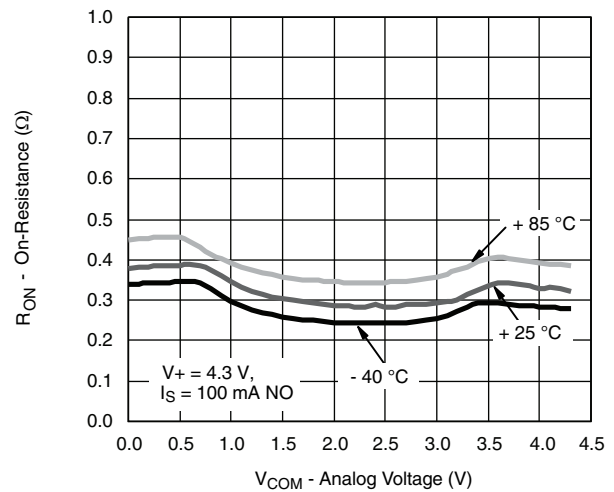
RON vs. VCOM and Supply Voltage



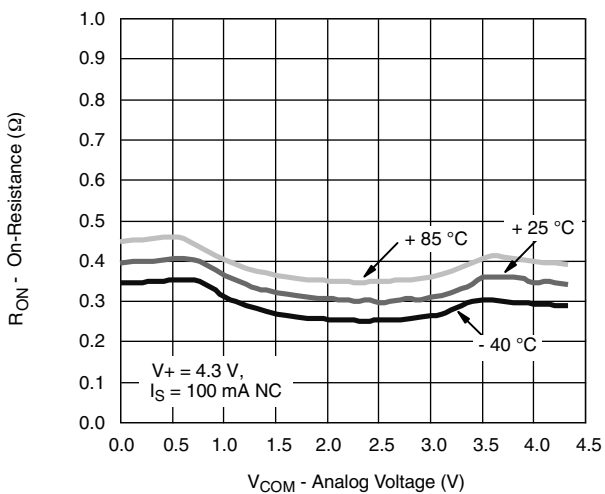
RON vs. Analog Voltage and Temperature



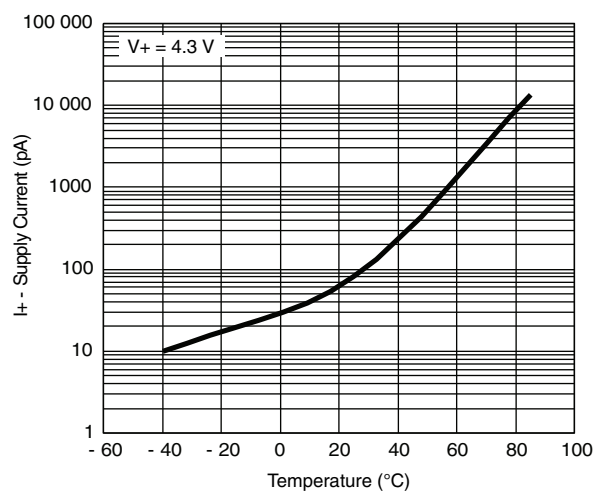
RON vs. Analog Voltage and Temperature



RON vs. Analog Voltage and Temperature

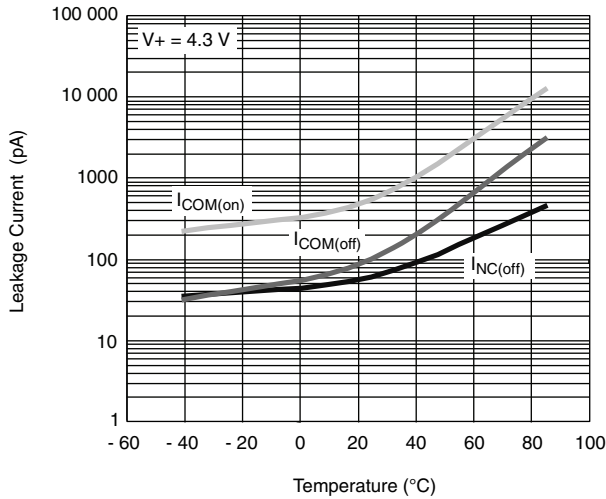


RON vs. Analog Voltage and Temperature

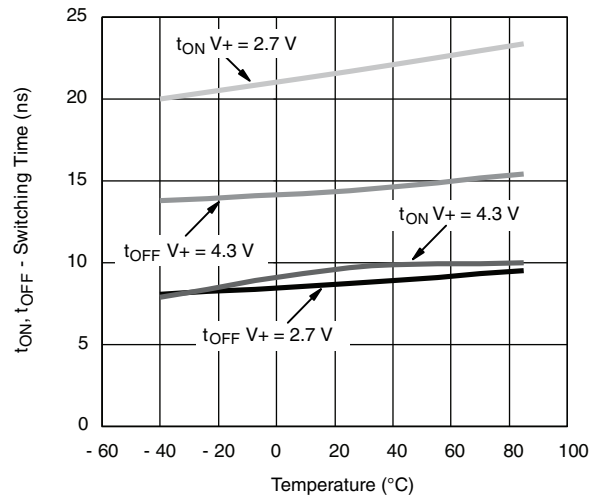


Supply Current vs. Temperature

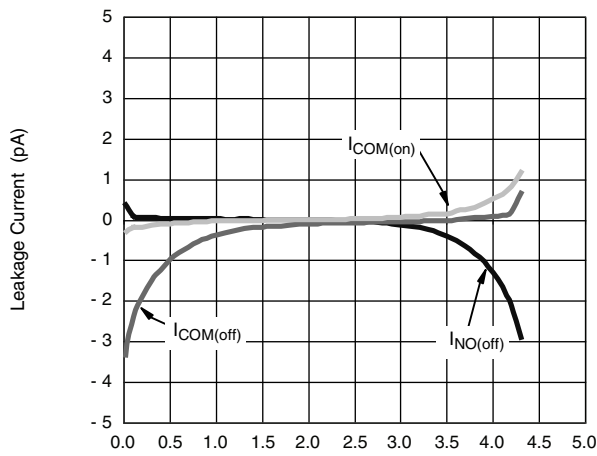
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



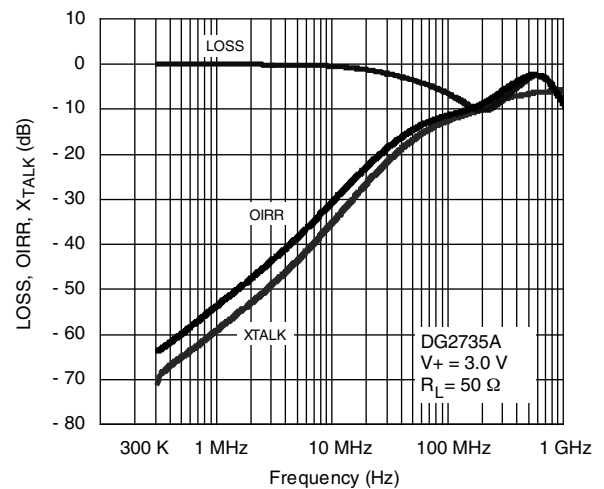
Leakage Current vs. Temperature



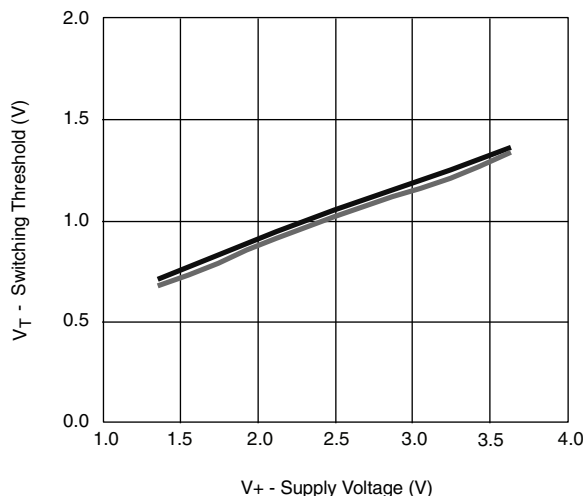
Switching Time vs. Temperature



Leakage vs. Analog Voltage

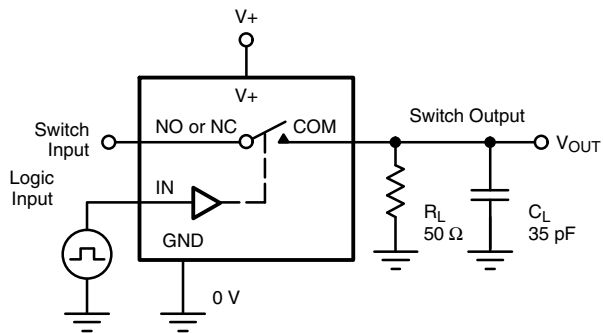


Insertion Loss, Off-Isolation Crosstalk vs. Frequency



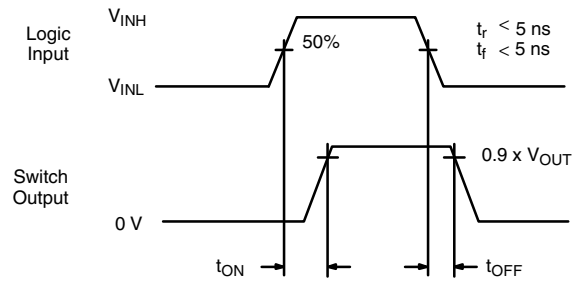
Switching Threshold vs. Supply Voltage

TEST CIRCUITS



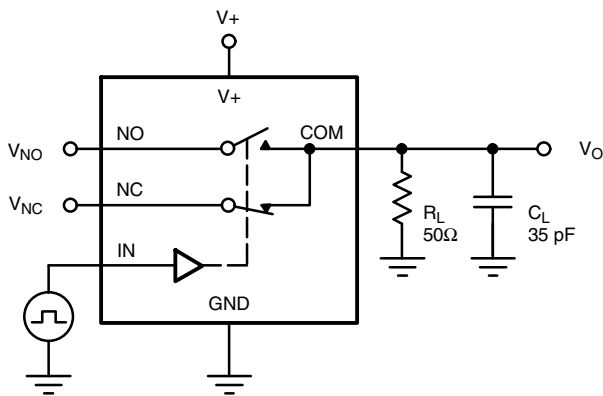
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
 Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

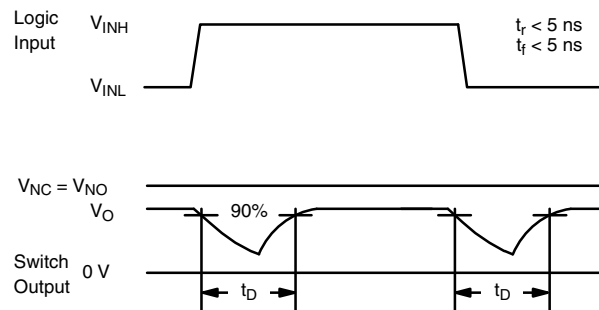
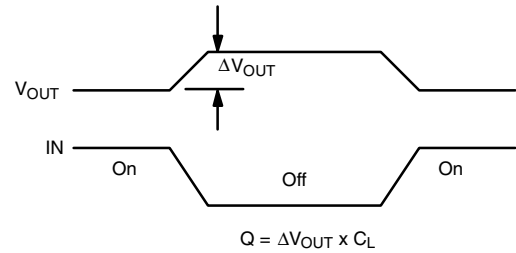
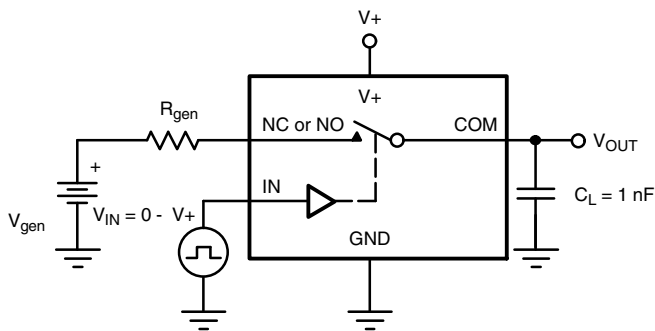
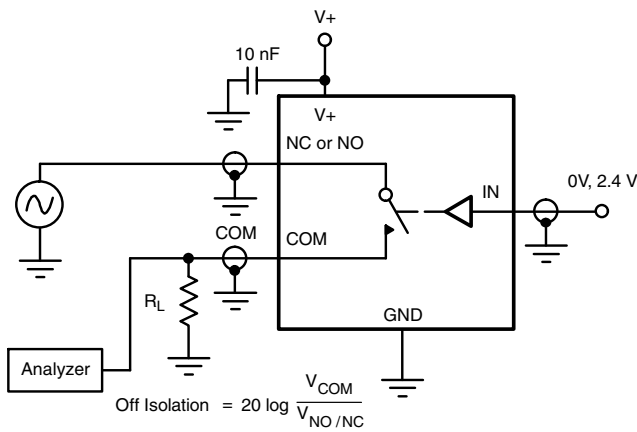
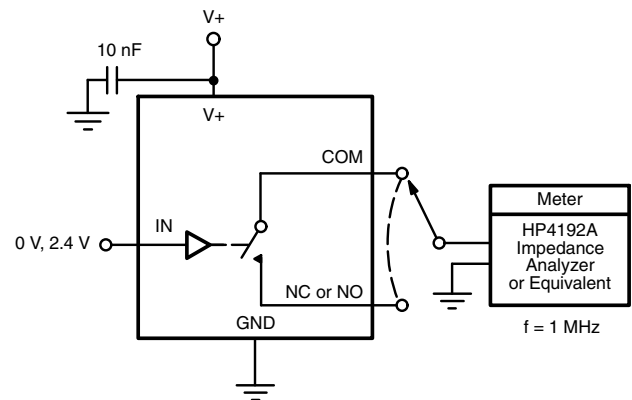


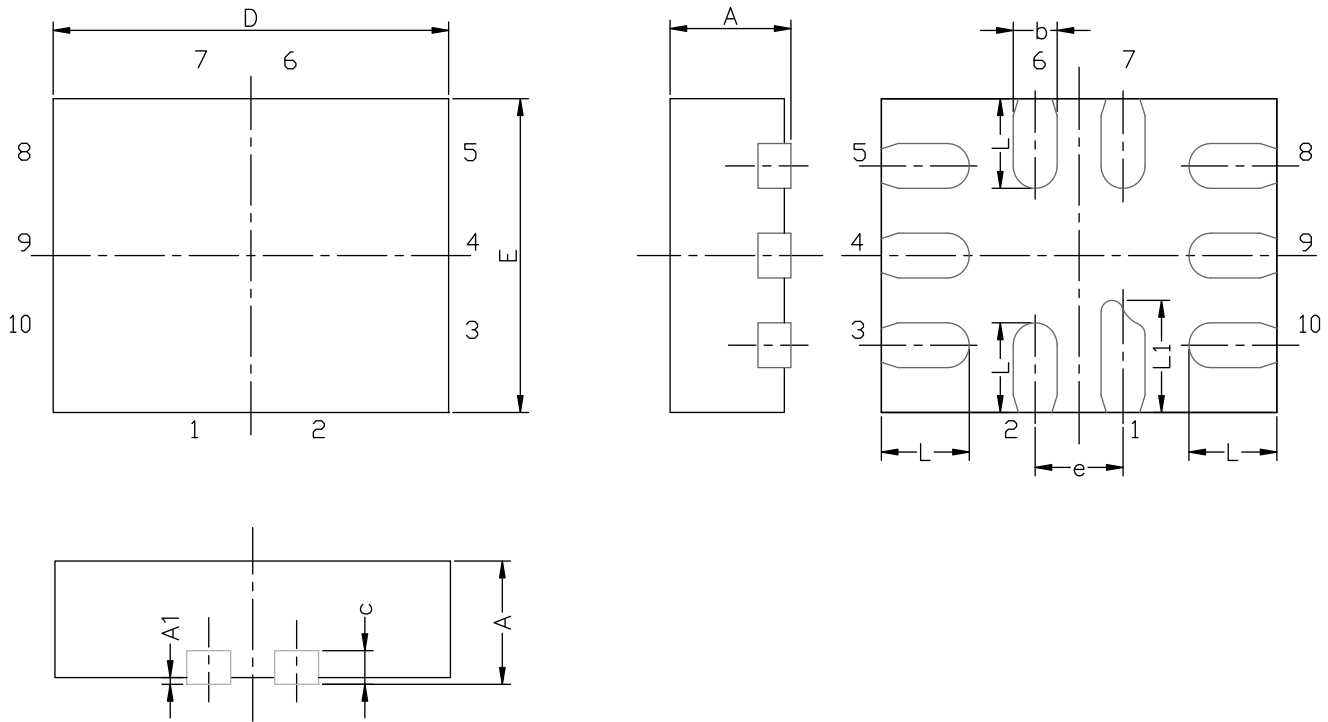
Figure 2. Break-Before-Make Interval

TEST CIRCUITS


IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

Figure 4. Off-Isolation

Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74420.

MINI QFN-10L CASE OUTLINE


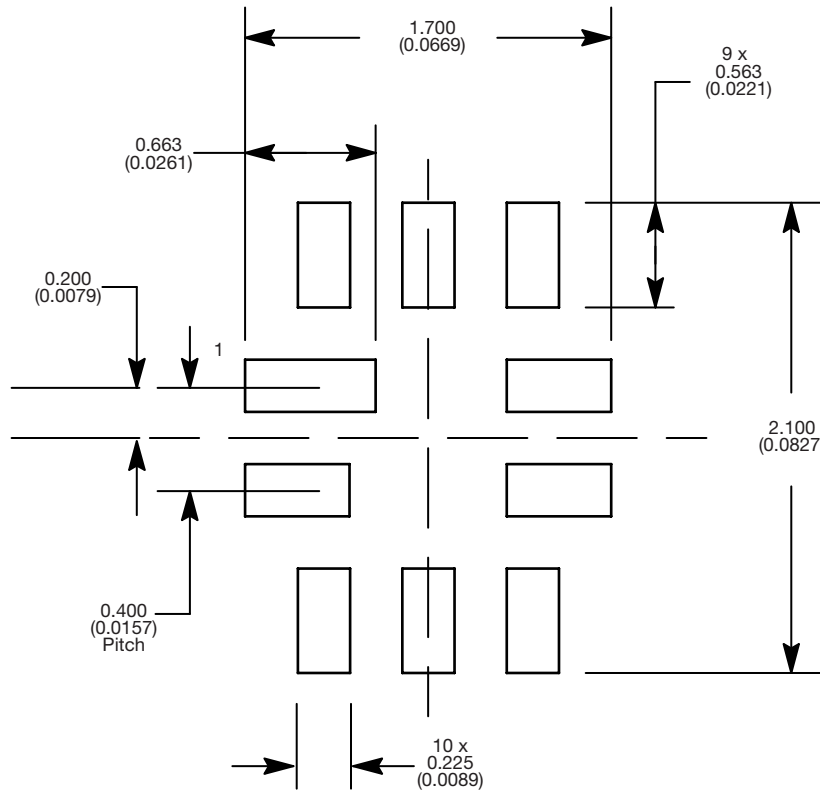
DIM	MILLIMETERS			INCHES		
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.
A	0.45	0.55	0.60	0.0177	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.150 or 0.127 REF ⁽¹⁾			0.006 or 0.005 REF ⁽¹⁾		
D	1.70	1.80	1.90	0.067	0.071	0.075
E	1.30	1.40	1.50	0.051	0.055	0.059
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

Note

⁽¹⁾ The dimension depends on the leadframe that assembly house used.

ECN T16-0163-Rev. B, 16-May-16
DWG: 5957

RECOMMENDED MINIMUM PADS FOR MINI QFN 10L



Mounting Footprint
Dimensions in mm (inch)



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