N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
30	0.0095 at V_{GS} = 10 V	18.2	9.2 nC
	0.014 at V_{GS} = 4.5 V	15	

FEATURES

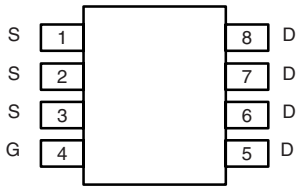
- **Halogen-free According to IEC 61249-2-21 Available**
- Extremely Low Q_{gd} WFET® Technology for Low Switching Losses
- TrenchFET® Power MOSFETs
- 100 % R_g Tested

RoHS COMPLIANT
HALOGEN FREE Available

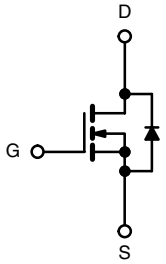
APPLICATIONS

- High-Side DC/DC Conversion
  - Notebook
  - Server

SO-8



Top View



N-Channel MOSFET

Ordering Information: Si4686DY-T1-E3 (Lead (Pb)-free)
Si4686DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	18.2	A
	T_C = 70 °C		14.5	
	T_A = 25 °C		13.8[b, c]	
	T_A = 70 °C		11[b, c]	
Pulsed Drain Current		I_{DM}	50	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	4.3	
	T_A = 25 °C		2.5[b, c]	
Single-Pulse Avalanche Current	L = 0.1 mH	I_{AS}	10	
Single-Pulse Avalanche Energy		E_{AS}	5	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	5.2	W
	T_C = 70 °C		3.3	
	T_A = 25 °C		3.0[b, c]	
	T_A = 70 °C		1.9[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)				

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	35	42	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	20	24	

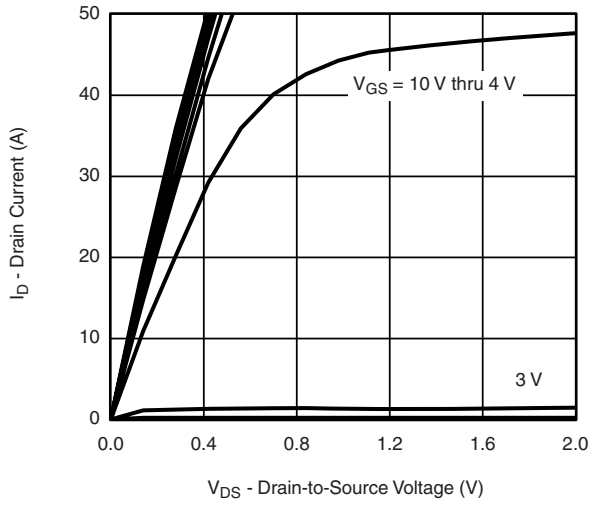
Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under Steady State conditions is 80 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		31.3		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 13.8 A		0.0078	0.0095	Ω
		V_{GS} = 4.5 V, I_D = 11.4 A		0.011	0.014	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 13.8 A		56		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		1220		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			98		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 13.8 A		17	26	nC
		V_{DS} = 15 V, V_{GS} = 5 V, I_D = 13.8 A		9.2	14	
Gate-Source Charge	Q_{gs}			4.1		
Gate-Drain Charge	Q_{gd}			2.8		
Gate Resistance	R_g	f = 1 MHz		0.8	1.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		20	30	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			8	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		13	20	
Rise Time	t_r			16	25	
Turn-Off Delay Time	$t_{d(off)}$			23	35	
Fall Time	t_f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			4.3	A
Pulse Diode Forward Current[a]	I_{SM}				50	
Body Diode Voltage	V_{SD}	I_S = 2.6 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 2.6 A, dI/dt = 100 A/µs, T_J = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			15	30	nC
Reverse Recovery Fall Time	t_a			12.5		ns
Reverse Recovery Rise Time	t_b			12.5		

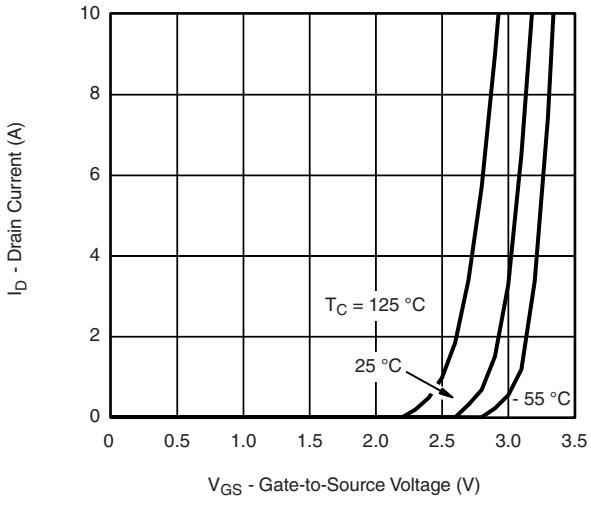
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

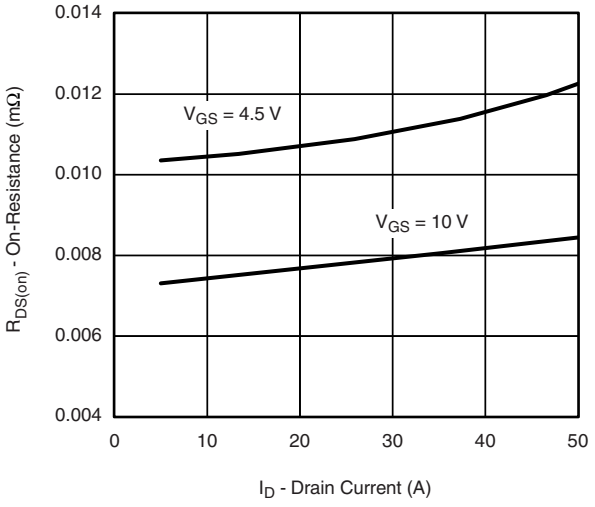
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



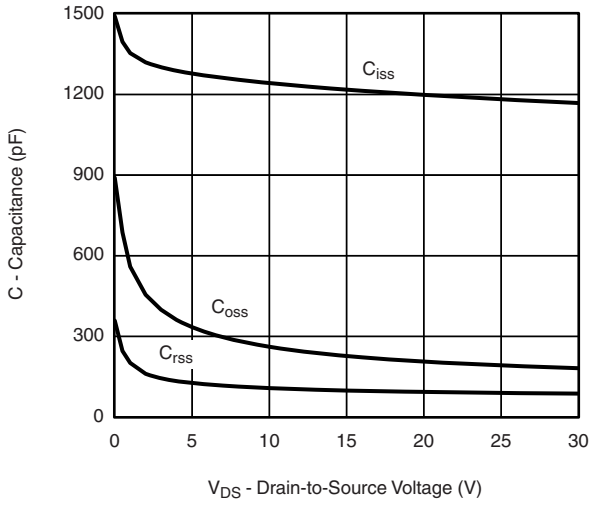
Output Characteristics



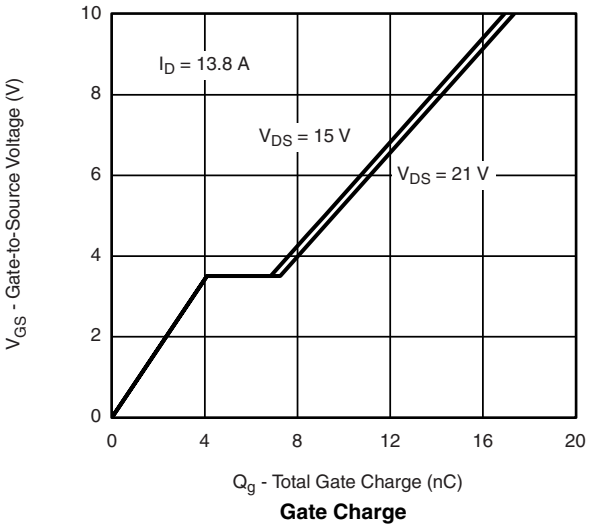
Transfer Characteristics



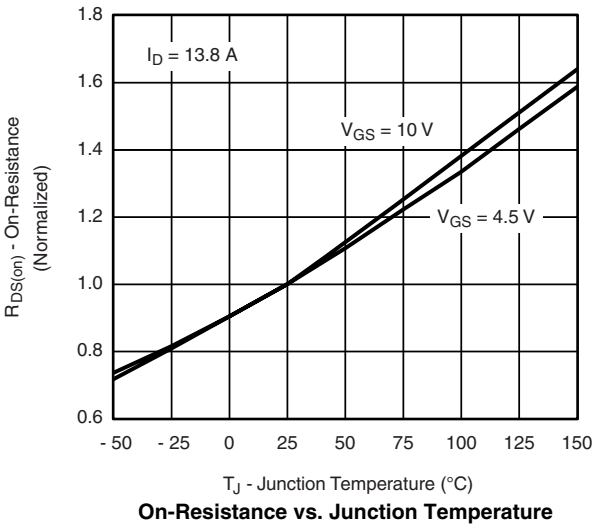
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

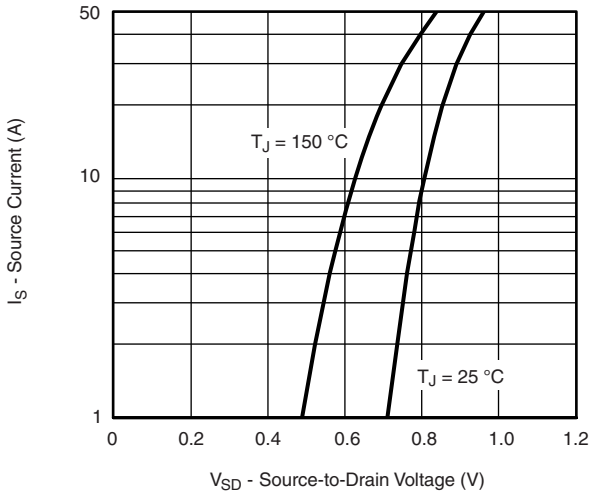


Gate Charge

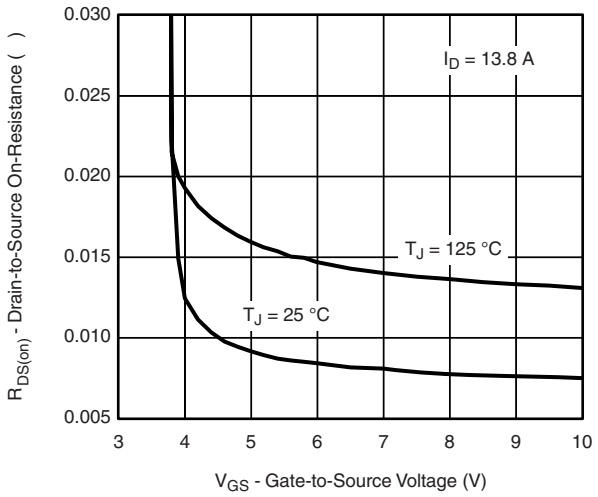


On-Resistance vs. Junction Temperature

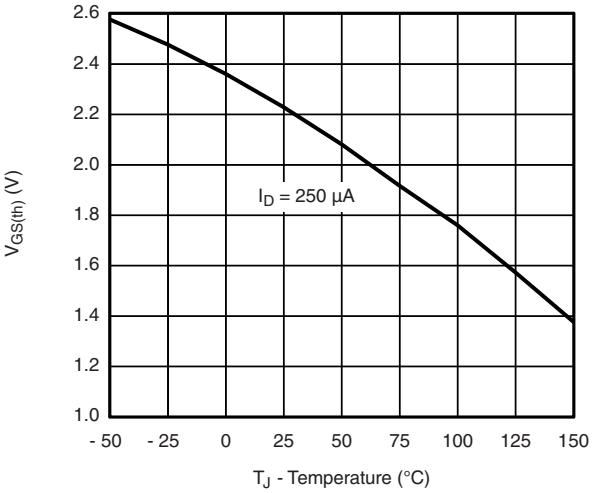
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



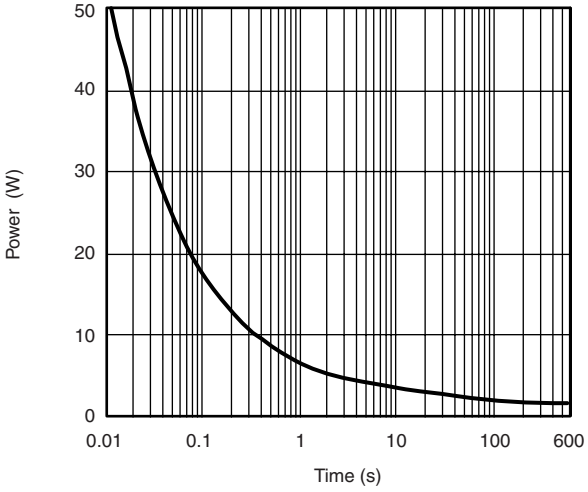
Source-Drain Diode Forward Voltage



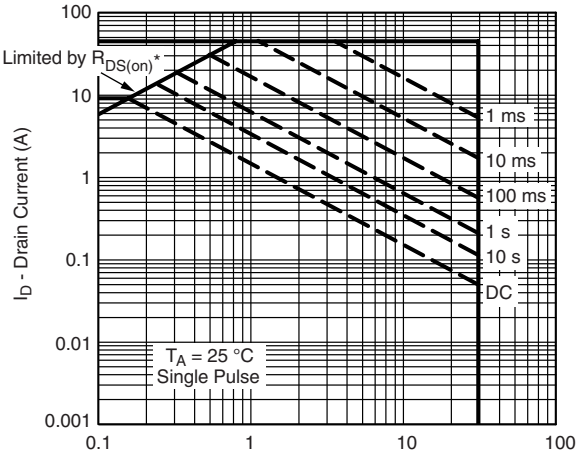
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



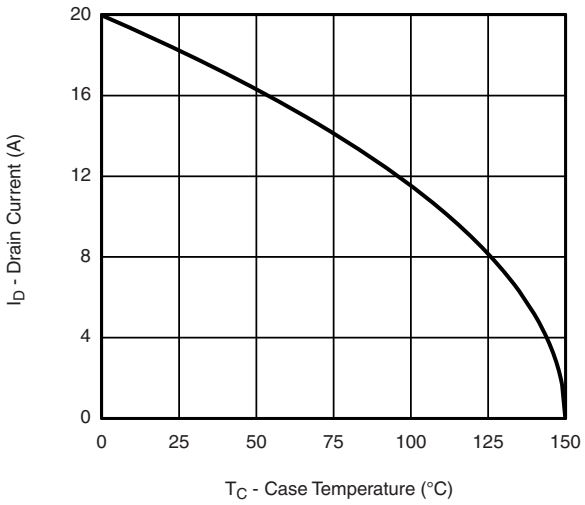
Single Pulse Power, Junction-to-Ambient



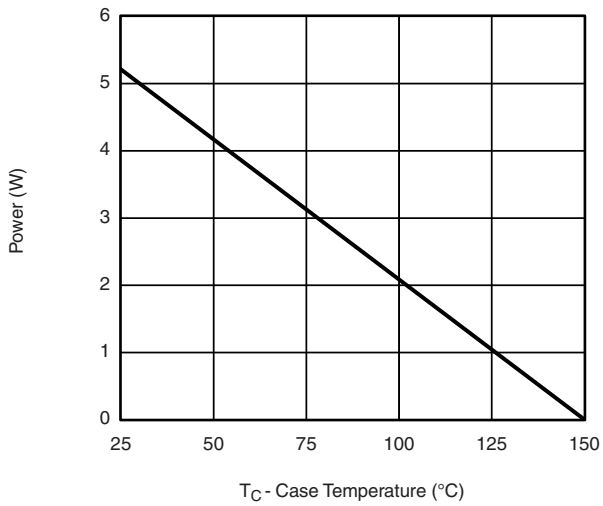
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



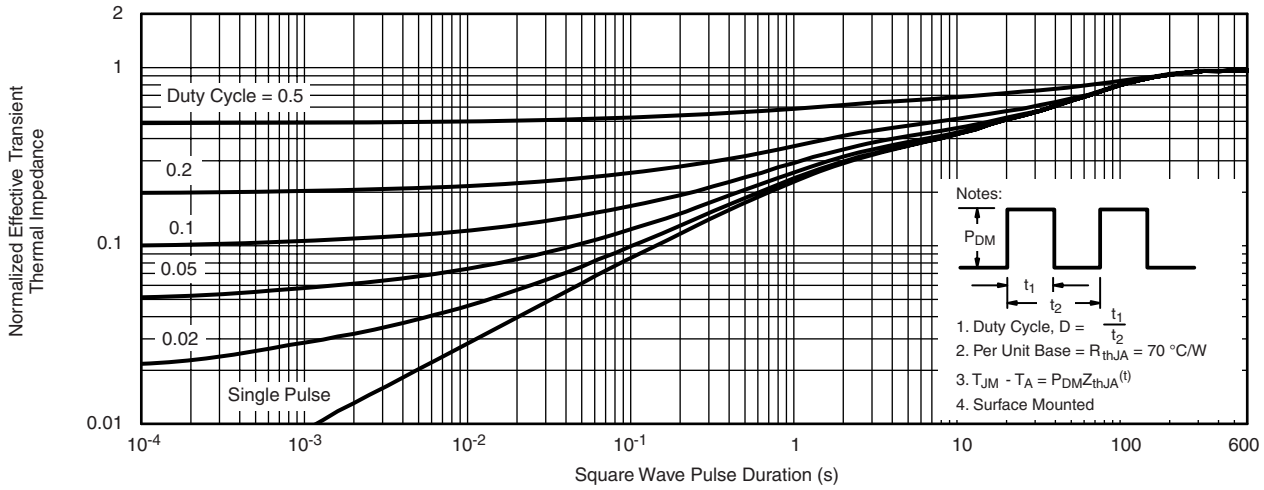
Current Derating*



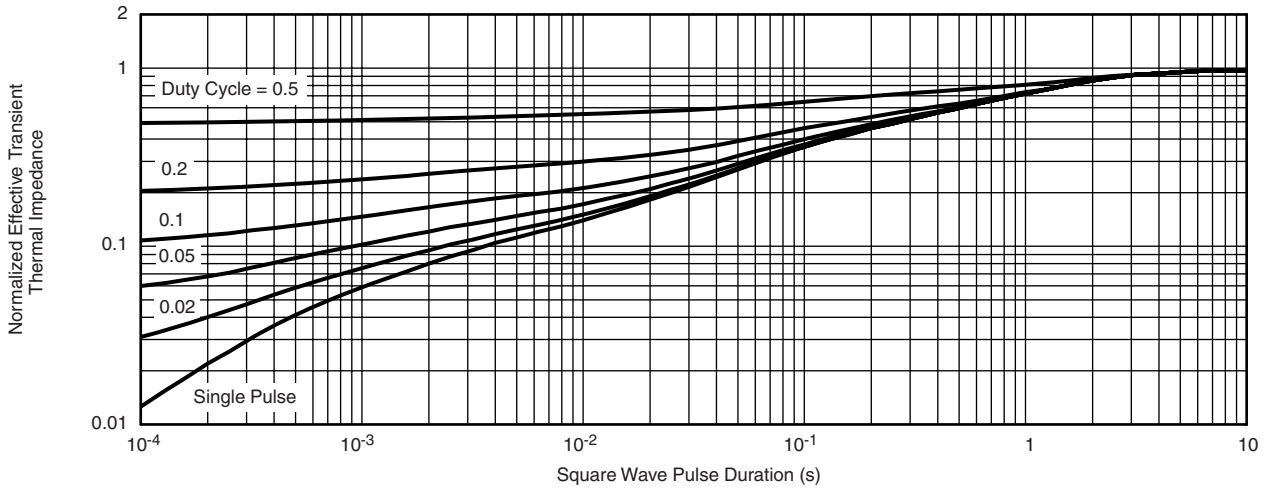
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



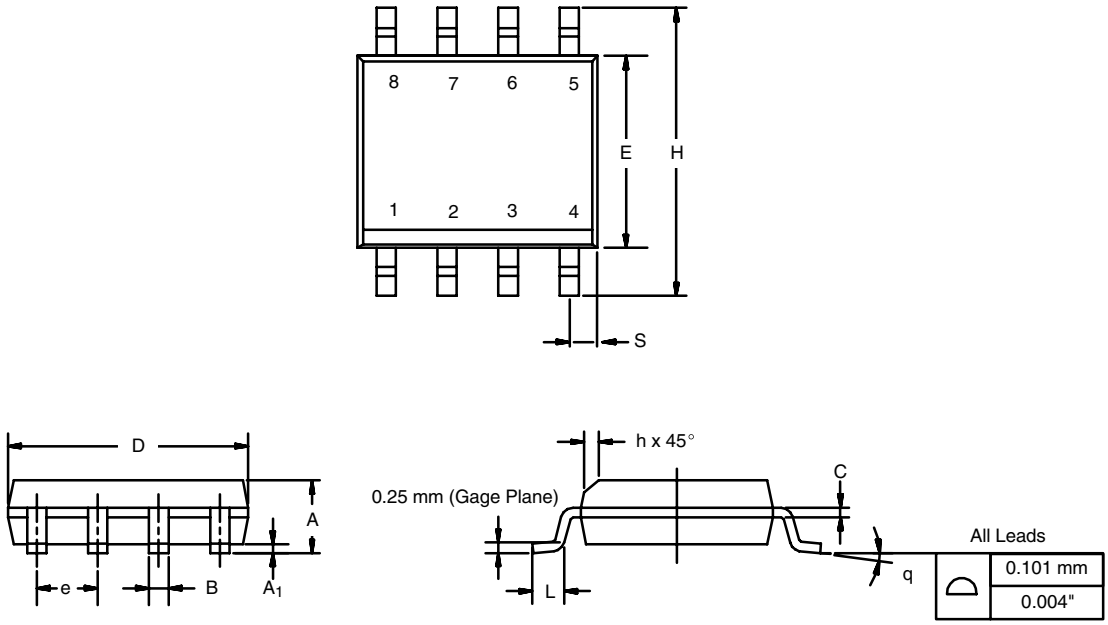
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

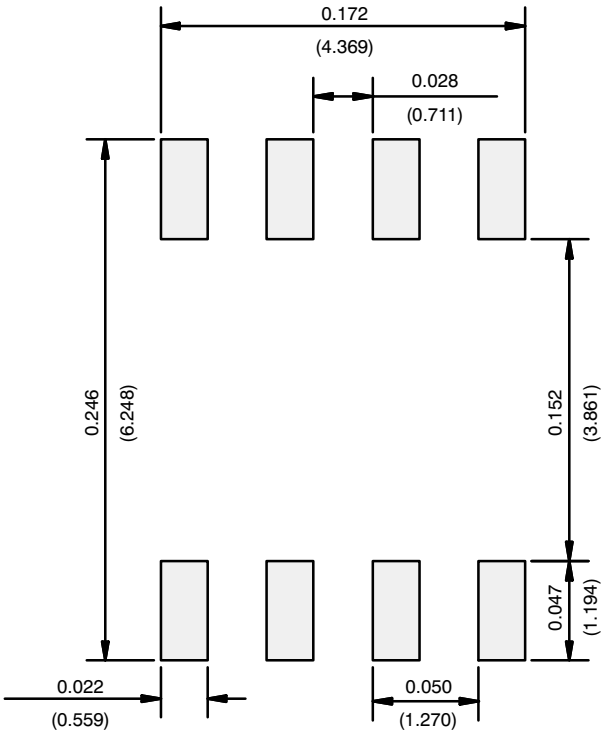
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73422.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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