3-Ω, High Bandwidth, Dual SPDT Analog Switch

DESCRIPTION

The DG2517, DG2518 are low-voltage dual single-pole/double-throw monolithic CMOS analog switches. Designed to operate from 1.8 V to 5.5 V power supply, the DG2517, DG2518 achieves a bandwidth of 242 MHz while providing low on-resistance (3 Ω), excellent on-resistance matching (0.2 Ω) and flatness (1 Ω) over the entire signal range.

The DG2517, DG2518 offers the advantage of high linearity that reduces signal distortion, making ideal for audio, video, and USB signal routing applications. Additionally, the DG2517, DG2518 are 1.6 V logic compatible within the full operation voltage range.

Built on Vishay Siliconix's proprietary sub-micron high-density process, the DG2517, DG2518 brings low power consumption at the same time as reduces PCB spacing with the MSOP10 and DFN10 packages.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. The DFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The MSOP package uses 100 % matte Tin device termination and is represented by the lead (Pb)- free "-E3" suffix. Both the matte Tin and nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

- 1.8 V to 5.5 V single supply operation
- Low R_{ON}: 3 Ω at 4.2 V
- 242 MHz, - 3 dB bandwidth
- Low off-isolation, - 51 dB at 10 MHz
- + 1.6 V logic compatible

Pb-free
RoHS
COMPLIANT

BENEFITS

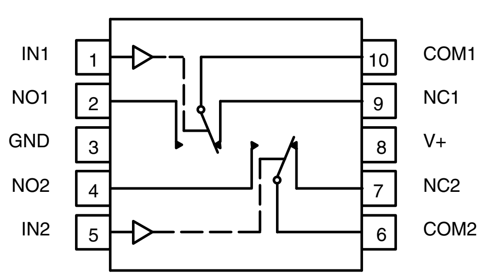
- High linearity
- Low power consumption
- High bandwidth
- Full rail signal swing range

APPLICATIONS

- USB/UART signal switching
- Audio/video switching
- Cellular phone
- Media players
- Modems
- Hard drives
- PCMCIA

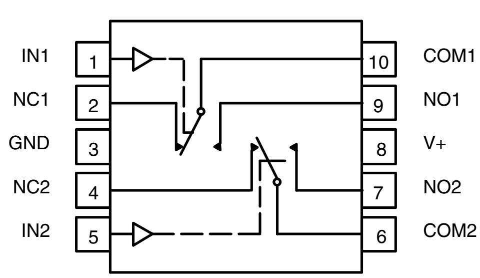
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2517



Top View

DG2518



Top View

TRUTH TABLE		
Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	MSOP-10	DG2517DQ-T1-E3
		DG2518DQ-T1-E3
	DFN-10	DG2517DN-T1-E4
		DG2518DN-T1-E4

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
Reference to GND			
V+		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages)[b]	MSOP-10[c]	320	mW
	DFN-10[d]	1191	

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 4.0 mW/°C above 70 °C.
d. Derate 14.9 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.5 or 1.4 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 1.5 V $I_{NO/NC}$ = 10 mA		Room Full		3.2	4.5 5.0	Ω
R_{ON} Flatness	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 1.5, 2 V $I_{NO/NC}$ = 10 mA		Room Full		1.0	1.4 16	
R_{ON} Match Between Channels	ΔR_{ON}	V+ = 2.7 V, V_{COM} = 1.5 V $I_{NO/NC}$ = 10 mA		Room Full		0.1	0.3 0.4	
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.6 V, V_{NO}, V_{NC} = 0.3 V/ 3 V V_{COM} = 3 V/0.3 V		Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$			Room Full	- 1 - 10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.6 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V		Room Full	- 1 - 10		1 10	
Digital Control								
Input High Voltage[d]	V_{INH}			Full	1.4			V
Input Low Voltage	V_{INL}			Full			0.5	
Input Capacitance	C_{in}			Full		4		pF
Input Current	I_{INL} or I_{INH}			Full	1		1	µA
Dynamic Characteristics								
Turn-On Time	t_{ON}	V+ = 2.7 V, V_{NO} or V_{NC} = 1.5 V R_L = 300 Ω, C_L = 35 pF		Room Full		15	30 50	ns
Turn-Off Time	t_{OFF}			Room Full		10	25 35	
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF		Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 1.5 V, R_{GEN} = 0 Ω		Room		1		pC
- 3 dB Bandwidth	BW	0 dBm, C_L = 5 pF, R_L = 50 Ω		Room		242		MHz
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 71		dB
			f = 10 MHz	Room		- 51		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 73		
			f = 10 MHz	Room		- 55		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		8		pF
	$C_{NC(off)}$			Room		8		
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		35		
	$C_{NC(on)}$			Room		35		
Power Supply								
Power Supply Current	I+	V_{IN} = 0 or V+		Full		0.01	1.0	µA

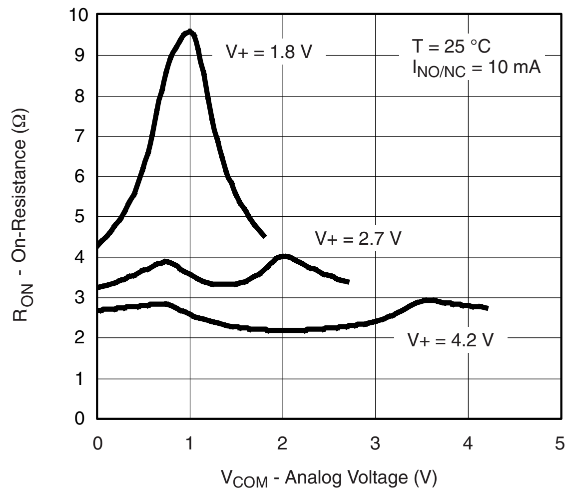
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

SPECIFICATIONS (V+ = 5 V)								
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 5 V, ± 10 %, V_{IN} = 0.8 or 2.0 V[e]		**Temp.**[a]	**Limits - 40 °C to 85 °C Min.**[b]	**Typ.**[c]	**Max.**[b]	**Unit**
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance	R_{ON}	V+ = 4.2 V, V_{COM} = 3.5 V, $I_{NO/NC}$ = 10 mA		Room Full		3	4.0 4.3	Ω
R_{ON} Flatness	R_{ON} Flatness	V+ = 4.2 V, V_{COM} = 1, 2, 3.5 V $I_{NO/NC}$ = 10 mA		Room Full		1.1	1.4 1.6	Ω
R_{ON} Match Between Channels	ΔR_{ON}	V+ = 4.2 V, V_{COM} = 3.5 V, $I_{NO/NC}$ = 10 mA		Room Full		0.1	0.3 0.4	Ω
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V		Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$			Room Full	- 1 - 10		1 10	nA
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{COM} = V_{NO}, V_{NC} = 1 V/4.5 V		Room Full	- 1 - 10		1 10	nA
Digital Control								
Input High Voltage[d]	V_{INH}			Full	2.0			V
Input Low Voltage	V_{INL}			Full			0.8	V
Input Capacitance	C_{in}			Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+		Full	1		1	µA
Dynamic Characteristics								
Turn-On Time	t_{ON}	V+ = 4.2 V, V_{NO} or V_{NC} = 3 V R_L = 300 Ω, C_L = 35 pF		Room Full		12	25 45	ns
Turn-Off Time	t_{OFF}			Room Full		8	20 30	ns
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF		Full	1			ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 2.5 V, R_{GEN} = 0 Ω		Room		2		pC
- 3 dB Bandwidth	BW	0 dBm, C_L = 5 pF, R_L = 50 Ω		Room		242		MHz
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 71		dB
			f = 10 MHz	Room		- 51		dB
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 73		dB
			f = 10 MHz	Room		- 55		dB
Source-Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		8		pF
	$C_{NC(off)}$			Room		8		pF
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		35		pF
	$C_{NC(on)}$			Room		35		pF
Power Supply								
Power Supply Range	V+				1.8		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+		Full		0.01	1.0	µA

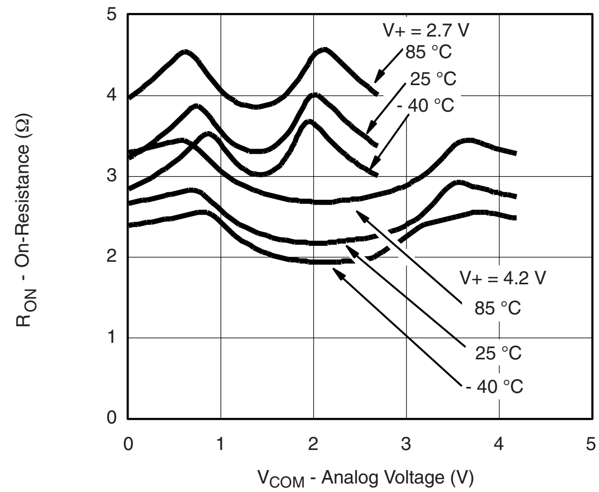
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

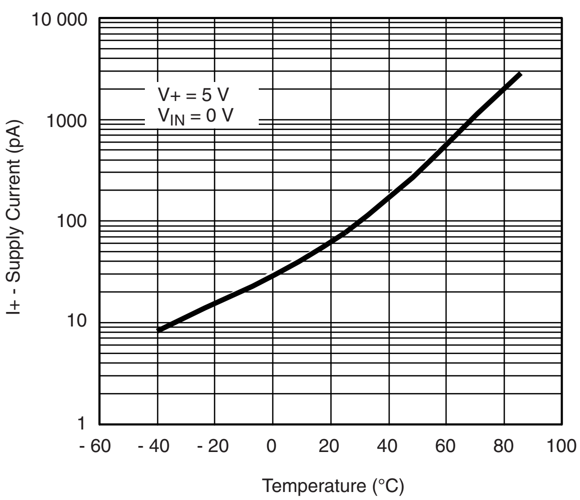
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



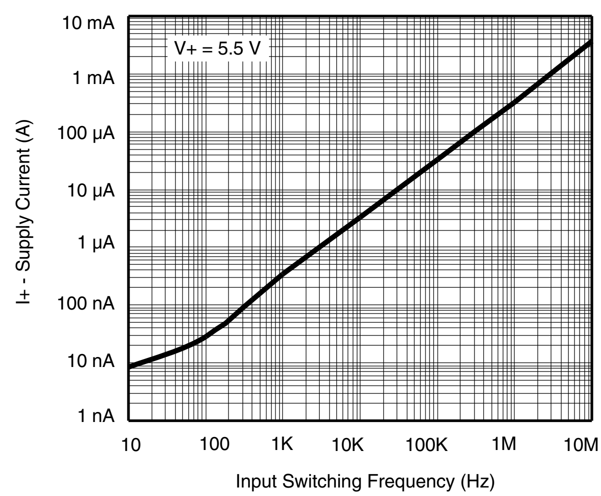
R_{ON} vs. V_{COM} and Supply Voltage



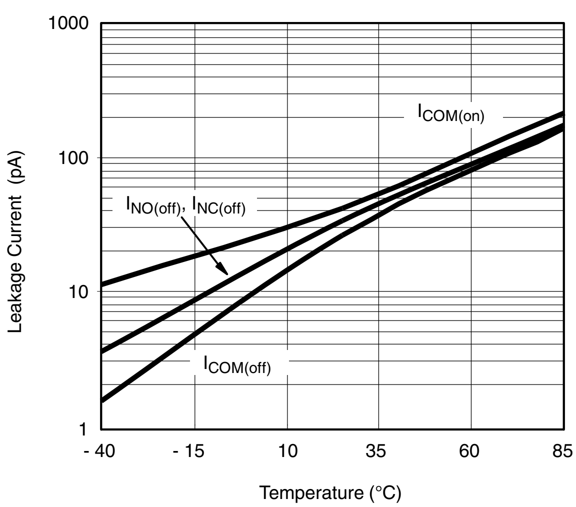
R_{ON} vs. Analog Voltage and Temperature



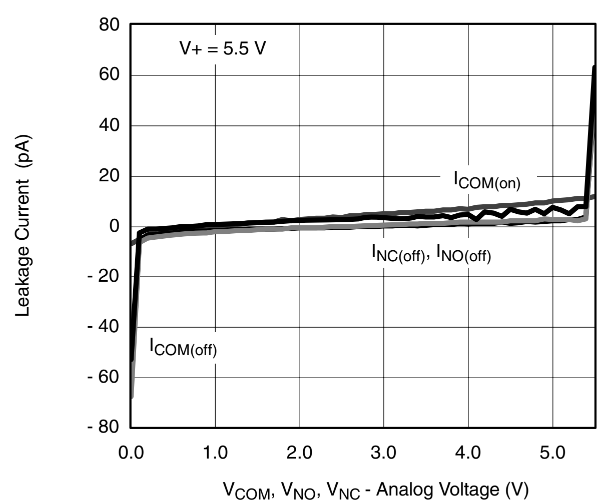
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

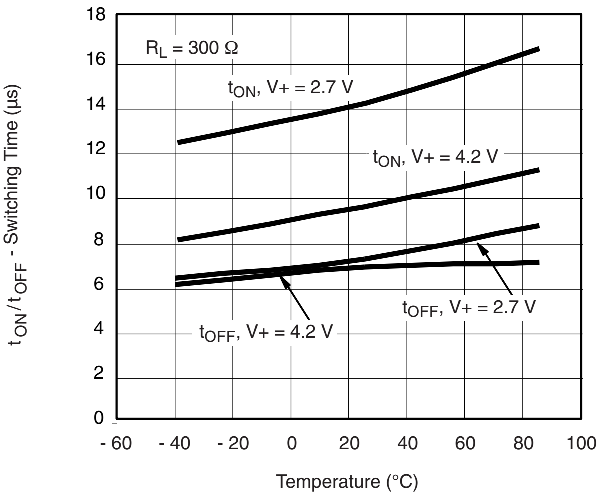


Leakage Current vs. Temperature

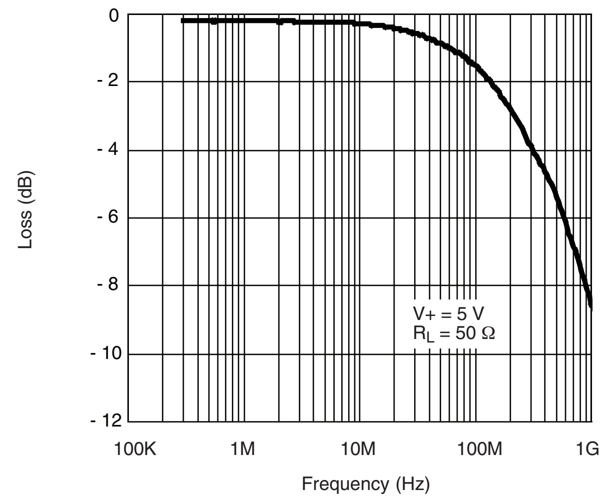


Leakage vs. Analog Voltage

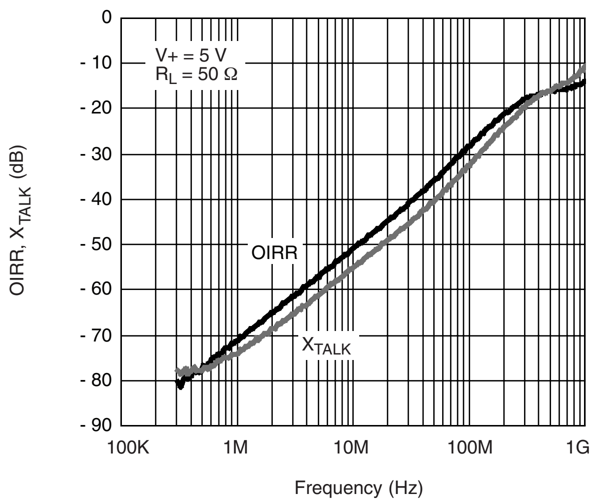
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



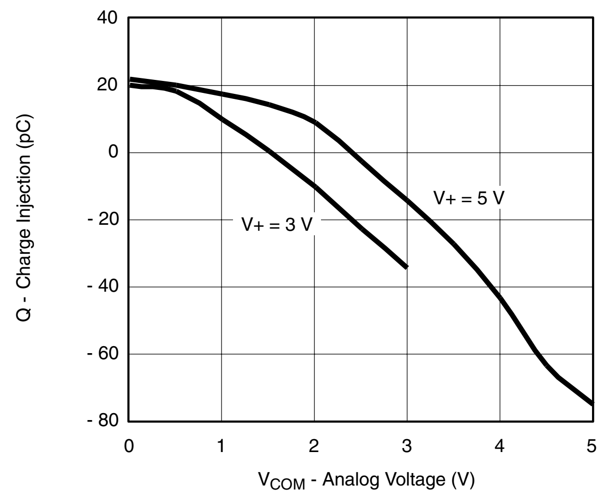
Switching Time vs. Temperature



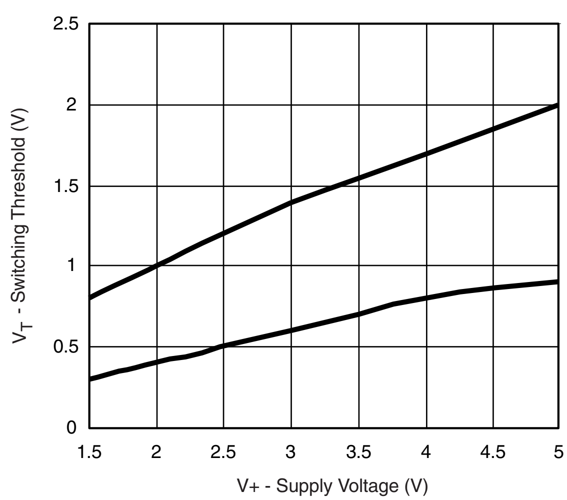
Insertion Loss vs. Frequency



Off-Isolation and Crosstalk vs. Frequency

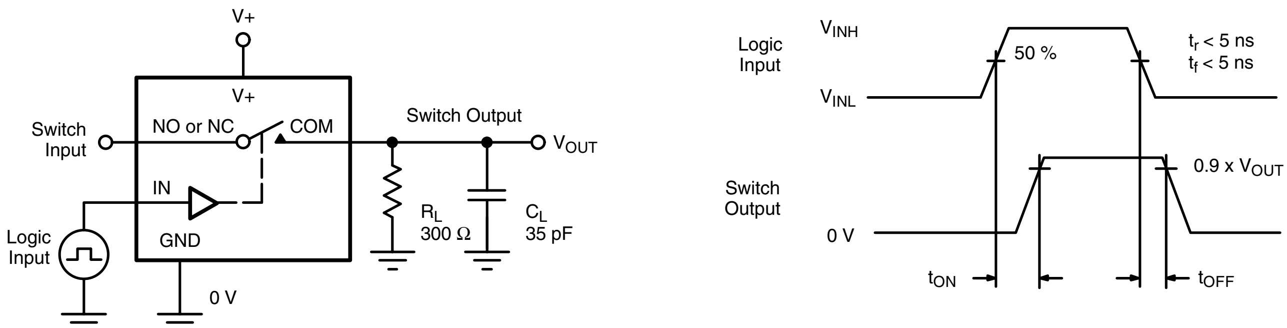


Charge Injection vs. Analog Voltage



Switching Threshold vs. Supply Voltage

TEST CIRCUITS

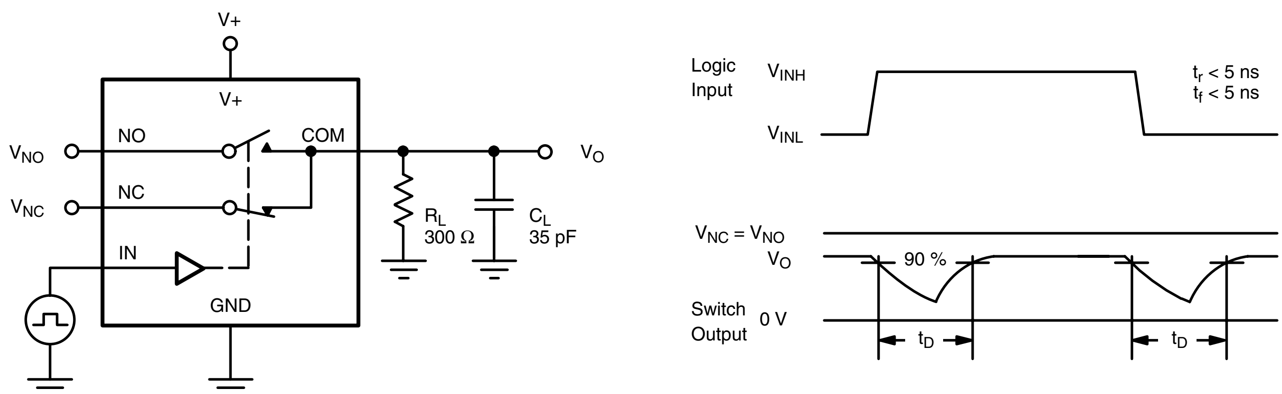


C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

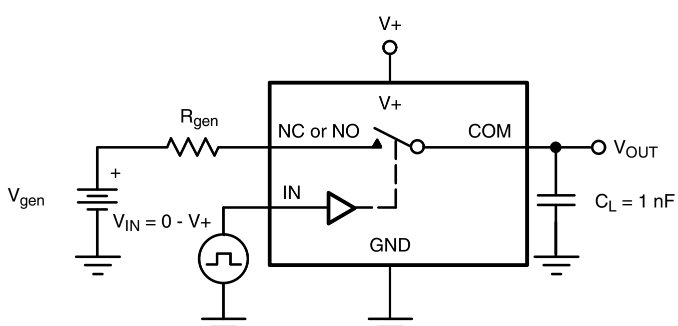
Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

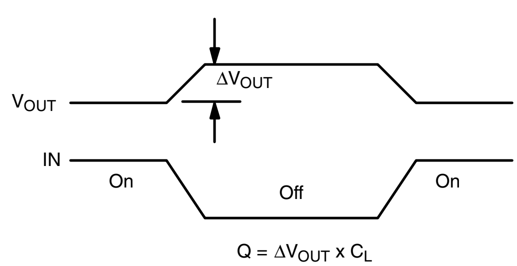
Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval





IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

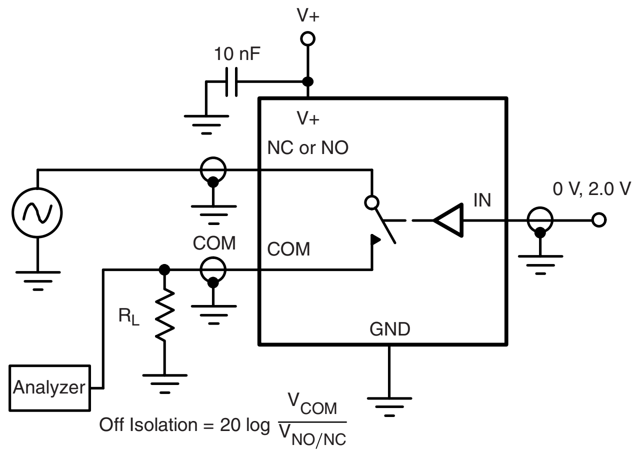


Figure 4. Off-Isolation

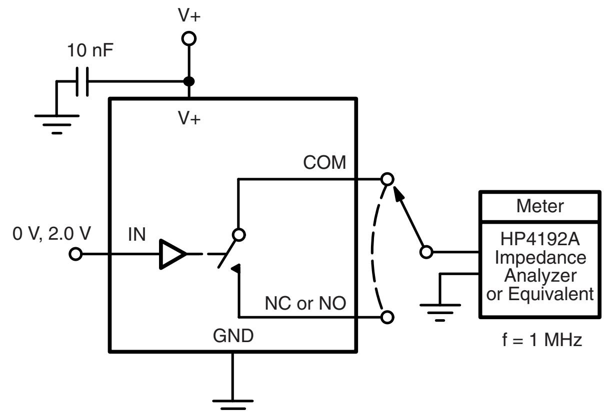
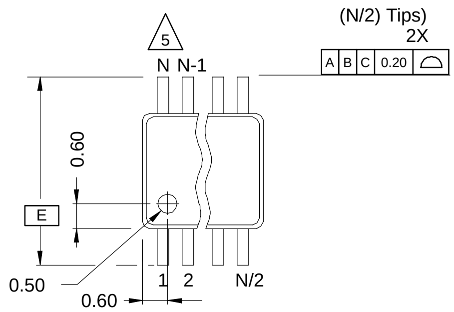


Figure 5. Channel Off/On Capacitance

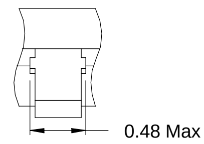
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?74333.

MSOP: 10-LEADS

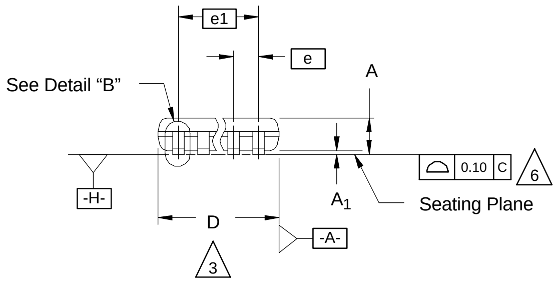
JEDEC Part Number: MO-187, (Variation AA and BA)



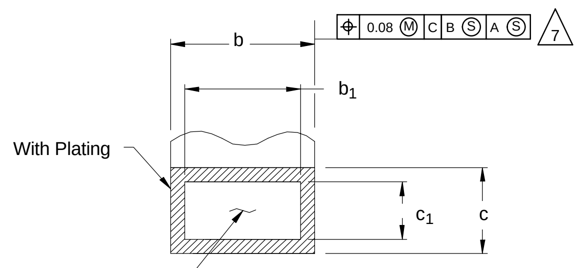
Top View



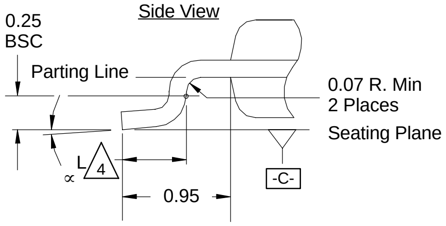
Detail "B"
(Scale: 30/1)
Dambar Protrusion



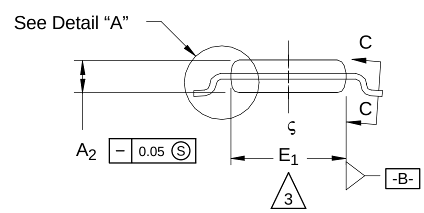
Side View



Section "C-C"
Scale: 100/1
(See Note 8)



Detail "A"
(Scale: 30/1)



End View

NOTES:

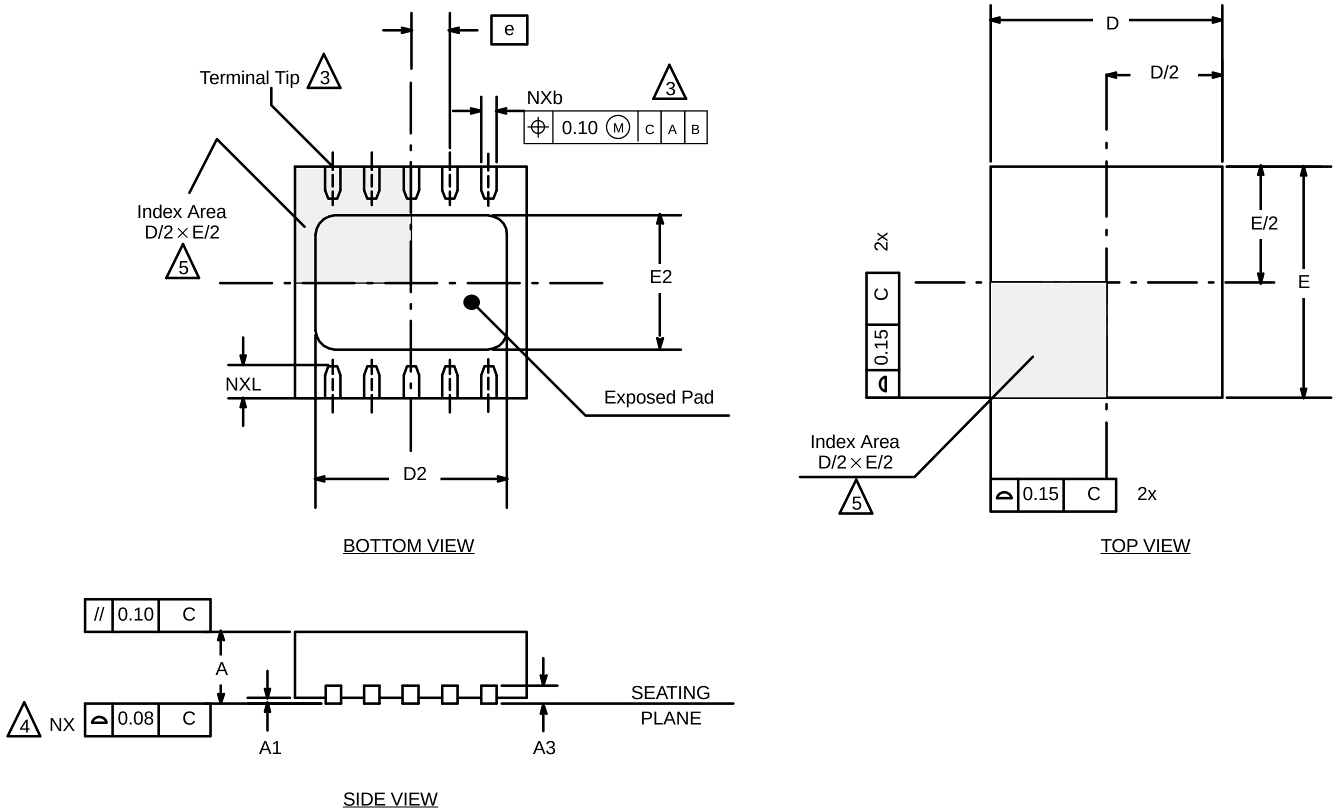
1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

	MILLIMETERS			
Dim	**Min**	**Nom**	**Max**	**Note**
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	-	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D		3.00 BSC		3
E		4.90 BSC		
E_1	2.90	3.00	3.10	3
e		0.50 BSC		
e_1		2.00 BSC		
L	0.40	0.55	0.70	4
N		10		5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

DFN-10 LEAD (3 X 3)



NOTES:

1. All dimensions are in millimeters and inches.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

	MILLIMETERS			INCHES		
Dim	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 BSC			0.008 BSC	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	2.20	2.38	2.48	0.087	0.094	0.098
E		3.00 BSC			0.118 BSC	
E2	1.49	1.64	1.74	0.059	0.065	0.069
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
*Use millimeters as the primary measurement.						
ECN: S-42134—Rev. A, 29-Nov-04 DWG: 5943						

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