




## Standard Recovery Diodes (MAGN-A-PAK Power Modules), 250 A to 320 A



MAGN-A-PAK

### FEATURES

- High voltage
- Electrically isolated base plate
- 3000 V<sub>RMS</sub> isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL approved file E78996 
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
COMPLIANT

PRIMARY CHARACTERISTICS	
I <sub>F(AV)</sub>	250 A to 320 A
Type	Modules - diode, high voltage
Package	MAGN-A-PAK
Circuit configuration	Two diodes doubler circuit, two diodes common cathode, single diode

### DESCRIPTION / APPLICATIONS

This VS-VSK series of MAGN-A-PAKs uses high voltage power diodes in two basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges and the single diode module can be used in conjunction with the thyristor modules as a freewheel diode.

These modules are intended for general purpose applications such as battery chargers, welders and plating equipment and where high voltage and high current are required (motor drives, etc.)

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VSK.250..	VSK.270..	VSK.320..	UNITS
I <sub>F(AV)</sub>		250	270	320	A
	T <sub>C</sub>	100	100	100	°C
I <sub>F(RMS)</sub>		393	424	502	A
I <sub>FSM</sub>	50 Hz	7015	8920	10 110	
	60 Hz	7345	9430	10 580	
I <sup>2</sup> t	50 Hz	246	398	511	kA <sup>2</sup> s
	60 Hz	225	363	466	
I <sup>2</sup> √t		2460	3980	5110	kA <sup>2</sup> √s
V <sub>RRM</sub>		400 to 2000	400 to 3000	400 to 2000	V
T <sub>J</sub>		-40 to +150			°C



**ELECTRICAL SPECIFICATIONS**

<b>VOLTAGE RATINGS</b>				
TYPE NUMBER	VOLTAGE CODE	V <sub>RRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> MAXIMUM AT 150 °C mA
VS-VSK.270 VS-VSK.320	04	400	500	50
VS-VSK.250 VS-VSK.270 VS-VSK.320	08	800	900	
	12	1200	1300	
	16	1600	1700	
	20	2000	2100	
VS-VSK.270	30	3000	3100	

<b>FORWARD CONDUCTION</b>								
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES			UNITS
					VSK.250	VSK.270	VSK.320	
Maximum average forward current at case temperature	I <sub>F(AV)</sub>	180° conduction, half sine wave			250	270	320	A
					100	100	100	°C
Maximum RMS forward current	I <sub>F(RMS)</sub>	As AC switch			393	424	502	A
Maximum peak, one-cycle forward, non-repetitive surge current	I <sub>FSM</sub>	t = 10 ms	No voltage reappplied	Sinusoidal half wave, initial T <sub>J</sub> = T <sub>J</sub> maximum	7015	8920	10 110	
		t = 8.3 ms			7345	9340	10 580	
		t = 10 ms	100 % V <sub>RRM</sub> reappplied		5900	7500	8500	
		t = 8.3 ms			6180	7850	8900	
Maximum I <sup>2</sup> t for fusing	I <sup>2</sup> t	t = 10 ms	No voltage reappplied		246	398	511	
		t = 8.3 ms			225	363	466	
		t = 10 ms	100 % V <sub>RRM</sub> reappplied	174	281	361		
		t = 8.3 ms		159	257	330		
Maximum I <sup>2</sup> √t for fusing	I <sup>2</sup> √t	t = 0.1 ms to 10 ms, no voltage reappplied			2460	3980	5110	kA <sup>2</sup> √s
Low level value of threshold voltage	V <sub>F(TO)1</sub>	(16.7 % × π × I <sub>F(AV)</sub> ) < I < π × I <sub>F(AV)</sub> , T <sub>J</sub> = T <sub>J</sub> maximum			0.79	0.74	0.69	V
High level value of threshold voltage	V <sub>F(TO)2</sub>	I > π × I <sub>F(AV)</sub> , T <sub>J</sub> = T <sub>J</sub> maximum			0.92	0.87	0.86	
Low level forward slope resistance	r <sub>f1</sub>	(16.7 % × π × I <sub>F(AV)</sub> ) < I < π × I <sub>F(AV)</sub> , T <sub>J</sub> = T <sub>J</sub> maximum			0.63	0.94	0.59	mΩ
High level forward slope resistance	r <sub>f2</sub>	I > π × I <sub>F(AV)</sub> , T <sub>J</sub> = T <sub>J</sub> maximum			0.49	0.81	0.44	
Maximum forward voltage drop	V <sub>FM</sub>	I <sub>FM</sub> = π × I <sub>F(AV)</sub> , T <sub>J</sub> = T <sub>J</sub> maximum, 180° conduction Average power = V <sub>F(TO)</sub> × I <sub>F(AV)</sub> + r <sub>f</sub> × (I <sub>F(RMS)</sub> ) <sup>2</sup>			1.29	1.48	1.28	V

<b>BLOCKING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse leakage current	I <sub>RRM</sub>	T <sub>J</sub> = 150 °C	50	mA
RMS insulation voltage	V <sub>INS</sub>	50 Hz, circuit to base, all terminals shorted, t = 1 s	3000	V



THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES			UNITS
			VSK.250	VSK.270	VSK.320	
Maximum junction operating and storage temperature range	$T_J, T_{Stg}$		-40 to +150			°C
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation	0.16	0.125	0.125	K/W
Maximum resistance, case to heat sink per module	$R_{thCS}$	Mounting surface flat, smooth and greased	0.035			
Mounting torque $\pm 10\%$	MAGN-A-PAK to heatsink Busbar to MAGN-A-PAK	A mounting compound is recommended and the torque should be rechecked after a period of about 3 hours to allow for the spread of the compound.	4 to 6			Nm
Approximate weight			800			g
			30		oz.	
Case style			MAGN-A-PAK			

ΔR CONDUCTION PER JUNCTION											
DEVICE	SINUSOIDAL CONDUCTION AT $T_J$ MAXIMUM					RECTANGULAR CONDUCTION AT $T_J$ MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.250	0.009	0.010	0.014	0.020	0.032	0.007	0.011	0.015	0.021	0.033	K/W
VSK.270	0.008	0.012	0.014	0.020	0.032	0.007	0.011	0.015	0.020	0.033	
VSK.320	0.008	0.010	0.013	0.020	0.032	0.007	0.011	0.015	0.020	0.033	

**Note**

- The table above shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

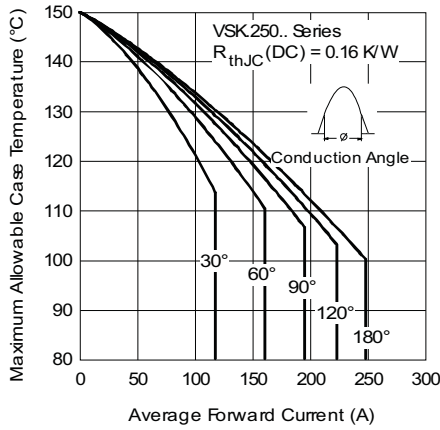


Fig. 1 - Current Ratings Characteristics

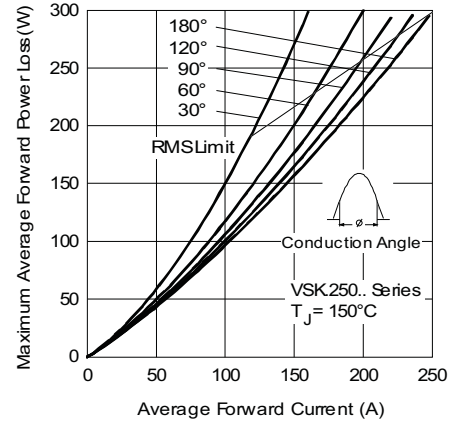


Fig. 3 - Forward Power Loss Characteristics

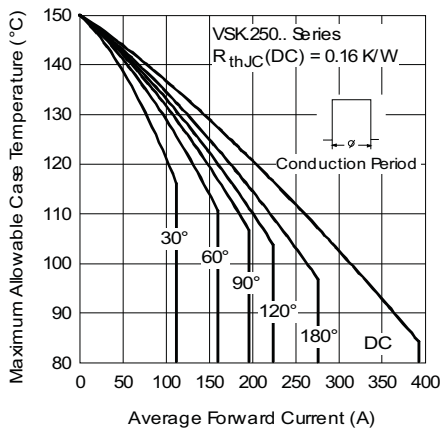


Fig. 2 - Current Ratings Characteristics

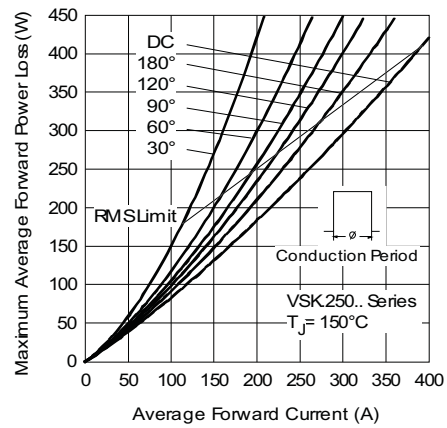


Fig. 4 - Forward Power Loss Characteristics

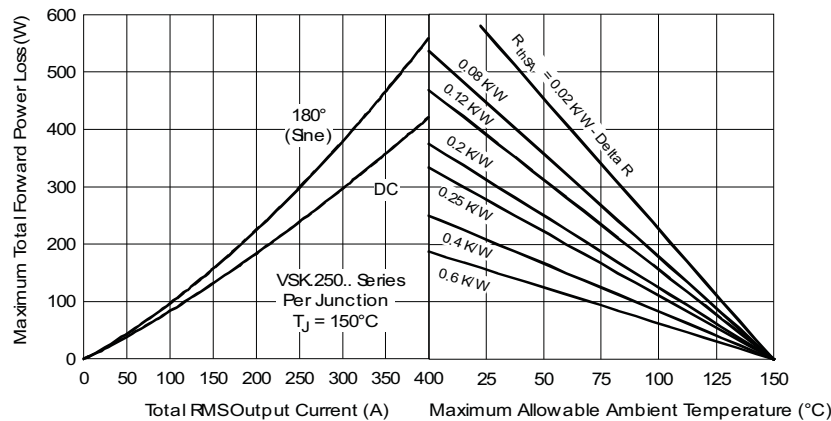


Fig. 5 - Forward Power Loss Characteristics

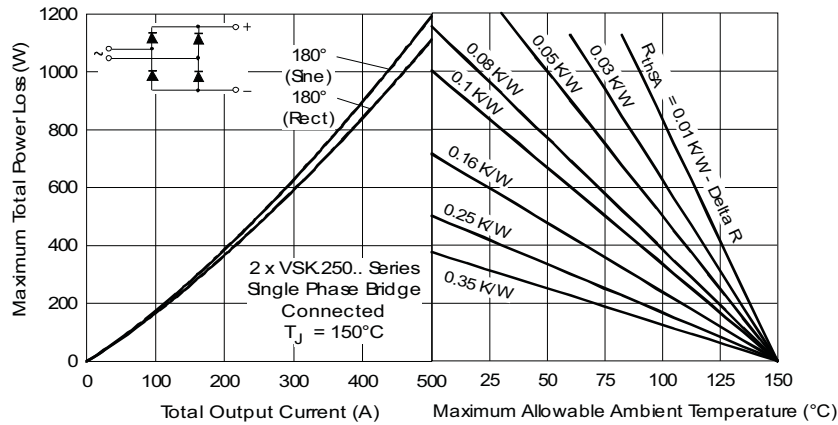


Fig. 6 - Forward Power Loss Characteristics

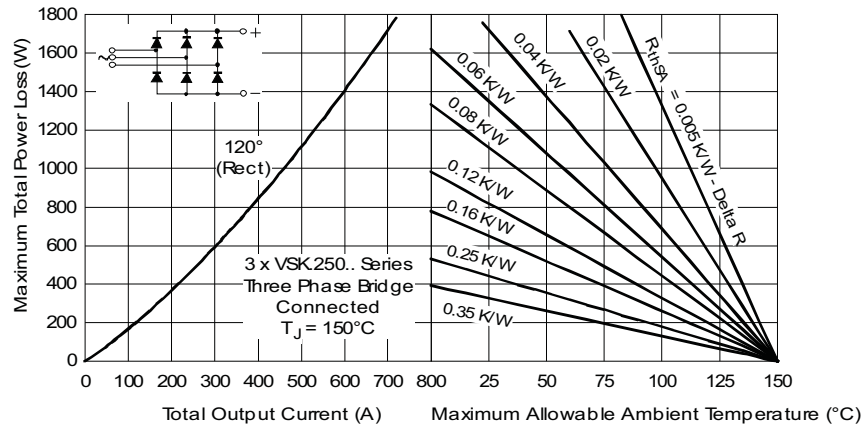


Fig. 7 - Forward Power Loss Characteristics

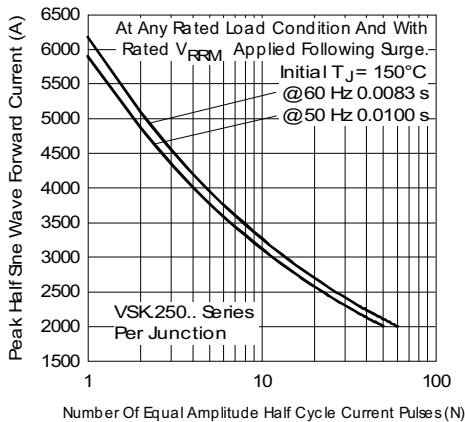


Fig. 8 - Maximum Non-Repetitive Surge Current

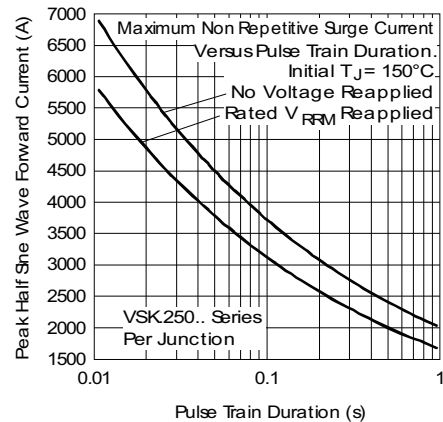


Fig. 9 - Maximum Non-Repetitive Surge Current

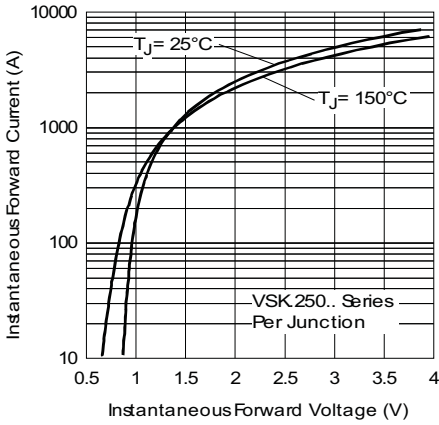


Fig. 10 - Forward Voltage Drop Characteristics

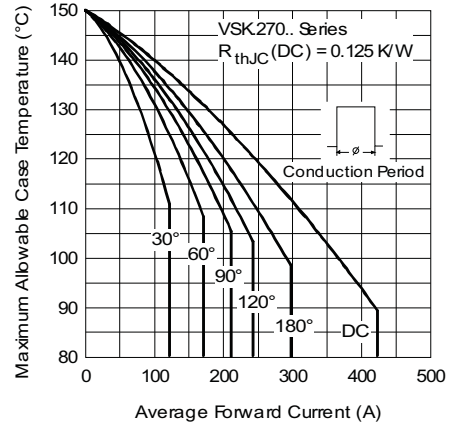


Fig. 13 - Current Ratings Characteristics

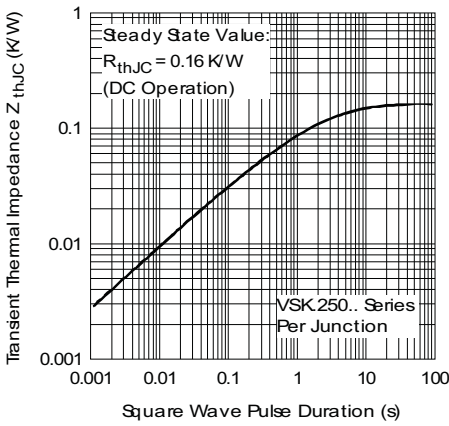


Fig. 11 - Thermal Impedance  $Z_{thJC}$  Characteristics

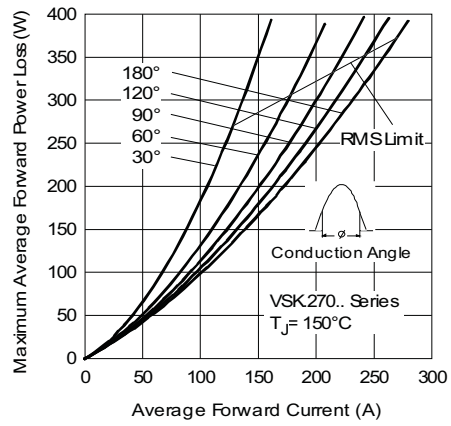


Fig. 14 - Forward Power Loss Characteristics

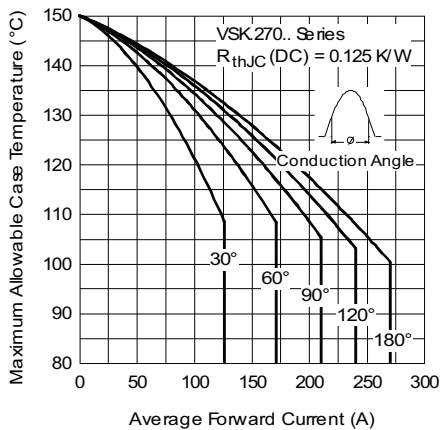


Fig. 12 - Current Ratings Characteristics

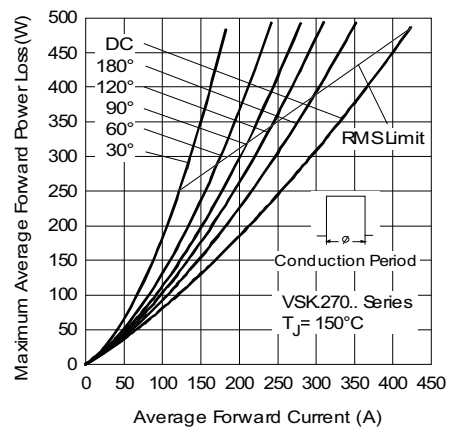


Fig. 15 - Forward Power Loss Characteristics

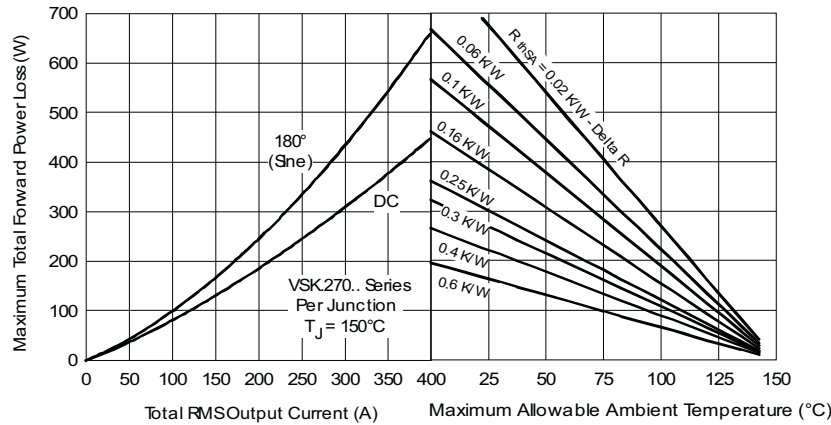


Fig. 16 - Forward Power Loss Characteristics

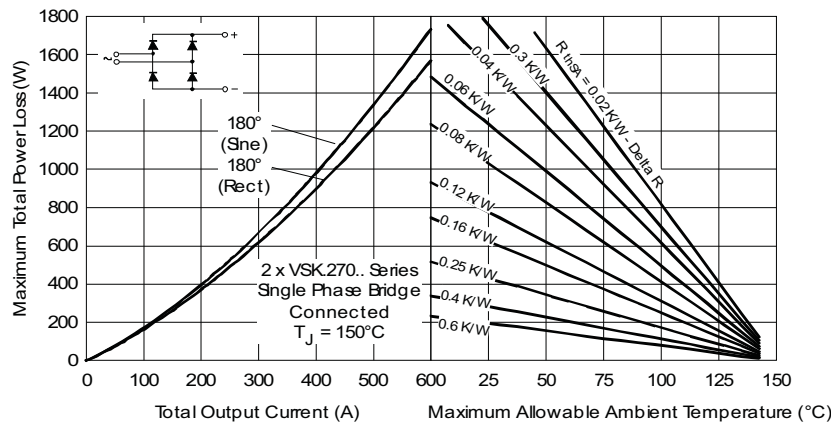


Fig. 17 - Forward Power Loss Characteristics

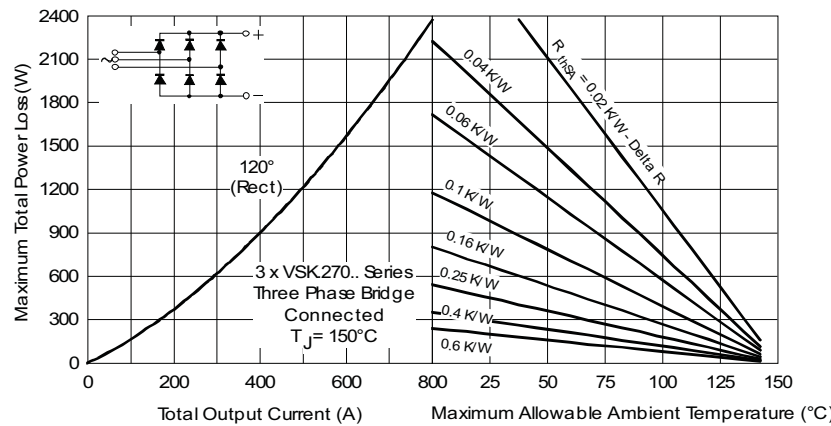


Fig. 18 - Forward Power Loss Characteristics

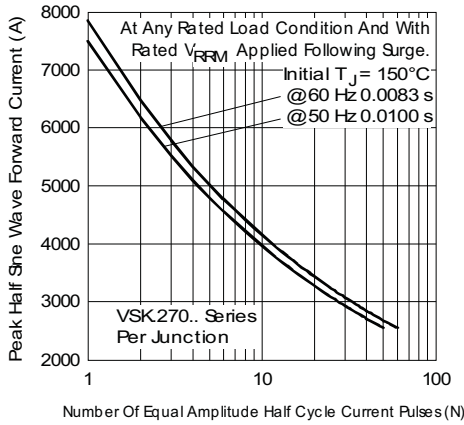


Fig. 19 - Maximum Non-Repetitive Surge Current

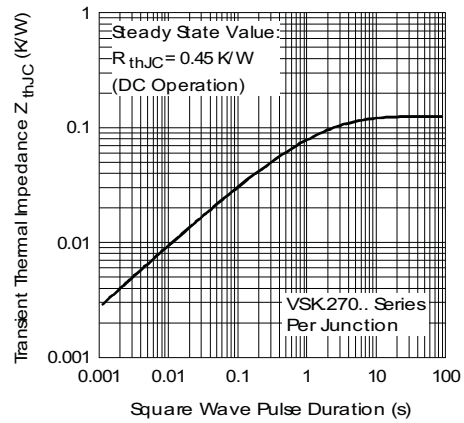


Fig. 22 - Thermal Impedance  $Z_{thJC}$  Characteristics

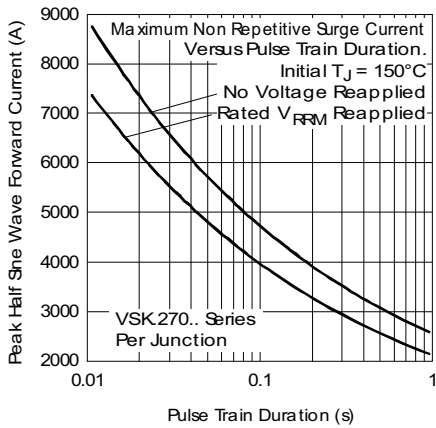


Fig. 20 - Maximum Non-Repetitive Surge Current

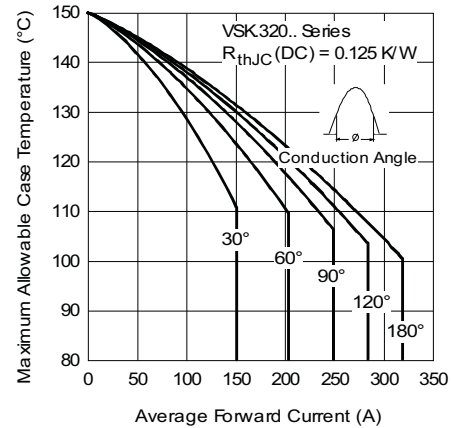


Fig. 23 - Current Ratings Characteristics

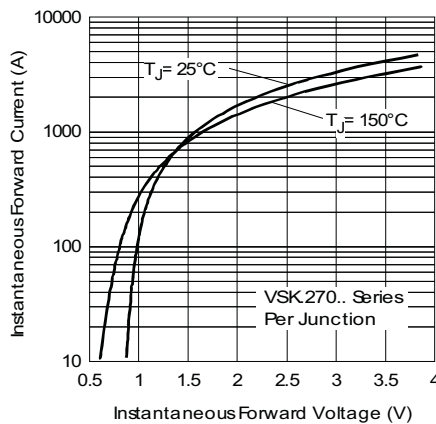


Fig. 21 - Forward Voltage Drop Characteristics

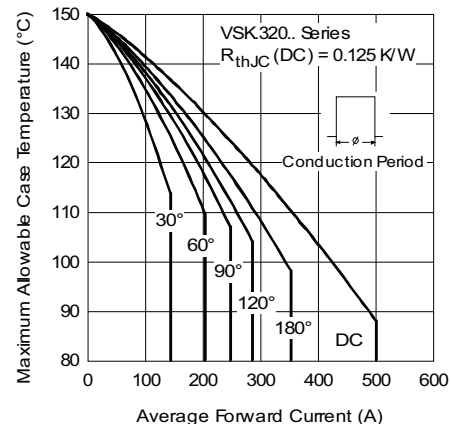


Fig. 24 - Current Ratings Characteristics



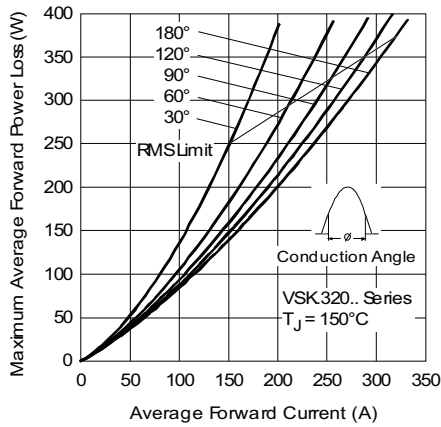


Fig. 25 - Forward Power Loss Characteristics

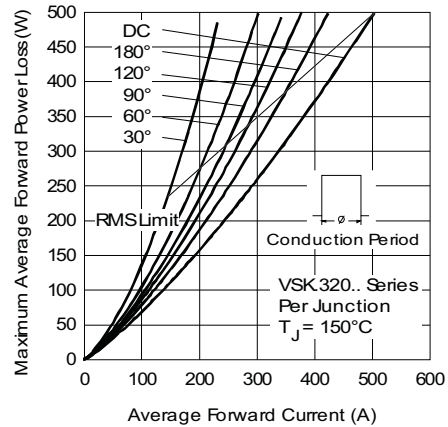


Fig. 26 - Forward Power Loss Characteristics

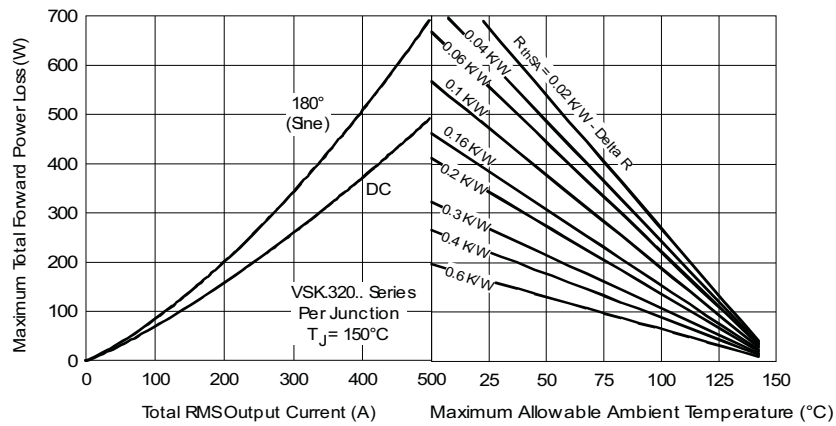


Fig. 27 - Forward Power Loss Characteristics

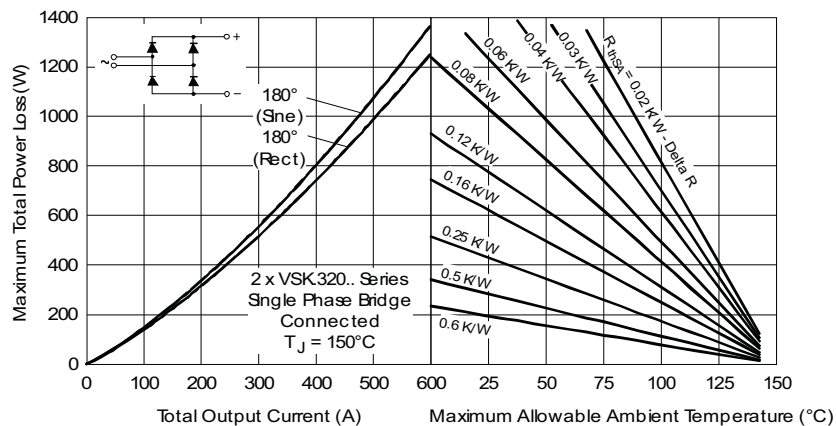


Fig. 28 - Forward Power Loss Characteristics

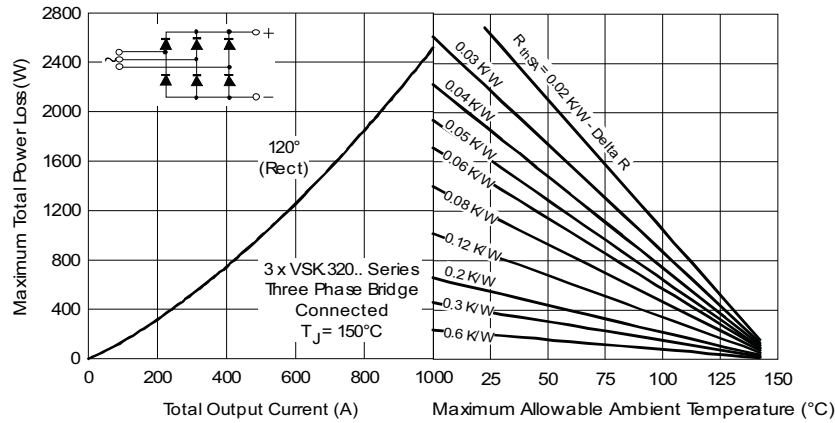


Fig. 29 - Forward Power Loss Characteristics

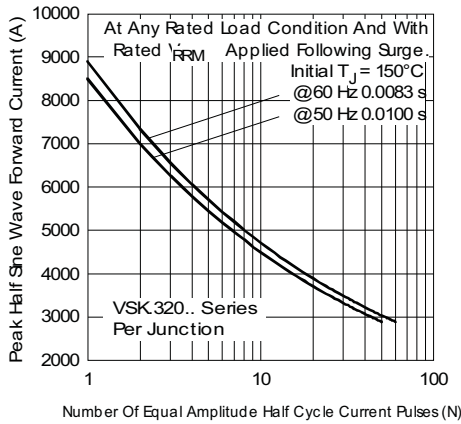


Fig. 30 - Maximum Non-Repetitive Surge Current

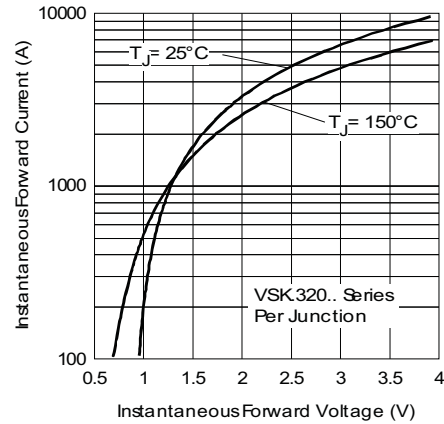


Fig. 32 - Forward Voltage Drop Characteristics

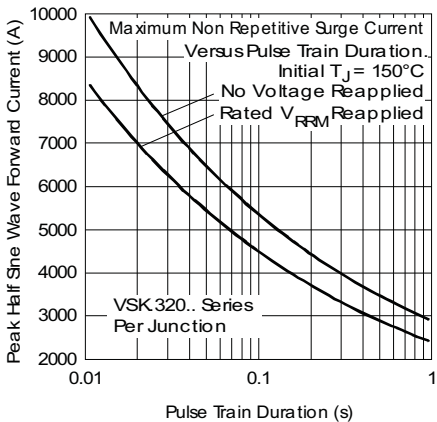


Fig. 31 - Maximum Non-Repetitive Surge Current

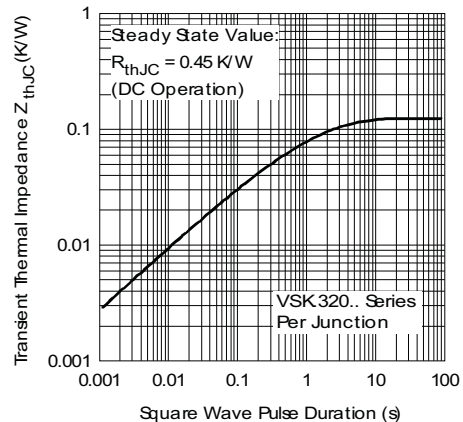


Fig. 33 - Thermal Impedance  $Z_{thJC}$  Characteristics



**ORDERING INFORMATION TABLE**

Device code	<b>VS-VS</b>	<b>KD</b>	<b>320</b>	<b>-</b>	<b>24</b>	<b>PbF</b>
	①	②	③		④	⑤

- 1** - Vishay Semiconductors product
- 2** - Circuit configuration (see Circuit Configuration table)
- 3** - Current rating:  $I_{F(AV)}$  rounded
- 4** - Voltage code x 100 =  $V_{RRM}$  (see Voltage Ratings table)
- 5** - Lead (Pb)-free

<b>CIRCUIT CONFIGURATION</b>		
<b>CIRCUIT DESCRIPTION</b>	<b>CIRCUIT CONFIGURATION CODE</b>	<b>CIRCUIT DRAWING</b>
Two diodes doubler circuit	KD	<p style="text-align: center;"><b>VSKD...</b></p>
Two diodes common cathode	KC	<p style="text-align: center;"><b>VSKC...</b></p>
Single diode	KE	<p style="text-align: center;"><b>VSKE...</b></p>

<b>LINKS TO RELATED DOCUMENTS</b>	
Dimensions	<a href="http://www.vishay.com/doc?95086">www.vishay.com/doc?95086</a>

## MAGN-A-PAK

**DIMENSIONS** in millimeters (inches)



### Notes

- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94 V-0



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