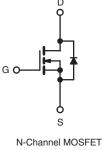


Power MOSFET

PRODUCT SUMMARY			
V _{DS} (V) at T _J max.	560 V		
R _{DS(on)} (Ω)	$V_{GS} = 10 V$	0.38	
Q _g (Max.) (nC)	68		
Q _{gs} (nC)	17.6		
Q _{gd} (nC)	21.8		
Configuration	Single	9	

TO-247AC





FEATURES

- Low Figure-of-Merit Ron x Qg
- 100 % Avalanche Tested
- Gate Charge Improved
- T_{rr}/Q_{rr} Improved
- Compliant to RoHS Directive 2002/95/EC



ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	SiHG16N50C-E3

ABSOLUTE MAXIMUM RATINGS T_{C} =	= 25 °C, unle	ess otherwis	se noted		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	v
Gate-Source Voltage			V _{GS}	± 30	v
Continuous Drain Current (T, = 150 °C) ^a		T _C = 25 °C	1-	16	А
Continuous Drain Current $(T_j = 150^{\circ} C)^{\circ}$		$T_C = 100 \ ^\circ C$	ID	10	
Pulsed Drain Current ^c			I _{DM}	40	
Linear Derating Factor				2	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	320	mJ
Maximum Power Dissipation			PD	250	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	ာိ
Soldering Recommendations (Peak Temperature) ^d	for 1	10 s		300	U

Notes

a. Limited by maximum junction temperature.

b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 2.5 mH, $R_g = 25 \Omega$, $I_{AS} = 16$ A.

c. Repetitive rating; pulse width limited by maximum junction temperature.

d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

SiHG16N50C

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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.5	C/ W

PARAMETER	SYMBOL	TEST	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		•					
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	to 25 °C, I _D = 1 mA	-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	$V_{DS} = V$	_{GS} , I _D = 250 μΑ	3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _G	_S = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	1	$V_{DS} = 5$	00 V, V _{GS} = 0 V	-	-	50	
Zero Gate voltage Drain Current	IDSS	V _{DS} = 400 V, V	/ _{GS} = 0 V, T _J = 125 °C	-	-	250	μA
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 10 V$	I _D = 8 A	-	0.317	0.38	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} =	50 V, I _D = 3 A	-	3	-	S
Dynamic							
Input Capacitance	C _{iss}	V	_{GS} = 0 V,	-	1900	-	
Output Capacitance	C _{oss}	V	_{DS} = 25 V,	-	230	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz		-	24	-	
Total Gate Charge	Qg			-	45	68	
Gate-Source Charge	Q _{qs}	$V_{GS} = 10 V$	$I_D = 16 \text{ A}, V_{DS} = 400 \text{ V}$	-	18	-	nC
Gate-Drain Charge	Q _{gd}			-	22	-	
Turn-On Delay Time	t _{d(on)}			-	27	-	
Rise Time	t _r	V _{DD} = 2	50 V, I _D = 16 A,	-	156	-	
Turn-Off Delay Time	t _{d(off)}	$R_{g} = 9.7$	$1 \Omega, V_{GS} = 10 V$	-	29	-	ns
Fall Time	t _f			-	31	-	
Gate Input Resistance	Rg	f = 1 M	Hz, open drain	-	1.6	-	Ω
Drain-Source Body Diode Characteristic	S						
Continuous Source-Drain Diode Current	I _S	MOSFET symbo showing the		-	-	16	А
Pulsed Diode Forward Current	I _{SM}	integral reverse p - n junction dic	ode	-	-	30	A
Body Diode Voltage	V_{SD}	T _J = 25 °C,	I _S = 10 A, V _{GS} = 0 V	-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	_		-	555	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		= I _S , dI/dt = 100 A/µs, / _B = 20 V	-	5.5	-	μC
Body Diode Reverse Recovery Current	I _{RRM}	- v	K – 70 A	-	18	-	Α

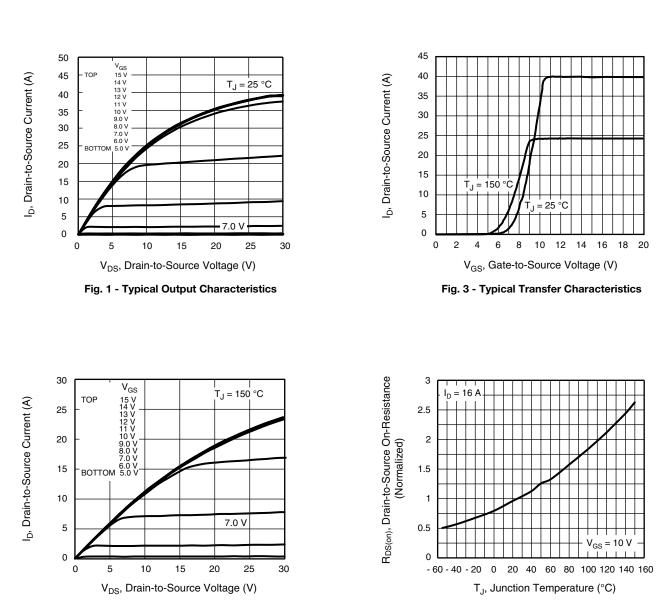
Note

• The information shown here is a preliminary product proposal, not a commercial product data sheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.



SiHG16N50C

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 2 - Typical Output Characteristics



SiHG16N50C

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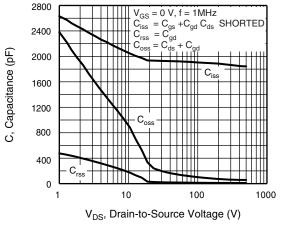


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

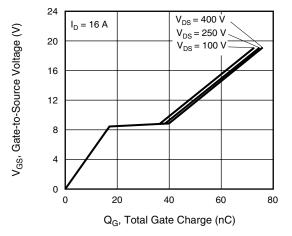


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

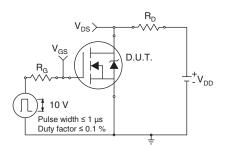


Fig. 9a - Switching Time Test Circuit

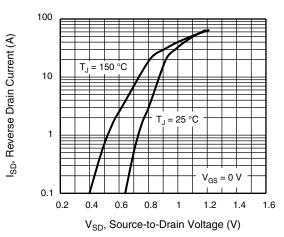


Fig. 7 - Typical Source-Drain Diode Forward Voltage

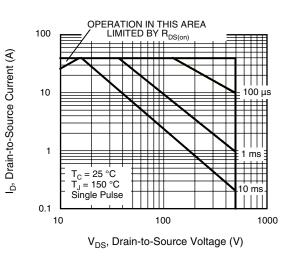


Fig. 8 - Maximum Safe Operating Area

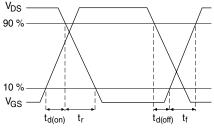
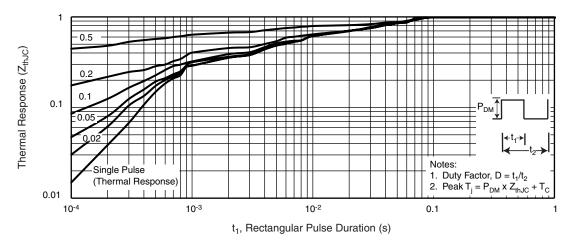


Fig. 9b - Switching Time Waveforms







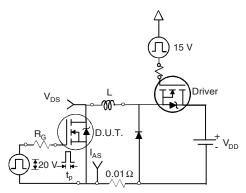


Fig. 11a - Unclamped Inductive Test Circuit

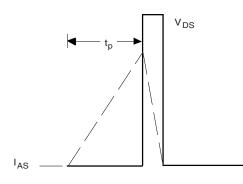


Fig. 11b - Unclamped Inductive Waveforms

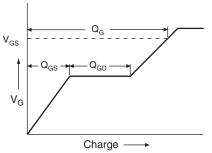
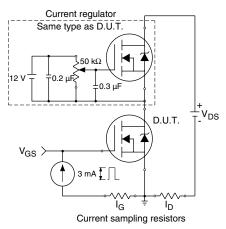


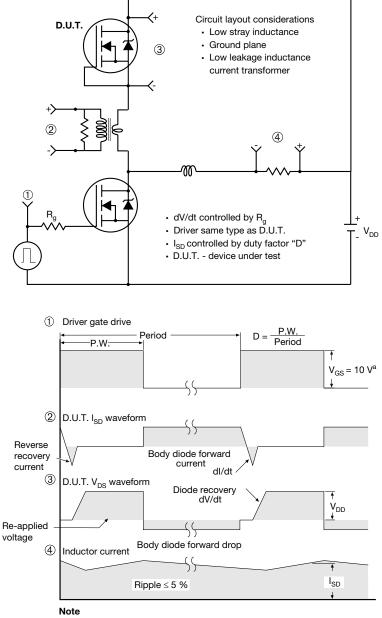
Fig. 12a - Basic Gate Charge Waveform







Peak Diode Recovery dV/dt Test Circuit



a. $V_{GS} = 5 V$ for logic level devices

Fig. 13 - For N-Channel

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TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9





Section C--C, D--D, E--E

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
А	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØP	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

Notes

- ⁽¹⁾ Package reference: JEDEC[®] TO247, variation AC
- (2) All dimensions are in mm
- ⁽³⁾ Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁵⁾ Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



VERSION 2: FACILITY CODE = Y



	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
с	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

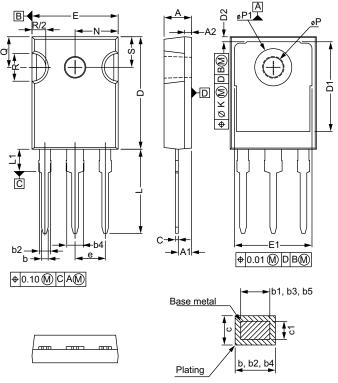
	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØΡ	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51	BSC	

Notes

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- ⁽³⁾ Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- ⁽⁵⁾ Lead finish uncontrolled in L1
- ⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- ⁽⁷⁾ Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



	MILLIN	IETERS		MILLIN	IETERS
DIM.	MIN.	MAX.	DIM.	MIN.	MAX.
А	4.65	5.31	D2	0.51	1.35
A1	2.21	2.59	E	15.29	15.87
A2	1.17	1.37	E1	13.46	-
b	0.99	1.40	е	5.46	BSC
b1	0.99	1.35	k	0.:	254
b2	1.65	2.39	L	14.20	16.10
b3	1.65	2.34	L1	3.71	4.29
b4	2.59	3.43	N	7.62	BSC
b5	2.59	3.38	Р	3.56	3.66
С	0.38	0.89	P1	-	7.39
c1	0.38	0.84	Q	5.31	5.69
D	19.71	20.70	R	4.52	5.49
D1	13.08	-	S	5.51	BSC

Notes

⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994

(2) Contour of slot optional

(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1

⁽⁵⁾ Lead finish uncontrolled in L1

⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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