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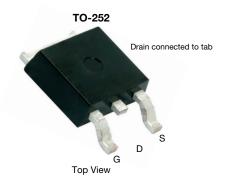
Automotive N-Channel 50 V (D-S) 175 °C MOSFET

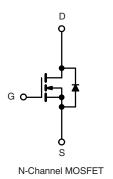
PRODUCT SUMMARY					
V _{DS} (V)	50				
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.011				
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.015				
I _D (A)	50				
Configuration	Single				
Package	TO-252				

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_q and UIS tested
- AEC-Q101 qualified d
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912







ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V _{DS}	50	V		
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current	T _C = 25 °C ^a	1	50		
	T _C = 125 °C	l _D	32		
Continuous Source Current (Diode Conduc	I _S	50	Α		
Pulsed Drain Current ^b	I _{DM}	200			
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	22.5		
Single Pulse Avalanche Energy	L = U.1 IIII	E _{AS}	25.3	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	D	75	W	
	T _C = 125 °C	P_D	25	VV	
Operating Junction and Storage Temperature Range		T _J , T _{sta}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount c	R_{thJA}	60	°C/W	
Junction-to-Case (Drain)		R _{thJC}	2	C/VV	

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static	•						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		50	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2.0	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 50 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 50 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 50 V, T _J = 175 °C	-	-	250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	50	-	-	Α
		V _{GS} = 10 V	I _D = 45 A	-	0.009	0.011	
Drain-Source On-State Resistance a	Б	V _{GS} = 10 V	I _D = 45 A, T _J = 125 °C	-	-	0.020	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 45 A, T _J = 175 °C	-	-	0.024	Ω
		V _{GS} = 4.5 V	I _D = 20 A	-	-	0.015	1
Forward Transconductance b	9fs	V _{DS} = 15 V, I _D = 30 A		-	58	-	S
Dynamic ^b							
Input Capacitance	C _{iss}			-	1685	2106	
Output Capacitance	Coss	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	345	430	pF
Reverse Transfer Capacitance	C _{rss}			-	144	180	
Total Gate Charge c	Q_g			-	34.6	52	
Gate-Source Charge c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 25 \text{ V}, I_D = 43 \text{ A}$	-	5.5	9	nC
Gate-Drain Charge ^c	Q_{gd}			-	9.1	14	
Gate Resistance	R_g		f = 1 MHz		1.8	3.9	Ω
Turn-On Delay Time ^c	t _{d(on)}				8.5	13	
Rise Time ^c	t _r	$V_{DD} = 25 \text{ V}, \text{ R}_L = 0.6 \Omega$ $I_D \cong 43 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		-	11.5	18	ns
Turn-Off Delay Time ^c	t _{d(off)}			-	22.5	34	
Fall Time ^c	t _f			1	7.5	12	
Source-Drain Diode Ratings and Chara	acteristics ^b						
Pulsed Current ^a	I _{SM}			-	-	200	Α
Forward Voltage	V_{SD}	I _F = 45 A, V _{GS} = 0 V			0.95	1.5	V

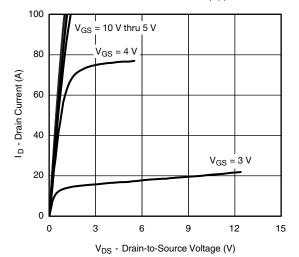
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

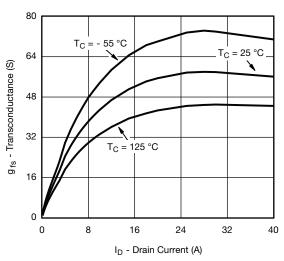
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



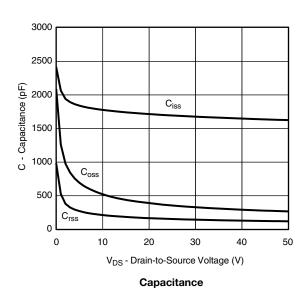
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

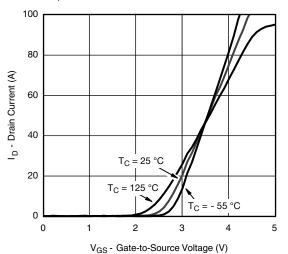


Output Characteristics

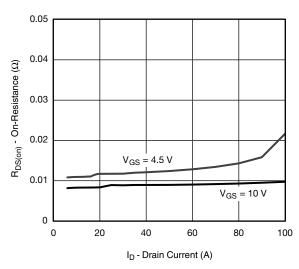


Transconductance

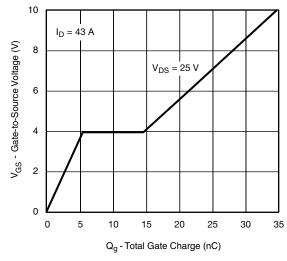




Transfer Characteristics



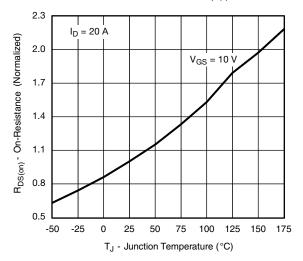
On-Resistance vs. Drain Current

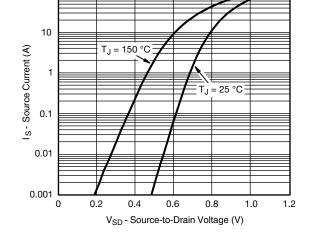


Gate Charge

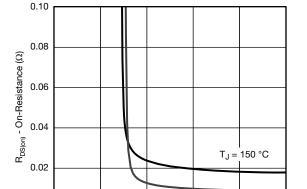


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)





On-Resistance vs. Junction Temperature

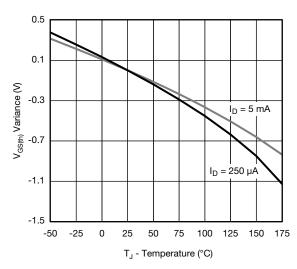


V_{GS} - Gate-to-Source Voltage (V)

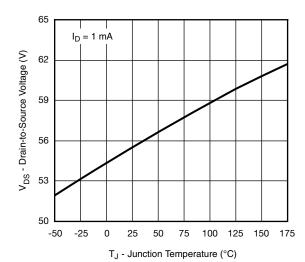
On-Resistance vs. Gate-to-Source Voltage

 $T_J = 25$ °C

Source Drain Diode Forward Voltage



Threshold Voltage



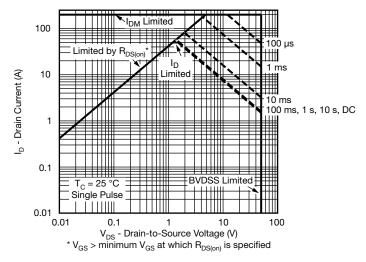
10

Drain Source Breakdown vs. Junction Temperature

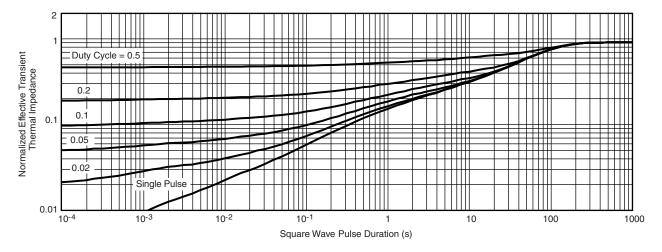
0 L



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



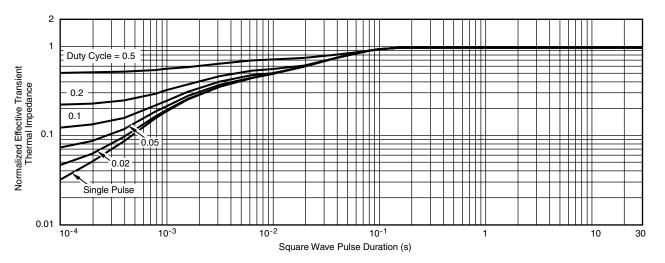
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72168.



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REVISION HISTORY a				
REVISION	DATE	DESCRIPTION OF CHANGE		
D	04-Aug-15	Revised R _g minimum limit		

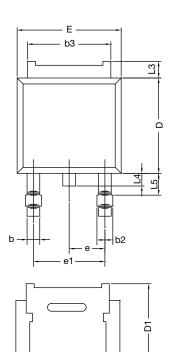
Note

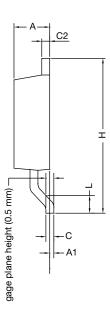
a. As of April 2014



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TO-252AA Case Outline





	MILLIN	METERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090	BSC	
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0592-Rev. A, 02-Sep-13					

DWG: 6019

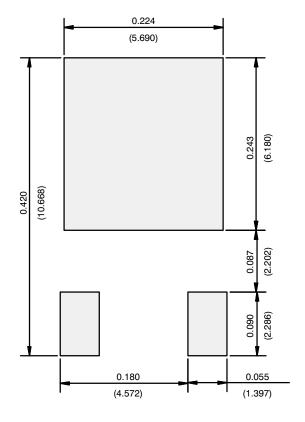
Note

• Dimension L3 is for reference only.

Revision: 02-Sep-13 Document Number: 64424



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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