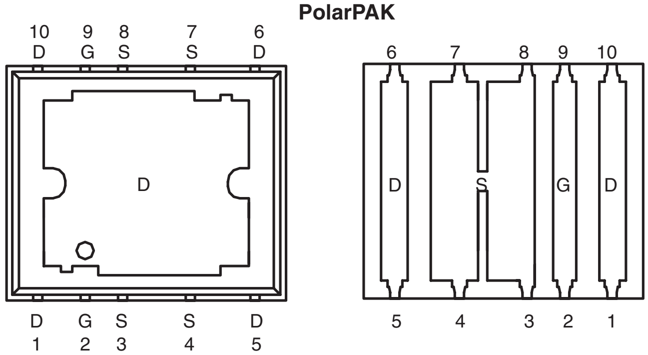
N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a] Silicon Limit	I_D (A)[a] Package Limit	Q_g (Typ.)
40	0.0055 at V_{GS} = 10 V	103	50	25 nC
	0.007 at V_{GS} = 4.5 V	91	50	

Package Drawing
www.vishay.com/doc?73398

PolarPAK



Top View   Bottom View

Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE832DF-T1-E3 (Lead (Pb)-free)
SiE832DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

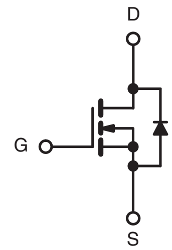
FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
  - Die Not Exposed
  - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- VRM
- Point-of-Load
- Synchronous Rectification



N-Channel MOSFET

For Related Documents
www.vishay.com/ppg?74414

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	103 (Silicon Limit)	A
			50[a] (Package Limit)	
	T_C = 70 °C		50[a]	
	T_A = 25 °C		23.6[b, c]	
	T_A = 70 °C		18.9[b, c]	
Pulsed Drain Current		I_{DM}	80	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	50[a]	
	T_A = 25 °C		4.3[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	35	
Avalanche Energy		E_{AS}	61	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	104	W
	T_C = 70 °C		66	
	T_A = 25 °C		5.2[b, c]	
	T_A = 70 °C		3.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

Notes:
a. Package limited is 50 A.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See Solder Profile (*www.vishay.com/doc?73257*). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]	$t \le 10$ s	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)[a]	Steady State	R_{thJC} (Drain)	1	1.2	
Maximum Junction-to-Case (Source)[a, c]		R_{thJC} (Source)	2.8	3.4	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Maximum under Steady State conditions is 68 °C/W.
c. Measured at source pin (on the side of the package).

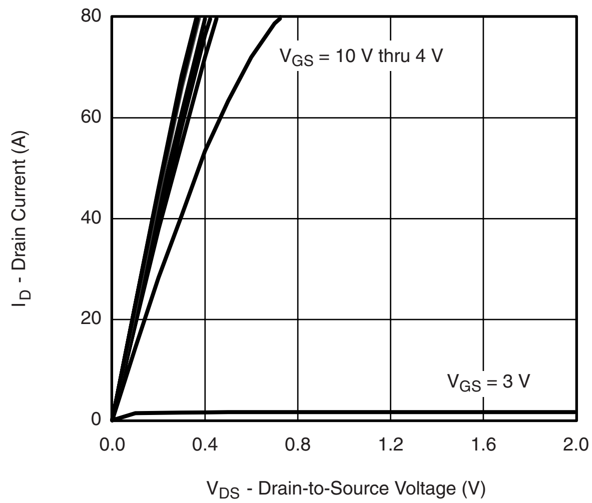
SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		43.1		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250 µA	1.5	2.2	3.0	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \ge$ 5 V, V_{GS} = 10 V	25			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 14 A		0.0046	0.0055	Ω
		V_{GS} = 4.5 V, I_D = 12 A		0.0058	0.007	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 13.6 A		86		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		3800		pF
Output Capacitance	C_{oss}			510		
Reverse Transfer Capacitance	C_{rss}			160		
Total Gate Charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 20 A		51	77	nC
		V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 20 A		25	38	
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			7		
Gate Resistance	R_g	f = 1 MHz		1.1	1.7	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		45	70	ns
Rise Time	t_r			260	400	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			55	85	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		15	25	
Rise Time	t_r			30	45	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			50	A
Pulse Diode Forward Current[a]	I_{SM}				80	
Body Diode Voltage	V_{SD}	I_S = 10 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10 A, dI/dt = 100 A/µs, T_J = 25 °C		85	130	ns
Body Diode Reverse Recovery Charge	Q_{rr}			110	170	nC
Reverse Recovery Fall Time	t_a			64		ns
Reverse Recovery Rise Time	t_b			21		

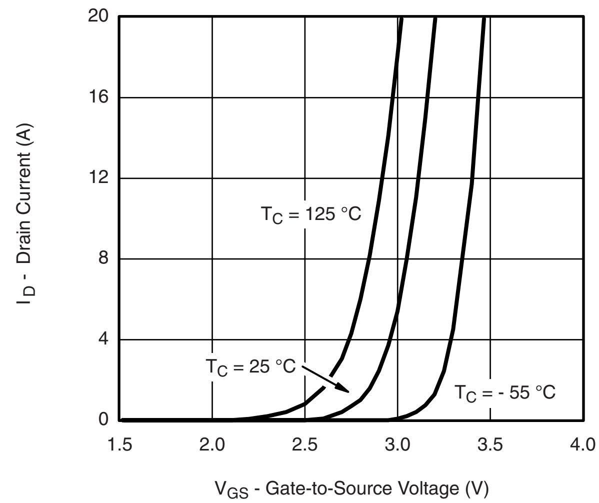
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

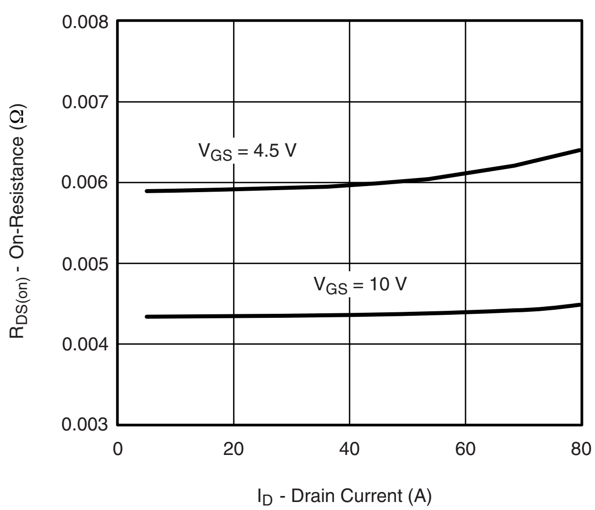
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



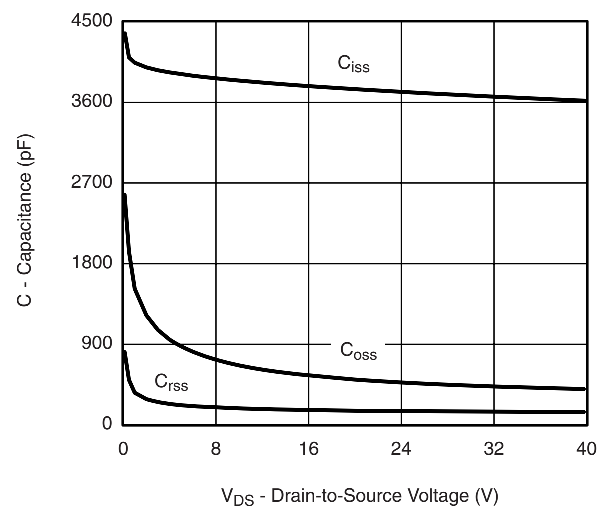
Output Characteristics



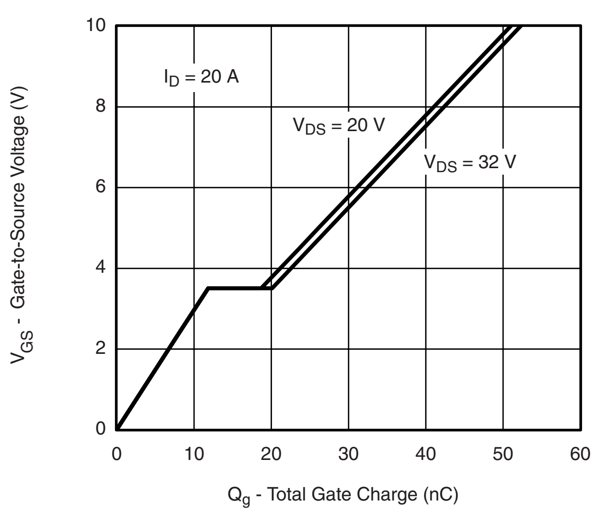
Transfer Characteristics



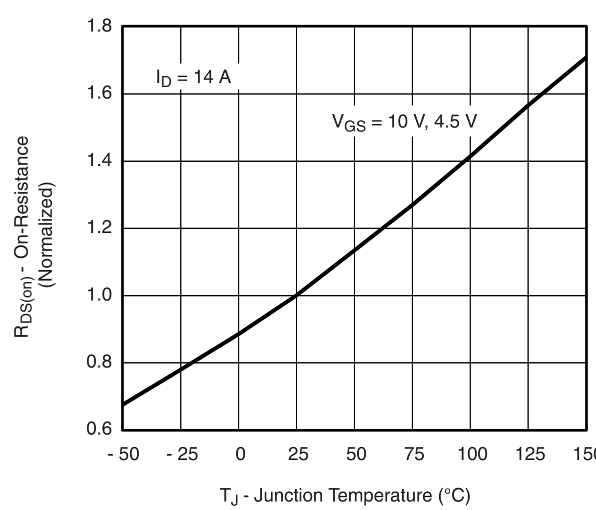
On-Resistance vs. Drain Current



Capacitance

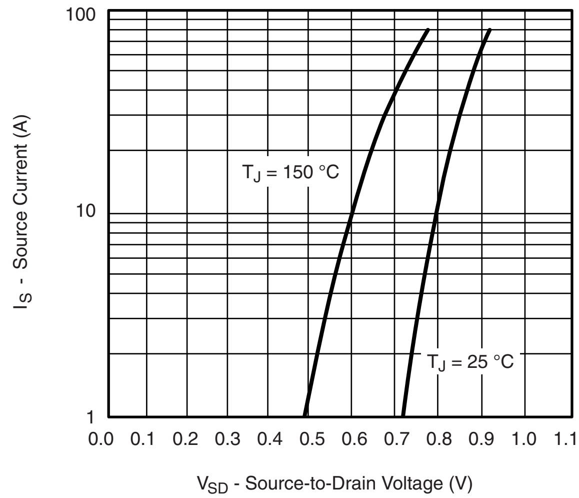


Gate Charge

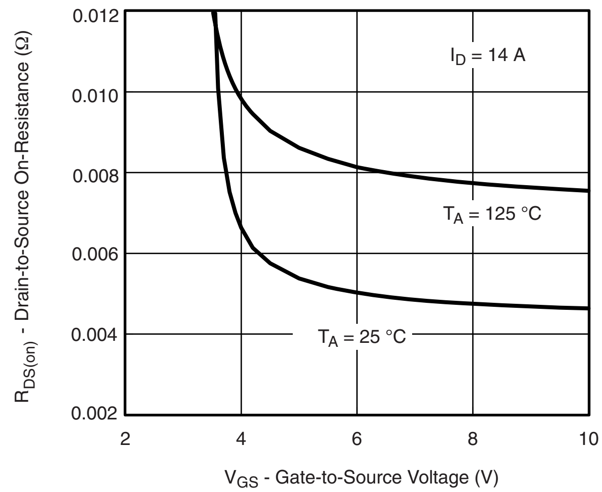


On-Resistance vs. Junction Temperature

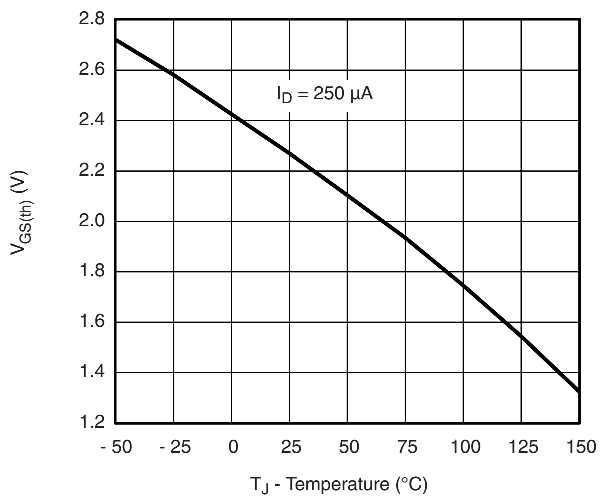
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



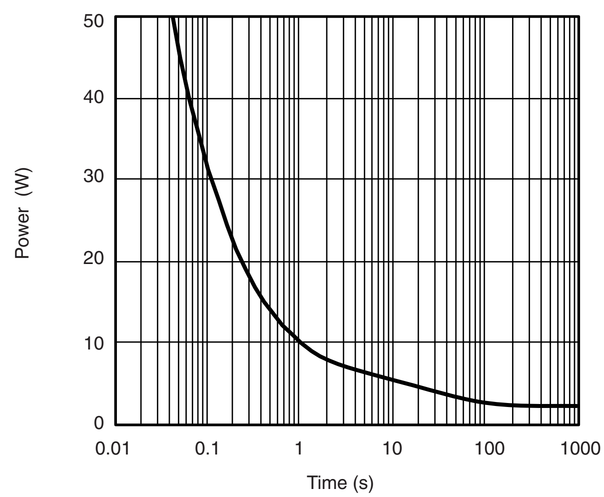
Source-Drain Diode Forward Voltage



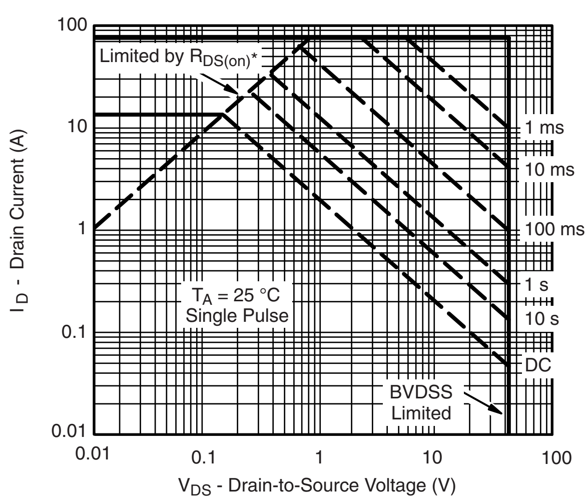
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

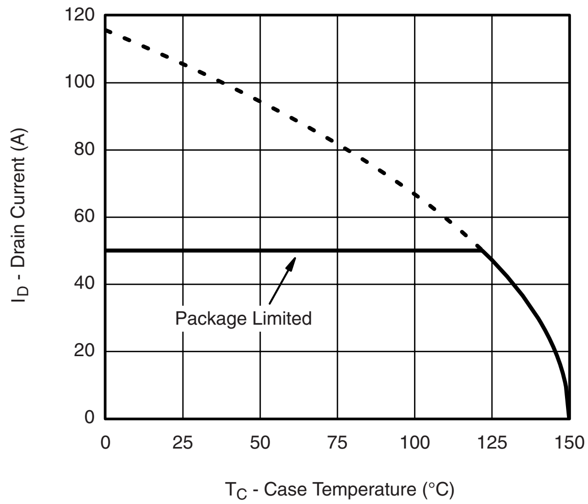


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

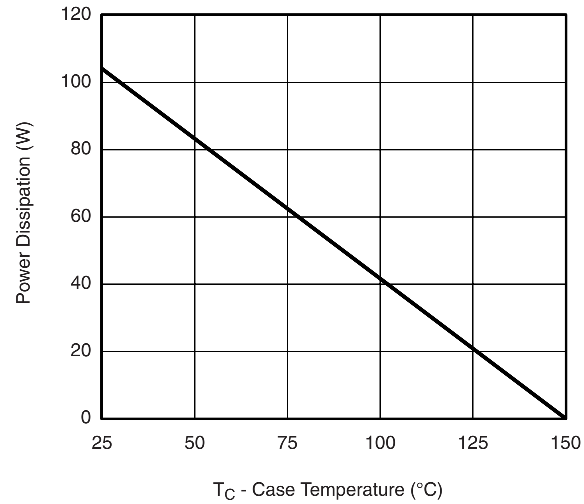
Safe Operating Area, Junction-to-Ambient

Document Number: 74414
S09-1338-Rev. C, 13-Jul-09

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



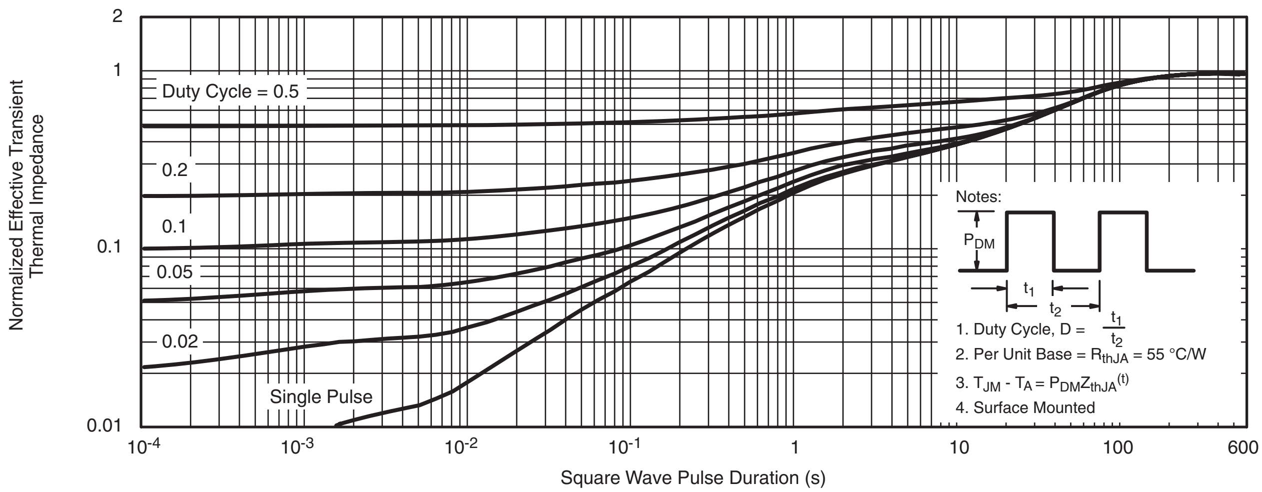
Current Derating*



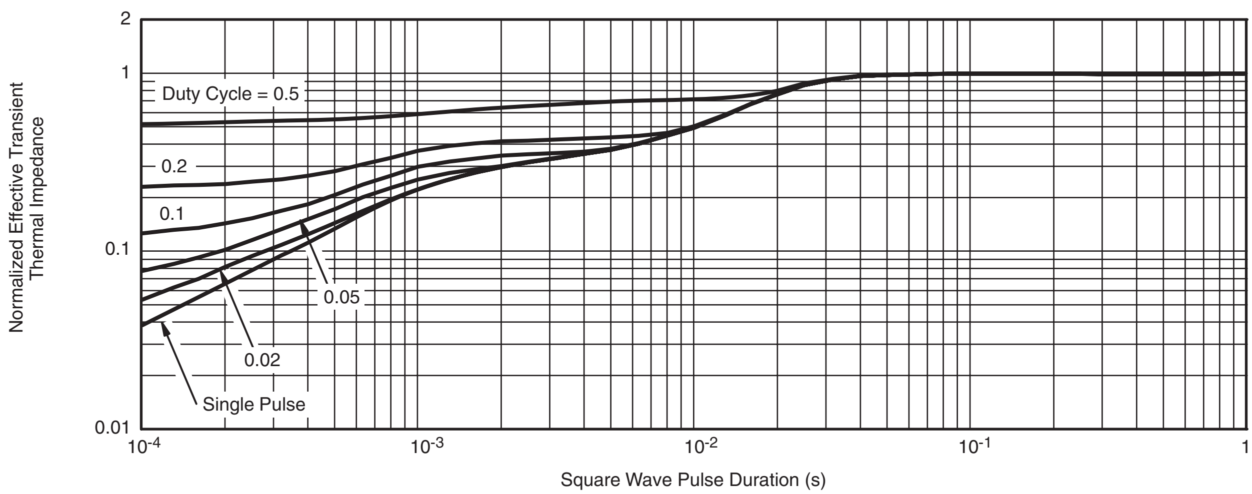
Power Derating, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

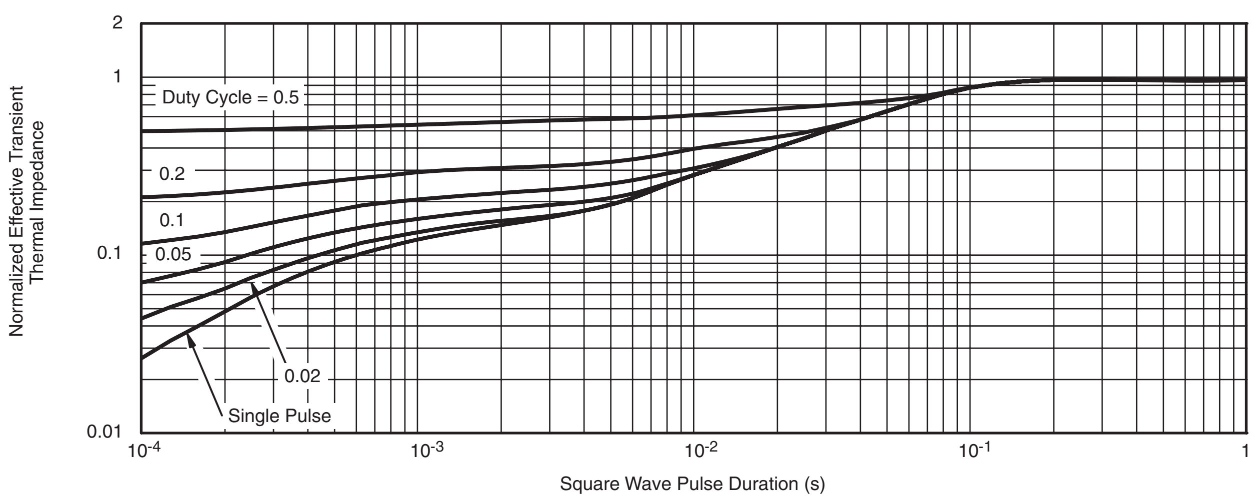
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)

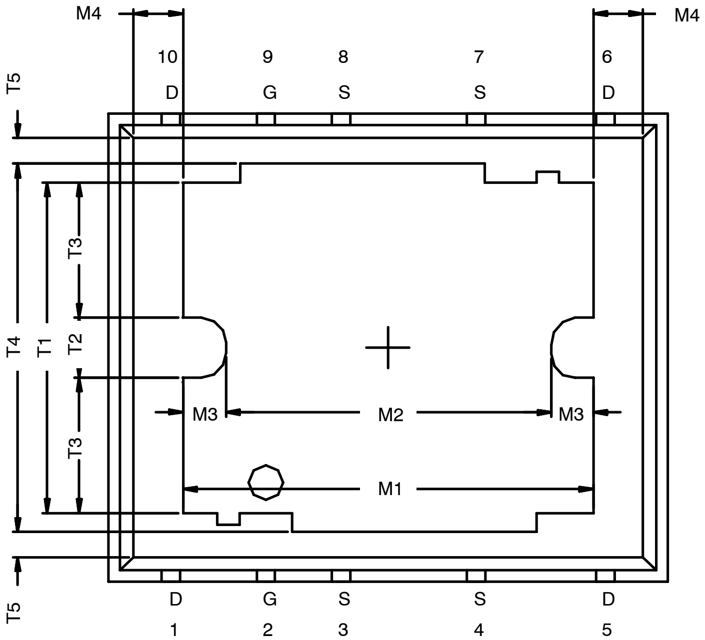


Normalized Thermal Transient Impedance, Junction-to-Source

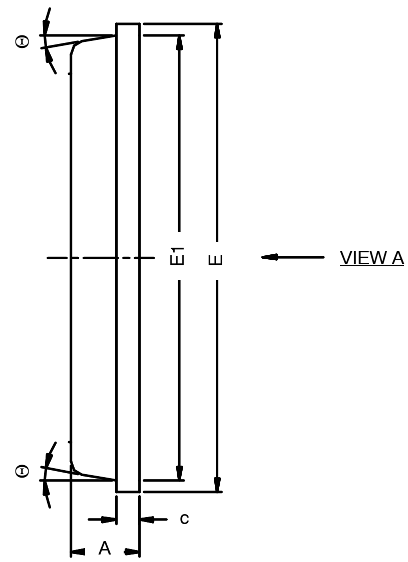
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74414.

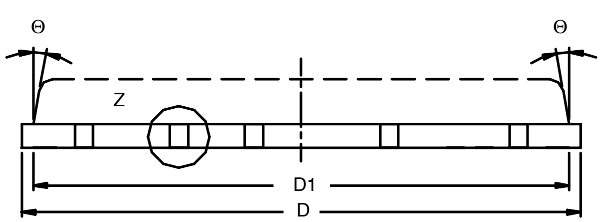
PolarPAK™ (Option S)

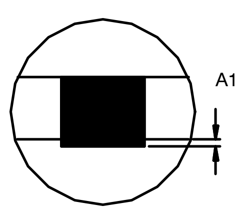
Product datasheet/information page contain links to applicable package drawing.



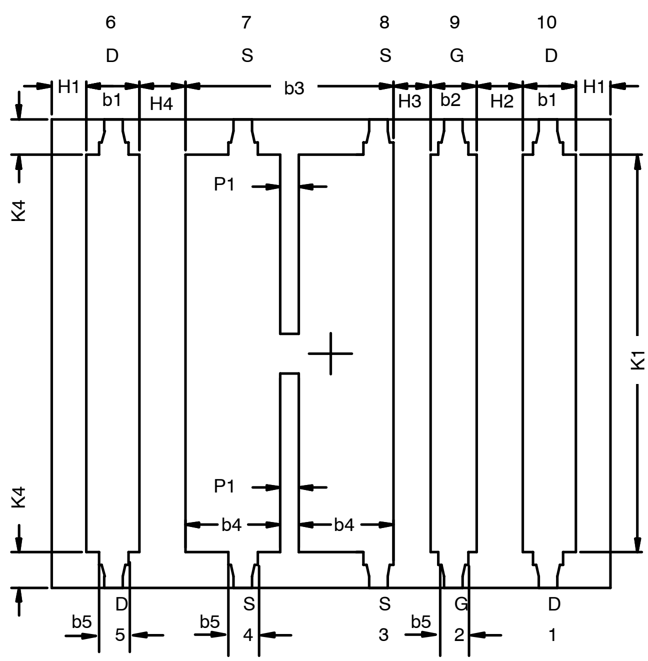
(Top View)







DETAIL Z

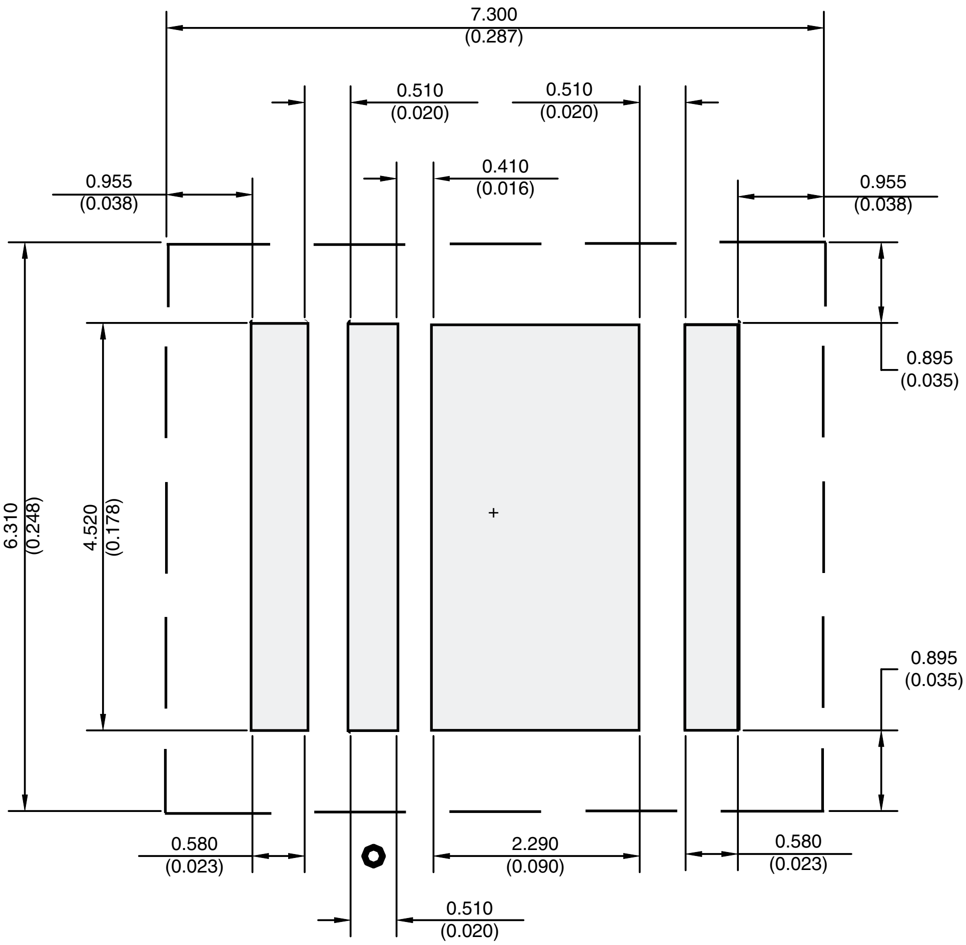


VIEW A
(Bottom View)

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	–	0.05	0.000	–	0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6.00	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23	–	–	0.009	–	–
H2	0.45	–	0.56	0.020	–	0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45	–	0.56	0.020	–	0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K4	0.24	–	–	0.009	–	–
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22	–	–	0.009	–	–
M4	0.05	–	–	0.002	–	–
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.150
T2	0.56	0.76	0.95	0.22	0.030	0.037
T3	1.20	–	–	0.051	–	–
T4	3.90	–	–	0.154	–	–
T5	0	0.18	0.36	0.000	0.007	0.014
Θ	0°	10°	12°	0°	10°	12°
ECN: S–51049—Rev. B, 13-Jun-05 DWG: 5947						

Note: Millimeters govern over inches

RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S
Dimensions in mm/(Inches)
No External Traces within Broken Lines
Dot indicates Gate Pin (Part Marking)

Return to Index

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