

## Half-Bridge N-Channel MOSFET Driver for DC/DC Conversion

### DESCRIPTION

The SiP41109 and SiP41110 are high-speed half-bridge MOSFET drivers for use in high frequency, high current, multiphase dc-to-dc synchronous rectifier buck power supplies. They are designed to operate at switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving N-channel MOSFETs.

They feature adaptive shoot-through protection to prevent simultaneous conduction of the external MOSFETs. There are two options available for the voltage of the high-side and low-side drivers. In the SiP41109, the regulator supplies gate drive voltage to the high-side driver and  $V_{CC}$  supplies the low-side driver. In the SiP41110, the regulator supplies the high- and low-side gate drive voltage.

The SiP41109 and SiP41110 are assembled in a lead (Pb)-free 8-pin SOIC package for operation over the industrial operating range (-40 °C to 85 °C).

### FEATURES

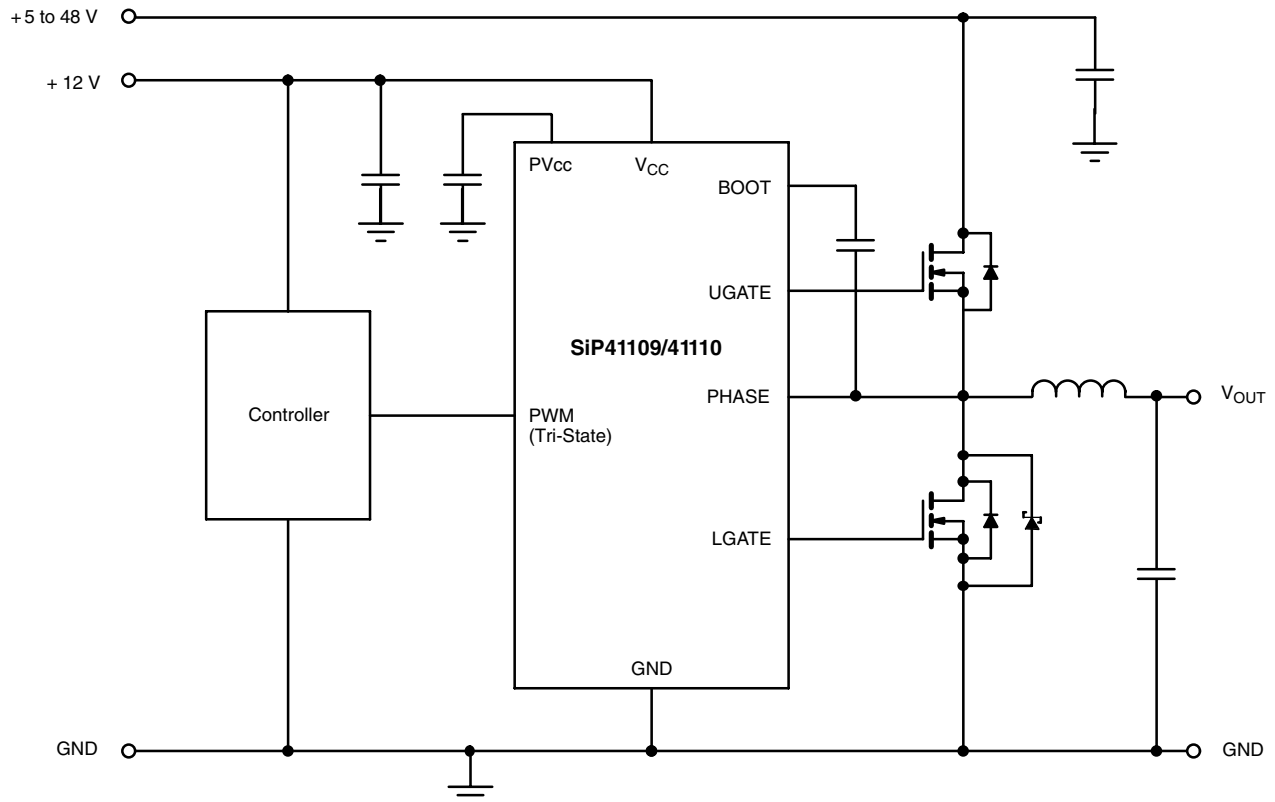
- PWM with tri-state enable
- 12 V low-side gate drive (SiP41109)
- 8 V low-side gate drive (SiP41110)
- Undervoltage lockout
- Internal bootstrap diode
- Switching frequency up to 1 MHz
- 30 ns max. propagation delay
- Drive MOSFETs in 5 V to 48 V systems
- Adaptive shoot-through protection



### APPLICATIONS

- Multi-phase DC/DC conversion
- High current low voltage DC/DC converters
- High frequency DC/DC converters
- Mobile and desktop computer DC/DC converters
- Core voltage supplies for PC micro-processors

### TYPICAL APPLICATION CIRCUIT



<b>ABSOLUTE MAXIMUM RATINGS</b> (all voltages referenced to GND = 0 V)			
Parameter		Limit	Unit
$V_{CC}, PV_{CC}$		- 0.3 to 15	V
BOOT, PHASE		- 0.3 to 55	
BOOT to PHASE		- 0.3 to 15	
Storage Temperature		- 40 to 150	°C
Operating Junction Temperature		125	
Power Dissipation <sup>a</sup>	SO-8	770	mW
Thermal Impedance ( $\Theta_{JA}$ ) <sup>b</sup>		130	°C/W

Notes:

a. Device Mounted with all leads soldered or welded to PC board.

b. Derate 7.7 mW/°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<b>RECOMMENDED OPERATING RANGE</b> (all voltages referenced to GND = 0 V)			
Parameter		Limit	Unit
$V_{CC}$		10.8 to 13.2	V
$V_{LX}$		48	
$C_{BOOT}$		100 nF to 1 $\mu$ F	
BOOT to PHASE		8	V
Operating Temperature Range		- 40 to 85	°C

<b>SPECIFICATIONS<sup>a</sup></b>						
Parameter	Symbol	Test Conditions Unless Specified $V_{CC} = 12\text{ V}, V_{BOOT} - V_{PHASE} = 8\text{ V}$ $T_A = -40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$	Limits			Unit
			Min. <sup>a</sup>	Typ. <sup>b</sup>	Max. <sup>a</sup>	
<b>Power Supplies</b>						
Supply Voltage	$V_{DD}$		10.8		13.2	V
Quiescent Current	$I_{CCQ}$	PWM non-switching		5.6	9.5	mA
Supply Current	$I_{DD}$	$f_{PWM} = 100\text{ kHz}, C_{LOAD} = 3\text{ nF}$		12.5		
				11.0		
Tristate (Shutdown) Current	$I_{CCT}$	PWM = open		850	1200	$\mu$ A
<b>Reference Voltage</b>						
Break-Before-Make	$V_{BBM}$			2.5		V
<b>PWM Input</b>						
Input High	$V_{IH}$		4.0		$V_{DD}$	V
Input Low	$V_{IL}$				1.0	
Bias Current	$I_B$	PWM 5 V or 0 V		$\pm 600$	$\pm 1000$	$\mu$ A
Tristate Threshold	High	$V_{TSH}$	3.0			V
	Low	$V_{TSL}$			2.0	
Tristate Holdoff Timeout <sup>c</sup>	$t_{TST}$			240		ns
<b>Bootstrap Diode</b>						
Forward Voltage	$V_F$	$I_F = 40\text{ mA}, T_A = 25\text{ }^\circ\text{C}$	0.70	0.85	1.0	V



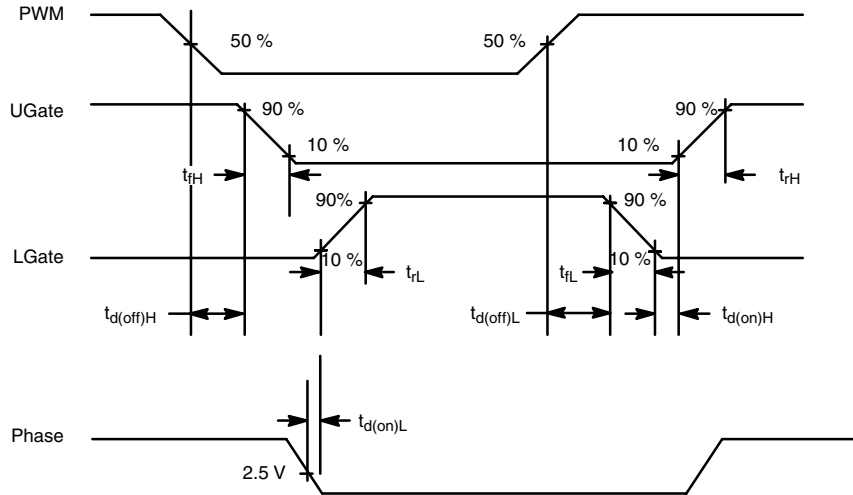
SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Specified $V_{CC} = 12\text{ V}$ , $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$		Limits			Unit
				Min. <sup>a</sup>	Typ. <sup>b</sup>	Max. <sup>a</sup>	
<b>MOSFET Drivers</b>							
High-Side Drive Current <sup>c</sup>	$I_{PKH(source)}$	$V_{BOOT} - V_{PHASE} = 8\text{ V}$			0.8		A
	$I_{PKH(sink)}$				1.0		
Low-Side Drive Current <sup>c</sup>	$I_{PKL(source)}$	$V_{PVCC} = 8\text{ V}$	SiP41110		0.9		
	$I_{PKL(sink)}$				1.2		
	$I_{PKL(source)}$	$V_{PVCC} = 12\text{ V}$	SiP41109		1.4		
	$I_{PKL(sink)}$				1.8		
High-Side Driver Impedance	$R_{DH(source)}$	$V_{BOOT} - V_{PHASE} = 8\text{ V}$ , PHASE = GND			2.3	4.2	$\Omega$
	$R_{DH(sink)}$				1.9	3.5	
Low-Side Driver Impedance	$R_{DL(source)}$	$V_{PVCC} = 8\text{ V}$	SiP41110		2.9	5.2	
	$R_{DL(sink)}$				1.3	2.4	
	$R_{DL(source)}$	$V_{PVCC} = 12\text{ V}$	SiP41109		2.4	4.3	
	$R_{DL(sink)}$				1.2	2.2	
High-Side Rise Time	$t_{rH}$	10% - 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ , $C_{LOAD} = 3\text{ nF}$			45		ns
High-Side Fall Time	$t_{fH}$				35		
High-Side Rise Time Bypass		10% - 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ , $C_{LOAD} = 3\text{ nF}$			45		
High-Side Fall Time Bypass					35		
High-Side Propagation Delay <sup>c</sup>	$t_{d(off)H}$	See Timing Waveforms			15		
	$t_{d(on)H}$				15		
Low-Side Rise Time	$t_{rL}$	10% to 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41110		40		
		10% to 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41109		40		
Low-Side Fall Time	$t_{fL}$	10% to 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41110		30		
		10% to 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41109		30		
Low-Side Propagation Delay	$t_{d(off)L}$	See Timing Waveforms			15		
	$t_{d(on)L}$				15		
<b>PHASE Timer</b>							
PHASE Falling Timeout <sup>c</sup>	$t_{PHASE}$				380		ns
<b>PV<sub>CC</sub> Regulator</b>							
Output Voltage	$V_{VCC}$			7.6	8	8.4	V
Output Current	$I_{PVCC}$				80	100	mA
Current Limit	$I_{LIM}$	$V_{DRV} = 0\text{ V}$		120	200	280	
Line Regulation	LNR	$V_{CC} = 10.8\text{ V}$ to $13.2\text{ V}$			0.05	0.5	%/V
Load Regulation	LDR	5 mA to 80 mA			0.1	1.0	%
<b>PV<sub>CC</sub> Regulator UVLO</b>							
PV <sub>CC</sub> Rising	$V_{UVLO2}$				6.7	7.2	V
PV <sub>CC</sub> Falling					6.4	6.9	
Hysteresis	Hyst			100	300	500	mV
<b>High-Side Undervoltage Lockout</b>							
Threshold	$V_{UVHS}$	Rising or falling		2.5	3.35	4.0	V
<b>V<sub>CC</sub> Undervoltage Lockout</b>							
Threshold	$V_{UVLO1}$			5.0	5.3	5.6	V
Power on Reset Time	POR				2.5		ms
<b>Thermal Shutdown</b>							
Temperature	$T_{SD}$	Temperature rising			165		$^\circ\text{C}$
Hysteresis	$T_H$	Temperature falling			25		

Notes:

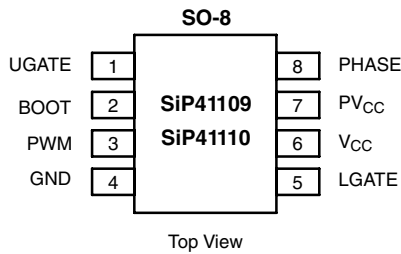
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at  $V_{CC} = 12\text{ V}$  unless otherwise noted.

## TIMING WAVEFORMS



## PIN CONFIGURATION AND TRUTH TABLE



TRUTH TABLE		
PWM	UGATE	LGATE
L	L	H
L	H	L
Tri-State	L	L

ORDERING INFORMATION		
Part Number	Temperature Range	Marking
SiP41109DY-T1-E3	- 40 °C to 85 °C	41109
SiP41110DY-T1-E3		41110
Eval Kit	Temperature Range	
SiP41109DB	- 40 °C to 85 °C	
SiP41110DB		

PIN DESCRIPTION		
Pin Number	Name	Function
1	UGATE	8 V high-side MOSFET gate drive
2	BOOT	Bootstrap supply for high-side driver. The bootstrap capacitor is connected between BOOT and PHASE.
3	PWM	Input signal for the MOSFET drivers and tri-state enable
4	GND	Ground
5	LGATE	Synchronous or low-side MOSFET gate drive
6	V <sub>CC</sub>	12 V supply. Connect a bypass capacitor ≥ 1 μF from here to ground
7	PV <sub>CC</sub>	8 V voltage regulator Output. Connect a bypass capacitor ≥ 1 μF from here to ground
8	PHASE	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor



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for the bootstrap circuit; only a capacitor is necessary to complete the bootstrap circuit. The bootstrap capacitor is sized according to

$$C_{BOOT} = (Q_{GATE} / (\Delta V_{BOOT} - V_{PHASE})) \times 10$$

where  $Q_{GATE}$  is the gate charge needed to turn on the high-side MOSFET and  $\Delta V_{BOOT} - V_{PHASE}$  is the amount of droop allowed in the bootstrapped supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$ . The bootstrap capacitor voltage rating must be greater than  $V_{CC} + 12\text{ V}$  to withstand transient spikes and ringing.

### Shoot-Through Protection

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the PHASE pin and the LGATE pin and control the switching as follows: When the signal on PWM goes low, UGATE will go low after an internal propagation delay. After the voltage on PHASE falls below 2.5 V by the inductor action, the low-side driver is enabled and LGATE goes high after some delay. When the signal on PWM goes high, LGATE will go low after an internal propagation delay. After the voltage on LGATE drops below

2.5 V the high-side driver is enabled and UGATE will go high after an internal propagation delay. If PHASE does not drop below 2.5 V within 380 ns after UGATE goes low, LGATE is forced high until the next PWM transition.

### V<sub>CC</sub> Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1  $\mu\text{F}$  ceramic capacitor as close as practical between the  $V_{CC}$  and GND pins.

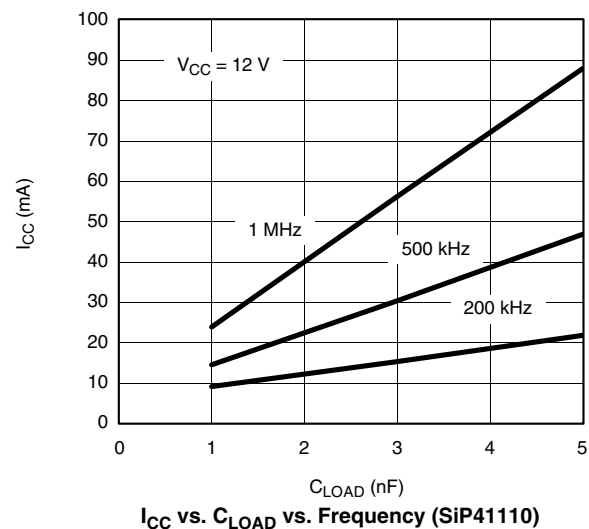
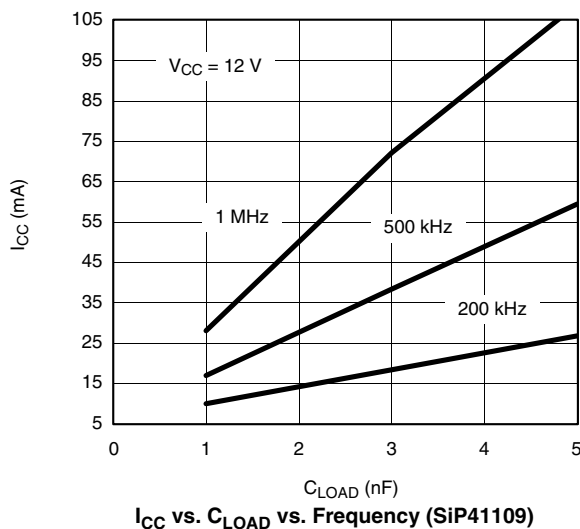
### Undervoltage Lockout

Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces LGATE and UGATE to low when  $V_{CC}$  is below its specified voltage. A separate UVLO forces UGATE low when the voltage between BOOT and PHASE is below the specified voltage.

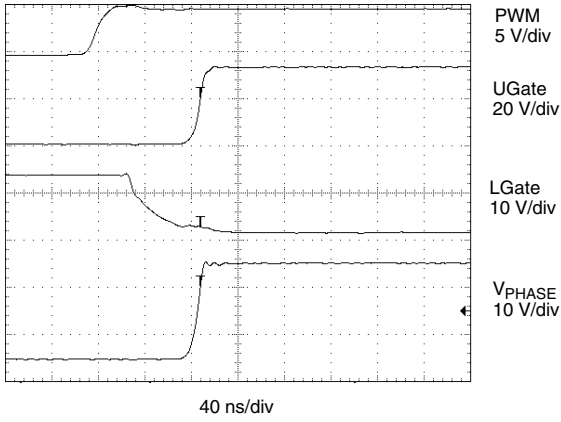
### Thermal Protection

If the die temperature rises above 165 °C, the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140 °C.

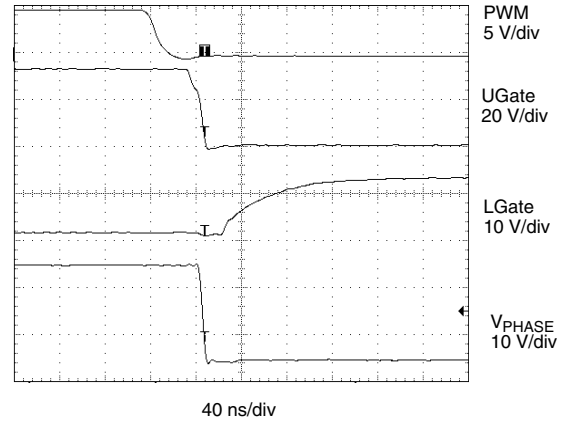
## TYPICAL CHARACTERISTICS



**TYPICAL WAVEFORMS**



**Figure 2. PWM Signal vs. HS Gate, LS Gate and PHASE (Rising)**



**Figure 3. PWM Signal vs. HS Gate, LS Gate and PHASE (Falling)**

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