

Half-Bridge N-Channel MOSFET Driver for DC/DC Conversion

DESCRIPTION

The SiP41109 and SiP41110 are high-speed half-bridge MOSFET drivers for use in high frequency, high current, multiphase dc-to-dc synchronous rectifier buck power supplies. They are designed to operate at switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving N-channel MOSFETs.

They feature adaptive shoot-through protection to prevent simultaneous conduction of the external MOSFETs. There are two options available for the voltage of the high-side and low-side drivers. In the SiP41109, the regulator supplies gate drive voltage to the high-side driver and $V_{\rm CC}$ supplies the low-side driver. in the SiP41110, the regulator supplies the high- and low-side gate drive voltage.

The SiP41109 and SiP41110 are assembled in a lead (Pb)-free 8-pin SOIC package for operation over the industrial operating range (- $40 \, ^{\circ}$ C to $85 \, ^{\circ}$ C).

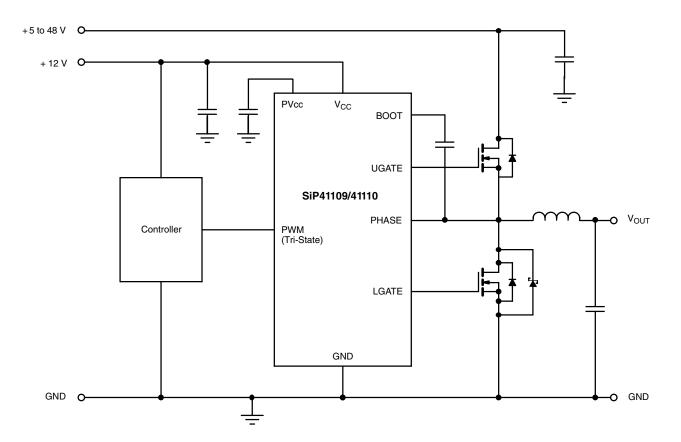
FEATURES

- · PWM with tri-state enable
- 12 V low-side gate drive (SiP41109)
- 8 V low-side gate drive (SiP41110)
- Undervoltage lockout
- · Internal bootstrap diode
- Switching frequency up to 1 MHz
- 30 ns max. propagation delay
- Drive MOSFETs in 5 V to 48 V systems
- Adaptive shoot-through protection

APPLICATIONS

- Multi-phase DC/DC conversion
- High current low voltage DC/DC converters
- High frequency DC/DC converters
- Mobile and desktop computer DC/DC converters
- Core voltage supplies for PC micro-processors

TYPICAL APPLICATION CIRCUIT





ABSOLUTE MAXIMUM RATINGS (all voltages referenced to GND = 0 V)				
Parameter		Limit	Unit	
V _{CC} , PV _{CC}		- 0.3 to 15		
BOOT, PHASE		- 0.3 to 55	V	
BOOT to PHASE		- 0.3 to 15		
Storage Temperature		- 40 to 150	°C	
Operating Junction Temperature		125		
Power Dissipation ^a SO-8		770	mW	
Thermal Impedance (⊖ _{JA}) ^b	30-8	130	°C/W	

Notes:

- a. Device Mounted with all leads soldered or welded to PC board.
- b. Derate 7.7 mW/°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (all voltages referenced to GND = 0 V)				
Parameter	Limit	Unit		
V _{CC}	10.8 to 13.2	V		
V_{LX}	48	v		
C _{BOOT}	100 nF to 1 μF			
BOOT to PHASE	8	V		
Operating Temperature Range	- 40 to 85	°C		

SPECIFICATIONS ^a								
			Test Conditions Unless Specified		Limits			
Parameter		Symbol	$V_{CC} = 12 \text{ V}, V_{BOOT} - V_{PHASE} = 8 \text{ V}$ $T_{A} = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C}$		Min.a	Typ. ^b	Max. ^a	Unit
Power Supplies								
Supply Voltage		V_{DD}			10.8		13.2	V
Quiescent Current		I _{CCQ}	PWM non-switching			5.6	9.5	
Supply Current		1	f _{PWM} = 100 kHz, C _{LOAD} = 3 nF	SiP41109		12.5		mA
Supply Current		I _{DD}	IPWM = 100 KHZ, OLOAD = 3111	SiP41110		11.0		<u> </u>
Tristate (Shutdown) Curre	ent	I _{CCT}	PWM = open			850	1200	μΑ
Reference Voltage								
Break-Before-Make		V _{BBM}				2.5		V
PWM Input								
Input High		V _{IH}			4.0		V_{DD}	V
Input Low		V _{IL}					1.0	V
Bias Current		I _B	PWM 5 V or 0 V			± 600	± 1000	μΑ
Tristate Threshold	High	V _{TSH}			3.0			
mstate mresnoid	Low	V _{TSL}					2.0	V
Tristate Holdoff Timeout ^c t _{TST}					240		ns	
Bootstrap Diode								
Forward Voltage V _F		V _F	I _F = 40 mA, T _A = 25 °C		0.70	0.85	1.0	V



SPECIFICATIONS ^a							
		Test Conditions Unless Specified $V_{CC} = 12 \text{ V, } V_{BOOT} - V_{PHASE} = 8 \text{ V}$ $T_{A} = -40 \text{ °C to } 85 \text{ °C}$		Limits			
Parameter	Symbol			Min.a	Typ. ^b	Max. ^a	Unit
MOSFET Drivers							
High Cide Drive CorrectC	I _{PKH(source)}	V _{BOOT} - V _{PHASE} = 8 V			0.8		
High-Side Drive Current ^c	I _{PKH(sink)}	VBOOT VPHASE - 5 V			1.0		
	I _{PKL(source)}	V _{PVCC} = 8 V	SiP41110		0.9		Α
Low-Side Drive Current ^c	I _{PKL(sink)}	A PACC - 2 1	011 41110		1.2		
Low-Side Drive Current	I _{PKL(source)}	V _{PVCC} = 12 V	SiP41109		1.4		
	I _{PKL(sink)}	1 PAGC = 12 1	011 41100		1.8		
High-Side Driver Impedance	R _{DH(source)}	V _{BOOT} - V _{PHASE} = 8 V, PHASE =	GND		2.3	4.2	
riigh Gide Briver impedance	R _{DH(sink)}	*BOOT *PHASE = 5 *, 1 1 1/102 =	GI 12		1.9	3.5	
	R _{DL(source)}	V _{PVCC} = 8 V	SiP41110		2.9	5.2	Ω
Low-Side Driver Impedance	R _{DL(sink)}	A PACC - 2.1	011 41110		1.3	2.4	32
Low-Gide Driver impedance	R _{DL(source)}	V _{PVCC} = 12 V	SiP41109		2.4	4.3	
	R _{DL(sink)}	V PVCC = 12 V	311 41103		1.2	2.2	
High-Side Rise Time	t _{rH}	10 % - 90 %, V _{BOOT} - V _{PHASE} = 8 V, C _L	04D = 3 nF		45		
High-Side Fall Time	t _{fH}	TO 70 00 70, VBOOT VPHASE - 0 V, OL	OAD - O III		35		
High-Side Rise Time Bypass		10 % - 90 %, V _{BOOT} - V _{PHASE} = 12 V, C _L	3 nF		45		
High-Side Fall Time Bypass		10 % 00 %, VBOOT VPHASE = 12 V, OL	OAD - OIII		35		
High Cids Dysus seties Delevic	t _{d(off)H}	See Timing Waveforms			15		
High-Side Propagation Delay ^c	t _{d(on)H}	See Tilling Wavelollis			15		
Low Cido Diso Timo		C _{LOAD} = 3 HF	SiP41110		40		ns
Low-Side Rise Time	t _{rL}	10 % to 90 %, V_{BOOT} - V_{PHASE} = 12 V C_{LOAD} = 3 nF	SiP41109		40		110
		10 % to 90 %, V_{BOOT} - V_{PHASE} = 8 V_{COAD} = 3 nF	SiP41110		30		
Low-Side Fall Time	t _{fL}	10 % to 90 %, V_{BOOT} - V_{PHASE} = 12 V C_{LOAD} = 3 nF	SiP41109		30		
Law Oida Bassassation Balan	t _{d(off)L}	1			15		
Low-Side Propagation Delay	t _{d(on)L}	See Timing Waveforms			15		
PHASE Timer	1						
PHASE Falling Timeout ^c	t _{PHASE}				380		ns
PV _{CC} Regulator							
Output Voltage	PV _{CC}			7.6	8	8.4	V
Output Current	I _{PVCC}				80	100	m ^
Current Limit	I _{LIM}	V _{DRV} = 0 V		120	200	280	mA
Line Regulation	LNR	V _{CC} = 10.8 V to 13.2 V			0.05	0.5	%/V
Load Regulation	LDR	5 mA to 80 mA			0.1	1.0	%
PV _{CC} Regulator UVLO							
PV _{CC} Rising	V				6.7	7.2	V
PV _{CC} Falling	$V_{\rm UVLO2}$				6.4	6.9	V
Hysteresis	Hyst			100	300	500	mV
High-Side Undervoltage Locko	ut						
Threshold	V _{UVHS}	Rising or falling		2.5	3.35	4.0	V
V _{CC} Undervoltage Lockout							
Threshold	V _{UVLO1}			5.0	5.3	5.6	V
Power on Reset Time	POR				2.5		ms
Thermal Shutdown							
Temperature	T _{SD}	Temperature rising			165		°C
Hysteresis	T _H	Temperature ralling			25		U

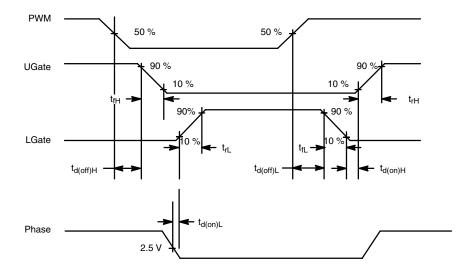
Notes:

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

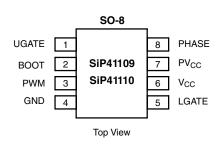
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at V_{CC} = 12 V unless otherwise noted.

TIMING WAVEFORMS





PIN CONFIGURATION AND TRUTH TABLE



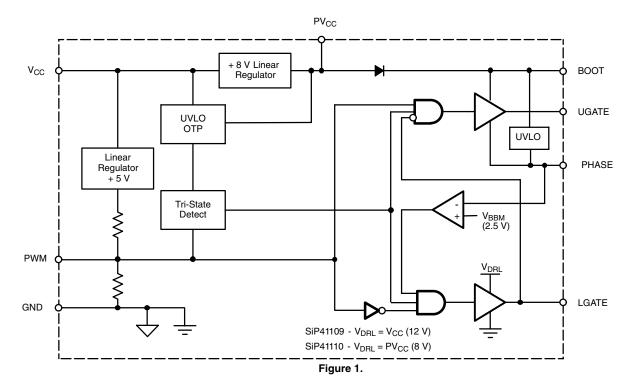
TRUTH TABLE			
PWM	UGATE	LGATE	
L	L	Н	
L	Н	L	
Tri-State	L	L	

ORDERING INFORMATION				
Part Number	Temperature Range	Marking		
SiP41109DY-T1-E3	- 40 °C to 85 °C	41109		
SiP41110DY-T1-E3	- 40 0 10 65 0	41110		
Eval Kit	Temperature Range			
SiP41109DB	- 40 °C to 85 °C			
SiP41110DB	1 40 0 10 63 0			

PIN DESC	PIN DESCRIPTION				
Pin Number	Name	Function			
1	UGATE	8 V high-side MOSFET gate drive			
2	BOOT	Bootstrap supply for high-side driver. The bootstap capacitor is connected between BOOT and PHASE.			
3	PWM	Input signal for the MOSFET drivers and tri-state enable			
4	GND	Ground			
5	LGATE	Synchronous or low-side MOSFET gate drive			
6	V _{CC}	12 V supply. Connect a bypass capacitor ≥ 1 μF from here to ground			
7	PV_{CC}	8 V voltage regulator Output. Connect a bypass capacitor ≥ 1 μF from here to ground			
8	PHASE	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor			



FUNCTIONAL BLOCK DIAGRAM



DETAILED OPERATION

PWM/Tri-State Enable

The PWM pin controls the switching of the external MOSFETs. The driver logic operates in a noninverting configuration. The PWM input stage should be driven by a signal with fast transition times, like those provided by a PWM controller or logic gate, (< 200 ns). The PWM input functions as a logic input and is not intended for applications where a slow changing input voltage is used to generate a switching output when the input switching threshold voltage is reached.

Shutdown

The SiP41109/41110 enters shutdown mode when the signal driving PWM enters the tri-state window for more than 240 ns. The shutdown state is removed when the PWM signal moves outside the tri-state window. If the PWM is left open, the pin is held to 2.5 V by an internal voltage divider, thus forcing the tri-state condition.

Low-Side Driver

In the SiP41109, the low-side driver voltage is supplied by V_{CC} . In the SiP41110, the low-side driver voltage is supplied by PV_{CC} . During shutdown, LGATE is held low.

High-Side Driver

The high-side driver is isolated from the substrate to create a floating high-side driver so that an N-channel MOSFET can be used for the high-side switch. The high-side driver voltage is supplied by $\mbox{PV}_{CC}.$ The voltage is maintained by a floating bootstrap capacitor, which is continually recharged by the switching action of the output. During shutdown UGATE is held low.

Gate Drive Voltage (PV_{CC}) Regulator

An integrated 80 mA, 8 V regulator supplies voltage to the PV_{CC} pin and it current limits at 200 mA typical when the output is shorted to ground. A capacitor (1 μF minimum) must be connected to the PV_{CC} pin to stabilize the regulator output. The voltage on PV_{CC} is supplied to the integrated bootstrap diode. PV_{CC} is used to recharge the bootstrap capacitor and powers the SiP41110 low-side driver. PV_{CC} pin can be externally connected to V_{CC} to bypass the 8 V regulator and increase high-side gate drive to 12 V. If the PV_{CC} pin is connected to V_{CC} the system voltage should not exceed 43 V.

Bootstrap Circuit

The internal bootstrap diode and an external bootstrap capacitor supply voltage to the BOOT pin. An integrated bootstrap diode replaces the external diode normally needed

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for the bootstrap circuit; only a capacitor is necessary to complete the bootstrap circuit. The bootstrap capacitor is sized according to

$$C_{BOOT} = (Q_{GATE}/(\Delta V_{BOOT} - V_{PHASE})) \times 10$$

where Q_{GATE} is the gate charge needed to turn on the high-side MOSFET and ΔV_{BOOT} - PHASE is the amount of droop allowed in the bootstrapped supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1 μF to 1 μF . The bootstrap capacitor voltage rating must be greater than V_{CC} + 12 V to withstand transient spikes and ringing.

Shoot-Through Protection

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the PHASE pin and the LGATE pin and control the switching as follows: When the signal on PWM goes low, UGATE will go low after an internal propagation delay. After the voltage on PHASE falls below 2.5 V by the inductor action, the low-side driver is enabled and LGATE goes high after some delay. When the signal on PWM goes high, LGATE will go low after an internal propagation delay. After the voltage on LGATE drops below



2.5 V the high-side driver is enabled and UGATE will go high after an internal propagation delay. If PHASE does not drop below 2.5 V within 380 ns after UGATE goes low, LGATE is forced high until the next PWM transition.

V_{CC} Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1 μF ceramic capacitor as close as practical between the V_{CC} and GND pins.

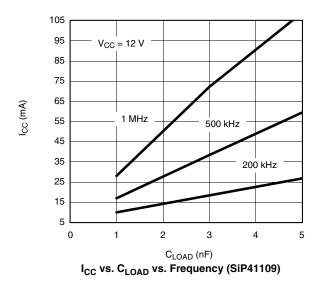
Undervoltage Lockout

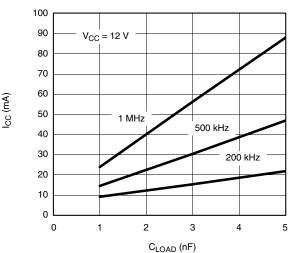
Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces LGATE and UGATE to low when V_{CC} is below its specified voltage. A separate UVLO forces UGATE low when the voltage between BOOT and PHASE is below the specified voltage.

Thermal Protection

If the die temperature rises above 165 $^{\circ}$ C, the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140 $^{\circ}$ C.

TYPICAL CHARACTERISTICS





I_{CC} vs. C_{LOAD} vs. Frequency (SiP41110)



TYPICAL WAVEFORMS

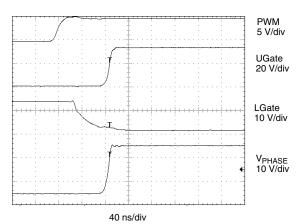


Figure 2. PWM Signal vs. HS Gate, LS Gate and PHASE (Rising)

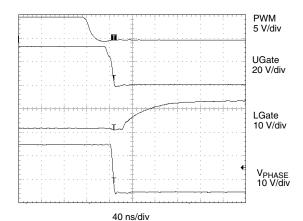


Figure 3. PWM Signal vs. HS Gate, LS Gate and PHASE (Falling)

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