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HALOGEN

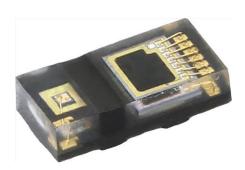
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A Small Package Proximity Sensor With a VCSEL, Low Idle Current, I²C Interface, and Smart Dual Slave Address



LINKS TO ADDITIONAL RESOURCES





DESCRIPTION

The VCNL36828P is a fully integrated proximity sensor. It combines a vertical-cavity surface-emitting laser (VCSEL), photodiode, and application-specific integrated circuit (ASIC) within a single package. The VCNL36828P has been developed for proximity detection applications that require a dual slave address, low power consumption, small package size, small window size, and short range operation. In addition, given the typical rated supply voltage of 1.8 V to reduce power consumption, the sensor is intended for battery-powered applications.

FEATURES

- Package type: surface-mount
- Dimensions (L x W x H in mm): 2.0 x 1.0 x 0.5
- Integrated modules: vertical-cavity surfaceemitting laser (VCSEL), photodiode, and application-specific integrated circuit (ASIC)
- 1.8 V rated power supply and I²C bus
- Low power consumption with 5 μA idle current
- A small package allows a design with a small window size
- Smart dual I2C slave address in one package
- Immunity to red glow (940 nm VCSEL)
- Programmable I_{VCSEL} sink current
- Intelligent cancellation to reduce cross talk phenomenon
- Smart persistence scheme to reduce measurement response time
- · Interrupt functionality
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Smartphones and true wireless stereo (TWS) earbuds
- VR / AR headsets and smart glasses
- Smartwatches
- Touchless button / dispensing

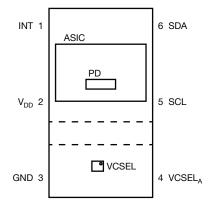
PRODUCT SUMMARY										
PART NUMBER	OPERATING RANGE (mm)	OPERATING VOLTAGE RANGE (V)	I ² C BUS VOLTAGE RANGE (V)	MAX. VCSEL DRIVING CURRENT (mA)	OUTPUT	ADC RESOLUTION PROXIMITY / AMBIENT LIGHT				
VCNL36828P	200	1.65 to 2.00	1.2 to 3.6	20	12 bit / 16 bit, I ² C	16 bit / -				

ORDERING INFORMATION								
ORDERING CODE	PACKAGING	VOLUME (1)	REMARKS					
VCNL36828P	Tape and reel	MOQ: 5000 pcs, 5000 pcs/reel	2.0 mm x 1.0 mm x 0.5 mm					

Note

(1) MOQ: minimum order quantity





PIN DESCRIPTION	PIN DESCRIPTION									
PIN NUMBER	PIN NAME	ТҮРЕ	DESCRIPTION							
1	INT	O (open drain)	Interrupt							
2	V _{DD}	I	Supply voltage							
3	GND	1	Ground							
4	VCSEL _A	I	VCSEL anode							
5	SCL (1)	I / O (open drain)	I ² C serial clock							
6	SDA ⁽¹⁾	I / O (open drain)	I ² C serial data							

Note

⁽¹⁾ Pin 5 (SCL) and pin 6 (SDA) can be swapped to change the slave address from 0x60 to 0x51; please refer to Table 1

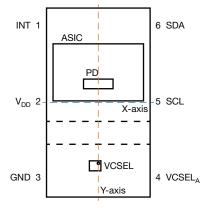
ABSOLUTE MAXIMUM RATINGS (T _{amb} = 25 °C, unless otherwise specified)									
PARAMETER TEST CONDITION SYMBOL MIN. MAX. UNIT									
Supply voltage		V _{DD}	0	2	V				
Ambient temperature range		T _{amb}	-40	+85	°C				
Storage temperature range		T _{stg}	-40	+100	°C				



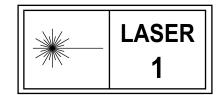
BASIC CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)										
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT				
ASIC										
Supply voltage		V_{DD}	1.65	1.80	2.00	V				
(4)	Shutdown state; light condition = dark; $V_{DD} = 1.8 \text{ V}$		-	1	-					
Supply current (1)	Idle state ⁽²⁾ ; V _{DD} = 1.8 V	I _{DD}	-	5	-	μA				
	Active state (2); V _{DD} = 1.8 V		-	330	-					
I ² C supply voltage		V _{PULL UP}	1.2	1.8	3.6	V				
I ² C signal input, logic high	V _{DD} = 1.8 V	V _{IH}	1	-	-	V				
I ² C signal input, logic low	V _{DD} = 1.8 V	V _{IL}	-	-	0.5	V				
VCSEL										
Supply voltage of the VCSEL (3)		V _{VCSEL}	2.62		3.60	V				
Forward voltage	I _F = 9 mA	V _F	-	1.92	-	V				
Forward current		I _F	7	-	20	mA				
Angle of half intensity		φ	-	± 4.5	-	0				
Peak wavelength	I _F = 9 mA	λρ	-	940	-	nm				
Spectral bandwidth	I _F = 9 mA	Δλ	-	3	-	nm				
PHOTODIODE										
Angle of helf consists site.	X-axis (4)		-	± 60	-	۰				
Angle of half sensitivity	Y-axis (4)	φ	-	± 45	-					
Peak sensitivity wavelength		λρ	-	850	-	nm				

Notes

- (1) Actual current consumption depends on the register settings. Please refer to the application note on the current consumption
- (2) Excluding VCSEL driving current
- (3) V_{VCSEL} should at least match the minimum required supply voltage for the VCSEL V_{VCSEL, min}. Please refer to the V_{VCSEL, min} table
- (4) Cross section of the package



V _{VCSEL, MIN.}								
PS_CURRENT (I _F)	7 mA	9 mA	11 mA	12 mA	15 mA	17 mA	19 mA	20 mA
V _{VCSEL, min.}	2.62 V	2.74 V	2.86 V	2.91 V	3.08 V	3.19 V	3.3 V	3.36 V
V _{VCSEL, max.}				3.6	6 V			

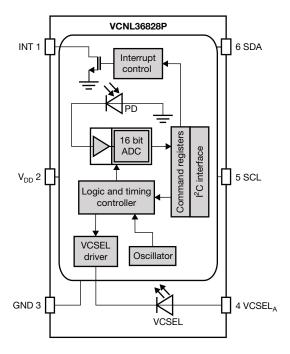


Note

• Product specification with IEC / EN 60825-1:2014 compliance and above label

BLOCK DIAGRAM

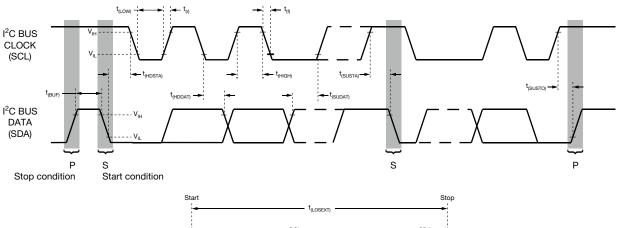
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I ² C BUS TIMING CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)									
DADAMETED	SYMBOL	STANDA	RD MODE	FAST	MODE	LINUT			
PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT			
Clock frequency	f _(I2CCLK)	10	100	10	400	kHz			
Bus free time between start and stop condition	t _(BUF)	4.7	-	1.3	-	μs			
Hold time after (repeated) start condition; after this period, the first clock is generated	t _(HDSTA)	4.0	-	0.6	-	μs			
Repeated start condition setup time	t _(SUSTA)	4.7	-	0.6	-	μs			
Stop condition setup time	t _(SUSTO)	4.0	-	0.6	-	μs			
Data hold time	t _(HDDAT)	0	3450	0	900	ns			
Data setup time	t _(SUDAT)	250	-	100	-	ns			
I ² C clock (SCL) low period	t _(LOW)	4.7	-	1.3	-	μs			
I ² C clock (SCL) high period	t _(HIGH)	4.0	-	0.6	-	μs			
Clock / data fall time	t _(f)	=	300	-	300	ns			
Clock / data rise time	t _(r)	-	1000	-	300	ns			

Note

• Data based on standard I²C protocol requirement, not tested in production



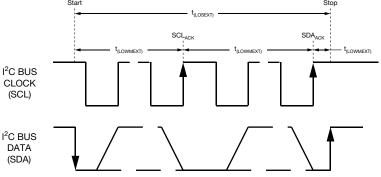


Fig. 1 - I²C Bus Timing Diagram

PARAMETER TIMING INFORMATION

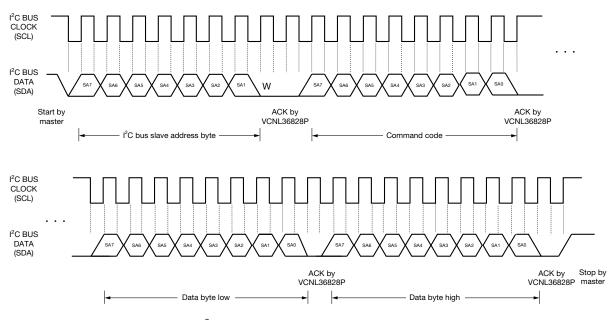


Fig. 2 - I²C Bus Timing for Sending Word Command Format

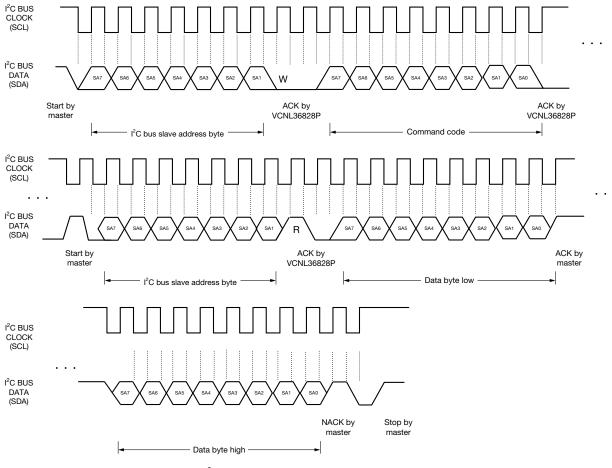


Fig. 3 - I²C Bus Timing for Receiving Word Command Format

TYPICAL PERFORMANCE CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

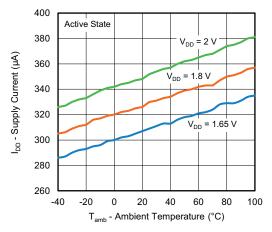


Fig. 4 - Supply Current vs. Ambient Temperature

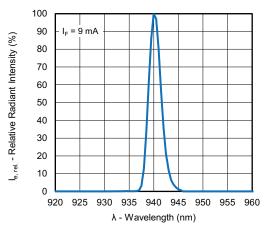


Fig. 7 - Relative Radiant Intensity vs. Wavelength of the VCSEL

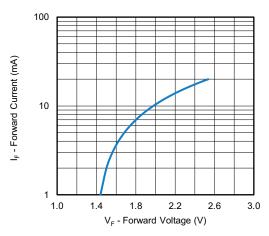


Fig. 5 - Forward Current vs. Forward Voltage of the VCSEL

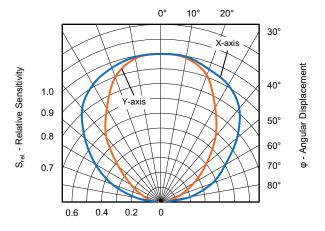


Fig. 8 - Relative Sensitivity vs. Angular Displacement of the Photodiode

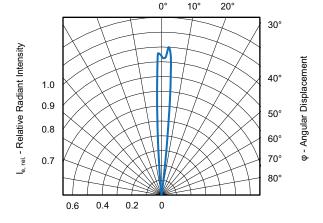


Fig. 6 - Relative Radiant Intensity vs. Angular Displacement of the VCSEL

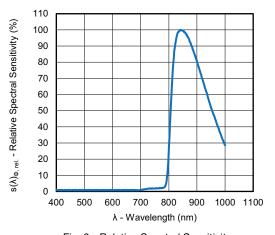
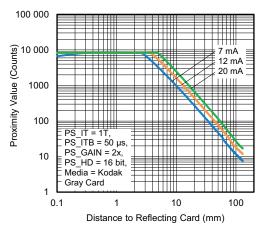
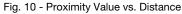


Fig. 9 - Relative Spectral Sensitivity vs. Wavelength of the Photodiode







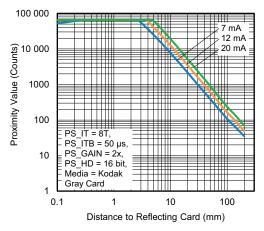


Fig. 11 - Proximity Value vs. Distance

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APPLICATION INFORMATION

Slave Address Selection

The VCNL36828P supports a smart dual slave address where the designer can change the slave address by swapping the SCL and SDA pins, as shown in Table 1.

TABLE 1	TABLE 1 - SLAVE ADDRESS TABLE								
PIN 5	PIN 6	7 BIT SLAVE ADDRESS	8 BIT SLAVE ADDRESS (WRITE)	8 BIT SLAVE ADDRESS (READ)					
SCL	SDA	0x60	0xC0	0xC1					
SDA	SCL	0x51	0xA2	0xA3					

A smart dual slave address provides the flexibility for the designer to connect two devices from two different slave addresses on the same I²C bus. Besides that, the two slave address options allow designers to select a different slave address if one is used by the other slave devices on the same I²C bus in a single device application.

Application Circuit With a Single Device - Slave Address 0x60

Fig. 12 shows an application circuit example with a single device. As described in Table 1, when pins 5 and 6 are connected to the clock and data signal from the microcontroller, as shown in Fig. 12, they will then be configured as an SCL pin and SDA pin, respectively. The 7 bit slave address option of 0x60 will be automatically selected.

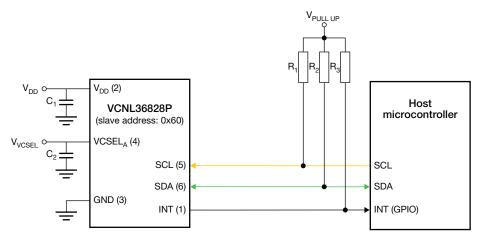


Fig. 12 - Application Circuit Example for a Single VCNL36828P - Slave Address 0x60



Application Circuit With a Single Device - Slave Address 0x51

On the other hand, when pins 5 and 6 are connected to the data and clock signal from the microcontroller, as shown in Fig. 13, they will then be configured as an SDA pin and SCL pin, respectively. The 7 bit slave address option of 0x51 will be automatically selected.

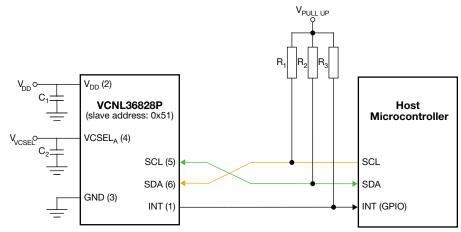


Fig. 13 - Application Circuit Example for a Single VCNL36828P - Slave Address 0x51

Table 2 shows the required values and the explanation for the individual application circuit parameters.

TABLE 2 - A	TABLE 2 - APPLICATION CIRCUIT PARAMETERS							
CIRCUIT PARAMETER	VALUE	DESCRIPTION						
V _{DD}	1.65 V to 2.00 V	A stable power supply such as a low dropout regulator or a switching regulator is required; the power supply isolation can be further improved with a decoupling capacitor C ₁						
V _{VCSEL}	2.62 V to 3.60 V	A stable power supply such as a low dropout regulator or a switching regulator that can supply an adequate amount of power (max. VCSEL pulse driving current of 20 mA) is required; the power supply isolation can be further improved with a decoupling capacitor C ₂ ; the minimum voltage depends on the selected driving current of the VCSEL; please refer to Table V _{VCSEL, min.} for reference						
V _{PULL UP}	1.2 V to 3.6 V	A stable power supply such as a low dropout regulator or a switching regulator is required; a voltage level shifter is required if the I ² C bus voltage from the microcontroller is higher than 3.6 V						
C ₁ - C ₄	100 nF to 1 μF	Decoupling capacitors are recommended to reduce the noise in the supply voltage						
R ₁ - R ₂	2.2 kΩ to 4.7 kΩ	Pull-up resistors within the range of 2.2 k Ω to 4.7 k Ω are recommended; any increase in bus capacitance or resistance will increase the logic high transition time						
R ₃	$4.7~\text{k}\Omega$ to $22~\text{k}\Omega$	Pull-up resistor within the range of 4.7 k Ω to 22 k Ω is recommended						



Application Circuit With a Smart Dual Slave Address

Fig. 14 shows an application circuit example with a smart dual slave address. By swapping the SCL and SDA pins of the second device, as shown in Table 1, the designer can change the 7 bit slave address of the VCNL36828P. This provides the flexibility for the designer to connect two devices from two different slave addresses on the same I²C bus.

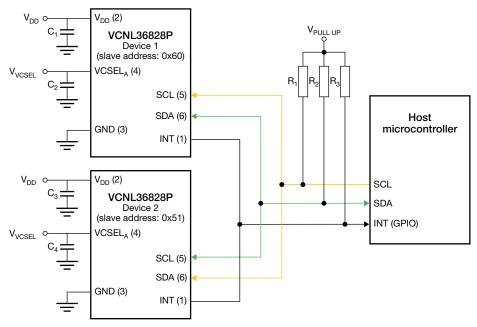


Fig. 14 - Application Circuit Example for Two VCNL36828Ps - Smart Dual Slave Address

I²C Write and Read Protocol

The communication with the VCNL36828P can be performed via I²C. The I²C write and read protocol when communicating with the proximity sensor is shown in Fig. 15.

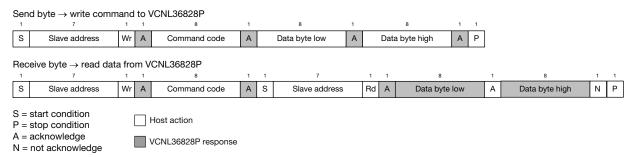


Fig. 15 - I²C Write and Read Protocol

It is imperative that only the restart condition for the I2C read is implemented instead of the stop and restart condition.



Function Description

COMMAND	DATA BYTE LOW / HIGH	REGISTER NAME	DEFAULT VALUE	FUNCTION	ACCESS	
				Internal calibration setting		
	L	PS_CONF1_L	0x00	Switch the sensor on / off		
0x00				High dynamic range setting		
	Н	PS_CONF1_H	0x00	Persistence setting		
				Interrupt setting		
				Measurement period setting		
	L	PS_CONF2_L	0x00	Signal strength setting (Integration time and multi-pulse)		
001				High gain setting		
0x01				Sensitivity of the ADC setting		
	Н	H PS_CONF2_H	0x00	Internal crosstalk cancellation setting		
				VCSEL driving current setting	Write and read	
		L PS CONF3 L		PS CONF3 L 0x00 Sensor mode setting		
0x02	L	L PS_CONF3_L	0000	Active force mode trigger setting		
UXU2	11	H PS CONF3 H	0x00	Short measurement period setting		
	П	H P5_CONF3_H		Sunlight cancellation setting		
0x03	L	PS_THDL_L	0x00	Low threshold interrupt value setting (low byte)		
UXUS	Н	PS_THDL_H	0x00	Low threshold interrupt value setting (high byte)		
0x04	L	PS_THDH_L	0x00	High threshold interrupt value setting (low byte)		
0X04	Н	PS_THDH_H	0x00	High threshold interrupt value setting (high byte)		
0x05	L	PS_CANC_L	0x00	Offset count cancellation value setting (low byte)		
0x05	Н	PS_CANC_H	0x00	Offset count cancellation value setting (high byte)		
0xF8	L	PS_DATA_L	0x00	Proximity output data (low byte)		
UXI O	Н	PS_DATA_H	0x00	Proximity output data (high byte)		
0xF9	L	Reserved	0x00 - 0xFF	Reserved		
UXI 9	Н	INT_FLAG	0x00	Interrupt flag	Read only	
0xFA	L	VCNL36828P_ID_L	0x28 / 0x29	Device ID Slave address: 0x60; ID = 0x28 Slave address: 0x51; ID = 0x29		
	Н	VCNL36828P_ID_H	0x01	Device ID		

Notes

[•] All of the reserved registers are used for internal test. These values must be kept constant

⁽¹⁾ The default ID depends on the connection of the SCL and SDA pins on the VCNL36828P with the SCL and SDA pins on the host MCU. If pins 5 and 6 on the VCNL36828P are connected to the SCL and SDA pins on the host, the default value will be 0x28. On the other hand, if pins 5 and 6 on the VCNL36828P are connected to the SDA and SCL pins on the host, the default value will be 0x29. Please refer to Fig. 13



Command Register Format

TABLE 4	TABLE 4 - REGISTER NAME: PS_CONF1_L										
Bit 7	Bit 6	Bit 5 Bit 4		Bit 3	Bit 2	Bit 1	Bit 0				
PS_CAL			Reserved				PS_ON				
COMMAND (CODE					0x00					
Bit N	lame	Fund	tion	Bit	Value	Descr	ription				
PS	CAL	Enable / disable the internal calibration		7	0x0 (0b0)	Disable (default)					
F3_	OAL	Litable / disable the	7 disable the internal calibration		0x1 (0b1)	(0b1) Enable					
Rese	erved	Reserved		6:1	0x00 (0b000000)	Should be I	cept default				
PS_ON		S ON Switch the sensor on / off		PS_ON Switch the sensor on / off		0	0x0 (0b0)	0x0 (0b0) Turn off the senso (shutdown) (defaul			
			0x1 (0b1)			Turn on the sensor					

TABLE 5	- REGISTER	R NAME: PS_CON	IF1_H					
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
Reserved	PS_HD	PS_SP_INT	PS_SMART_PERS	PS_F	PERS	PS_	INT	
COMMAND (CODE					0x00		
Bit N	lame	Fund	ction	Bit	Value	Descr	iption	
Rese	erved	Rese	erved	15	0x0 (0b0)	Should be I	kept default	
De	HD	Enable / disable high o	lynamic range (12 bit /	14	0x0 (0b0)	Disable (12	bit) (default)	
P5_	_HD	16 bit) ADC o	output setting	14	0x1 (0b1)	Enable	Enable (16 bit)	
DC C	D INIT	Enable / disable the sunlight protection mode interrupt setting		13	0x0 (0b0)	Disable (default)		
PS_S	P_IINT			13	0x1 (0b1)	Enable		
DC CMAI	RT PERS	Enable / disable the smart persistence		12	0x0 (0b0)	Disable	(default)	
F3_SIVIAI	NI_FENO	setting when the interrupt event is triggered		12	0x1 (0b1)	Ena	able	
					0x0 (0b00)	1 time (default)	
PS F	DEDO		onsecutive threshold	11 : 10	0x1 (0b01)	2 times		
F5_F	TENO	_	ecessary to trigger rupt	11.10	0x2 (0b10)	3 times		
			·		0x3 (0b11)	4 times		
					0x0 (0b00)	Interrupt disa	able (default)	
PS	INT	Set the interrur	nt mode setting	9:8	0x1 (0b01)	Logic high	Logic high / low mode	
10_	-11 4 1	Set the interrupt mode setting		3.0	0x3 (0b11)	Trigger by each high / low threshold event		



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TABLE 6 - F	REGISTER N	AME: PS_CO	NF2_L				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS_PE	RIOD	PS.	_IT	PS_I	MPS	PS_ITB	PS_GAIN
COMMAND COI	DE					0x01	
Bit Na	ame	Fund	ction	Bit	Value	Description	
				7:6	0x0 (0b00)	50 ms, which 20 measurem	
PS_PERIOD	Cat the massu	romant pariod	0x1 (0b01)			translates into rements/s	
	NIOD	Set the measurement period			0x2 (0b10)	200 ms, which translates into 5 measurements/s	
					0x3 (0b11)	400 ms, which 2.5 measu	
		Set the integration time for one measurement; the pulse length "T" is determined by PS_ITB		5 : 4	0x0 (0b00)	1 T (d	efault)
PS	IT				0x1 (0b01)	2 T	
F3_	, ,				0x2 (0b10)	4 T	
			•		0x3 (0b11)	8 T	
					0x0 (0b00)	1 pulse	(default)
PS M	1DC	Set the number of	of infrared signal	3:2	0x1 (0b01)	2 pulses	
F3_IVI	IF 3	pulses per m	neasurement	3.2	0x2 (0b10)	4 pu	lses
					0x3 (0b11)	8 pulses	
PS I	TD	Set the pulse length "T" for PS_IT		1	0x0 (0b0)	T = 25 μs	(default)
F3_I	10			'	0x1 (0b1)	T = 5	i0 μs
PS G	AINI	Set the gain	of the ADC	0	0x0 (0b0)	x 1 gain (default)	
P3_G	All N	Set the gain	OI THE ADO	U	0x1 (0b1)	x 2	gain

TABLE 7 -	REGISTER I	NAME: PS_C	ONF2_H				
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Rese	erved	PS_SENS	PS_OFFSET	Reserved		PS_CURRENT	
COMMAND C	ODE					0x01	
Bit N	lame	Fu	nction	Bit	Value	Desci	ription
Rese	erved	Re	served	15 : 14	0x0 (0b00)	Should be	kept default
De c	SENS	Cat the same	itivity of the ADC	13	0x0 (0b0)	Normal sensi	tivity (default)
PS_3	DEINO	Set the sens	illvity of the ADC	13	0x1 (0b1)	High sensitivity	
DS OI	FFSET	Enable / disable the internal crosstalk cancellation		12	0x0 (0b0)	Disable (default)	
F3_0i	ITSLI				0x1 (0b1)	Ena	able
Rese	erved	Re	Reserved		0x0 (0b0)	Should be	kept default
					0x0 (0b000)	7 mA (default)	
					0x1 (0b001)	9 mA	
					0x2 (0b010)	11 mA	
DC CLI	RRENT	Sot the VCS	EL driving current	10 : 8	0x3 (0b011)	12 mA	
F3_00	THEN	Set the VOSI	LE driving current	10.8	0x4 (0b100)	15 mA	
					0x5 (0b101)	17	mA
					0x6 (0b110)	19 mA	
					0x7 (0b111)	20	mA



TABLE 8 - MAX	(IMUM BIT RESO	LUTION AND DI	GITAL OUTPUT O	OUNTS				
BIT	NAME	PS_IT = 1T	PS_IT = 2T	PS_IT = 4T	PS_IT = 8T			
PS_HD = 0 (12 bit)	PS_GAIN = 0 (x1 gain)		12 bit / 4095 counts					
F3_11D = 0 (12 bit)	PS_GAIN = 1 (x2 gain)	12 DR / 4095 COURTS						
PS_HD = 1 (16 bit)	PS_GAIN = 0 (x1 gain)	12 bit / 4095 counts	13 bit / 8191 counts	14 bit / 16 383 counts	15 bit / 32 767 counts			
F3_ND = 1 (10 bit)	PS_GAIN = 1 (x2 gain)	13 bit / 8191 counts	14 bit / 16 383 counts	15 bit / 32 767 counts	16 bit / 65 535 counts			

TABLE 9 -	REGISTER	NAME: PS_C	ONF3_L					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Rese	erved	PS_TRIG PS_MODE			Reserved			
COMMAND CO	IAND CODE 0x02							
Bit N	lame	Fu	ınction	Bit	Value Description			
Rese	erved	Re	eserved	7:6	0x0 (0b00)	Should be kept default		
PS 1	TRIC	Set the active force mode trigger; This bit will be reset to 0 after the measurement cycle		5	0x0 (0b0)	Off (default)		
F3_1	inia			3	0x1 (0b1)	Trigger		
DC M	1ODE	Set the mea	asurement mode	4	0x0 (0b0)	Auto mode (default)		
P5_IV	PS_MODE		of the sensor		0x1 (0b1)	Active force mode		
Rese	erved	Re	eserved	3:0	0x0 (0b0000)	Should be	kept default	

TABLE 10	- REGISTER	NAME: PS_	CONF3_H						
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
PS_SP	ERIOD	Reserved		PS_SC		Rese	erved		
COMMAND C	ODE					0x02			
Bit N	lame	Fu	nction	Bit	Value	Desci	ription		
					0x0 (0b00)	(follow PS_PE	short period :RIOD setting) ault)		
PS_SP	PS_SPERIOD		Set the short measurement period		0x1 (0b01)	6.25 ms, which translates int 160 measurements/s			
					0x2 (0b10)	12.5 ms, which translates in 80 measurements/s			
					0x3 (0b11)	25 ms, which translates into 40 measurements/s			
Rese	erved	Re	served	13	0x0 (0b0)	Should be	kept default		
500	PG GC:		e / disable	12 : 10	0x0 (0b000)	Disable	(default)		
PS ₋			the sunlight cancellation		0x7 (0b111)	Enable			
Rese	erved	Re	served	9:8	0x0 (0b00)	Should be	kept default		



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TABLE 11	TABLE 11 - REGISTER NAME: PS_THDL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
PS_THDL_L								
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	PS_THDL_H							
COMMAND C	ODE					0x03		
Bit N	lame	Fu	ınction	Bit	Value	Description		
PS_TI	HDL_L	Sat the law thro	Cat the law threehold interment value		0 to 65 535	Low byte		
PS_TI	HDL_H	Set the low threshold interrupt value		15:8	0 10 03 333	High byte		

TABLE 12	- REGISTER	R NAME: PS_	THDH					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
PS_THDH_L								
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
			PS_THDI	1_H				
COMMAND C	ODE					0x04		
Bit N	lame	Fu	ınction	Bit	Value	Desci	ription	
PS_TI	HDH_L	Cat the high three	Cataba biah thurah aldistanyunt valua		0 to 65 535	Low byte		
PS_TI	HDH_H	Set the high threshold interrupt value		15:8	0 10 03 333	High byte		

TABLE 13	- REGISTER	NAME: PS_0	CANC					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
	PS_CANC_L							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Re	eserved			PS_CAN	IC_H		
COMMAND C	ODE					0x05		
Bit N	lame	Fu	inction	Bit	Value	Descr	iption	
PS_C/	ANC_L	Set t	the offset	7:0	0 to 4095	Low byte		
PS_CA	ANC_H	count cancellation value		11:8	0 10 4095	High byte		
Rese	erved	Re	eserved	15 : 12	0x0 (0b0000)	Should be kept default		

TABLE 14	TABLE 14 - REGISTER NAME: PS_DATA								
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
PS_DATA_L									
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
			PS_DATA	\ _H					
COMMAND C	ODE					0xF8			
Bit N	lame	Fu	ınction	Bit	Value	Description			
PS_D	ATA_L	Dood the pro	Dood the considerity of the state		0 to 65 535	Low byte			
PS_D/	ATA_H	Read the proximity output data		15:8	0 10 65 555	High byte			



TABLE 15	- REGISTER	NAME: INT	FLAG				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Reserv	ed			
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	Reserved		PS_SPFLAG	Rese	erved	PS_IF_CLOSE	PS_IF_AWAY
COMMAND CODE 0xF9							
Bit N	lame	Fu	ınction	Bit	Value	Desci	ription
Rese	erved	Re	eserved	7:0	0x00 - 0xFF (0b00000000 - 0b11111111)	Should be l	kept default
Rese	erved	Reserved		15 : 13	0x0 (0b000)	Should be l	kept default
PS SI	PFLAG	Read the sunlight protection mode interrupt event flag		12	0x0 (0b0)	No sunlight pr interrupt	
1 0_01	TEAG				0x1 (0b1)	Sunlight protection mode interrupt event flag	
Rese	erved	Re	eserved	11 : 10	0x0 (0b00)	Should be kept default	
DC IE	CLOSE	Read the high	threshold crossing	9	0x0 (0b0)	No high threshold crossing interrupt event flag	
PS_IF_CLOSE ''"		interrup	ot event flag	Đ	0x1 (0b1)	High threshold crossing interrup event flag	
DO IE	PS IF AWAY		Read the low threshold crossing		0x0 (0b0)	No low threshold crossing interrupt event flag	
P5_IF_	_AVVA I	interrup	ot event flag	8	0x1 (0b1)	Low threshold crossing interru event flag	

TABLE 16	- REGISTER	NAME: VCN	L36828P_ID					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
			VCNL36828	P_ID_L				
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
			VCNL36828	P_ID_H				
COMMAND C	ODE				0xFA			
Bit I	Name	Fu	nction	Bit	Value	Desci	ription	
VCNI 26	ו מפס			7.0	0x28 (0b00101000)	Device with a slave address of 0x60		
VCNL36828P_ID_L VCNL36828P_ID_H		Read the device ID		7:0	0x29 (0b00101001)	Device with a slave address of 0x51		
				15 : 8	0x01 (0b0000001)	Should be kept default		

PACKAGE INFORMATION in millimeters

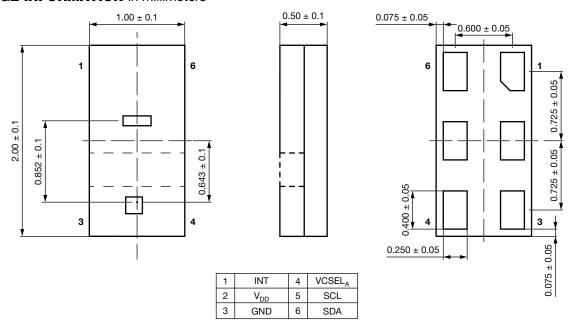


Fig. 16 - VCNL36828P Package Dimensions

RECOMMENDED LAYOUT PAD INFORMATION in millimeters

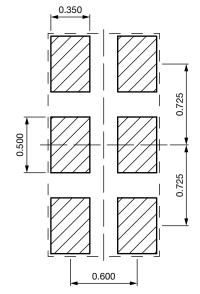


Fig. 17 - VCNL36828P PCB Layout Footprint

RECOMMENDED INFRARED REFLOW

Soldering conditions which are based on J-STD-020C

IR REFLOW PROFILE CONDITION			
PARAMETER	CONDITIONS	TEMPERATURE	TIME
Peak temperature		260 °C + 5 °C / - 5 °C (max.: 265 °C)	10 s
Preheat temperature range and timing		150 °C to 200 °C	60 s to 180 s
Timing within 5 °C to peak temperature		-	10 s to 30 s
Timing maintained above temperature / time		217 °C	60 s to 150 s
Timing from 25 °C to peak temperature		-	8 min (max.)
Ramp-up rate		3 °C/s (max.)	-
Ramp-down rate		6 °C/s (max.)	-

Recommend Normal Solder Reflow is 235 °C to 265 °C

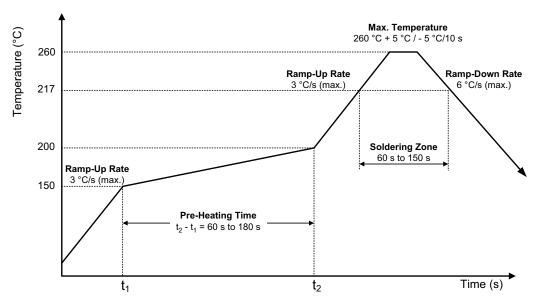
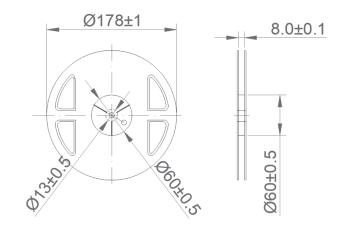
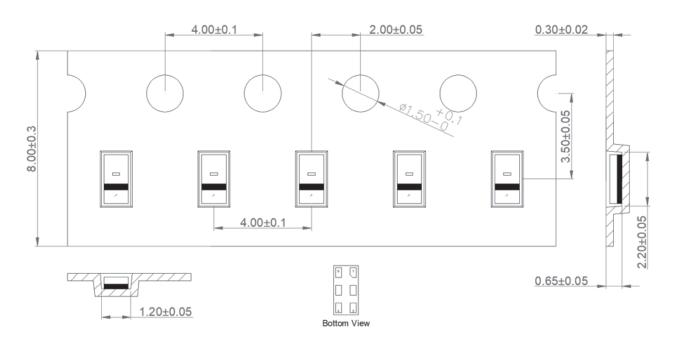


Fig. 18 - VCNL36828P Solder Reflow Profile Chart

TAPE PACKAGING INFORMATION in millimeters







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