N-and P-Channel 30 V (D-S) 175 °C MOSFET

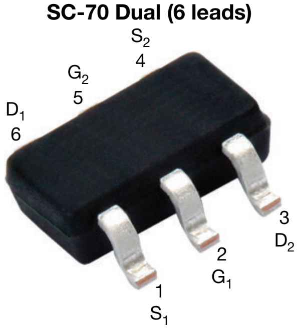
PRODUCT SUMMARY		
	N-CHANNEL	**P-CHANNEL**
V_{DS} (V)	30	-30
$R_{DS(on)}$ (Ω) at V_{GS} = ± 10 V	0.280	0.940
$R_{DS(on)}$ (Ω) at V_{GS} = ± 4.5 V	0.380	1.800
I_D (A)	0.85	-0.85
Configuration	N & P Pair	
Package	SC-70	

FEATURES

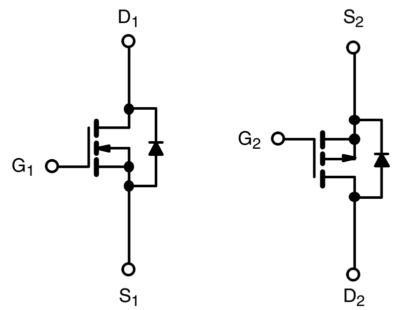
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE
Pb-free
RoHS COMPLIANT
HALOGEN FREE

SOT-363
SC-70 Dual (6 leads)



Top View



N-Channel MOSFET P-Channel MOSFET

Marking Code: 9R

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER		**SYMBOL**	**N-CHANNEL**	**P-CHANNEL**	**UNIT**
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current [c]	T_C = 25 °C	I_D	0.85	-0.85	A
	T_C = 125 °C		0.85	-0.56	
Continuous Source Current (Diode Conduction)		I_S	0.85	-0.85	
Pulsed Drain Current [a]		I_{DM}	3.3	-3.3	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	3.5	-1.9	
Single Pulse Avalanche Energy		E_{AS}	0.6	0.2	mJ
Maximum Power Dissipation [a]	T_C = 25 °C	P_D	1.5	1.5	W
	T_C = 125 °C		0.5	0.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175		°C

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**N-CHANNEL**	**P-CHANNEL**	**UNIT**
Junction-to-Ambient	PCB Mount [b]	R_{thJA}	220	220	°C/W
Junction-to-Foot (Drain)		R_{thJF}	100	100	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. When mounted on 1" square PCB (FR4 material).
c. Package limited.

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)								
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static								
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		N-Ch	30	-	-	V
		V_{GS} = 0 V, I_D = -250 µA		P-Ch	-30	-	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		N-Ch	1	1.8	2.6	
		V_{DS} = V_{GS}, I_D = -250 µA		P-Ch	-1	-1.8	-2.6	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 30 V	N-Ch	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = -30 V	P-Ch	-	-	-1	
		V_{GS} = 0 V	V_{DS} = 30 V, T_J = 125 °C	N-Ch	-	-	50	
		V_{GS} = 0 V	V_{DS} = -30 V, T_J = 125 °C	P-Ch	-	-	-50	
		V_{GS} = 0 V	V_{DS} = 30 V, T_J = 175 °C	N-Ch	-	-	150	
		V_{GS} = 0 V	V_{DS} = -30 V, T_J = 175 °C	P-Ch	-	-	-150	
On-State Drain Current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} = 5 V	N-Ch	2	-	-	A
		V_{GS} = -10 V	V_{DS} = -5 V	P-Ch	-0.5	-	-	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 1 A	N-Ch	-	0.210	0.280	Ω
		V_{GS} = -10 V	I_D = -0.5 A	P-Ch	-	0.788	0.940	
		V_{GS} = 4.5 V	I_D = 0.1 A	N-Ch	-	0.290	0.380	
		V_{GS} = -4.5 V	I_D = -0.1 A	P-Ch	-	1.400	1.800	
Forward Transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 0.7 A		N-Ch	-	1.2	-	S
		V_{DS} = -15 V, I_D = -0.5 A		P-Ch	-	0.6	-	
Dynamic [b]								
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 15 V, f = 1 MHz	N-Ch	-	38	48	pF
		V_{GS} = 0 V	V_{DS} = -15 V, f = 1 MHz	P-Ch	-	40	50	
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 15 V, f = 1 MHz	N-Ch	-	14	21	
		V_{GS} = 0 V	V_{DS} = -15 V, f = 1 MHz	P-Ch	-	14	21	
Reverse Transfer Capacitance	C_{rss}	V_{GS} = 0 V	V_{DS} = 15 V, f = 1 MHz	N-Ch	-	6	10	
		V_{GS} = 0 V	V_{DS} = -15 V, f = 1 MHz	P-Ch	-	5	9	
Total Gate Charge	Q_g	V_{GS} = 4.5 V	V_{DS} = 15 V, I_D = 0.7 A	N-Ch	-	1	1.4	nC
		V_{GS} = -4.5 V	V_{DS} = -15 V, I_D = -0.5 A	P-Ch	-	1.2	1.6	
Gate-Source Charge	Q_{gs}	V_{GS} = 4.5 V	V_{DS} = 15 V, I_D = 0.7 A	N-Ch	-	0.2	-	
		V_{GS} = -4.5 V	V_{DS} = -15 V, I_D = -0.5 A	P-Ch	-	0.3	-	
Gate-Drain Charge [c]	Q_{gd}	V_{GS} = 4.5 V	V_{DS} = 15 V, I_D = 0.7 A	N-Ch	-	0.4	-	
		V_{GS} = -4.5 V	V_{DS} = -15 V, I_D = -0.5 A	P-Ch	-	0.6	-	
Gate Resistance	R_g	f = 1 MHz		N-Ch	5.8	-	17.3	Ω
				P-Ch	3.7	-	11.1	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 20 Ω I_D ≅ 0.7 A, V_{GEN} = 4.5 V, R_g = 1 Ω		N-Ch	-	3	6	ns
		V_{DD} = -15 V, R_L = 20 Ω I_D ≅ -0.5 A, V_{GEN} = -4.5 V, R_g = 1 Ω		P-Ch	-	4	8	
Rise Time	t_r	V_{DD} = 15 V, R_L = 20 Ω I_D ≅ 0.7 A, V_{GEN} = 4.5 V, R_g = 1 Ω		N-Ch	-	18	28	
		V_{DD} = -15 V, R_L = 20 Ω I_D ≅ -0.5 A, V_{GEN} = -4.5 V, R_g = 1 Ω		P-Ch	-	39	50	
Turn-Off Delay Time	$t_{d(off)}$	V_{DD} = 15 V, R_L = 20 Ω I_D ≅ 0.7 A, V_{GEN} = 4.5 V, R_g = 1 Ω		N-Ch	-	8	14	
		V_{DD} = -15 V, R_L = 20 Ω I_D ≅ -0.5 A, V_{GEN} = -4.5 V, R_g = 1 Ω		P-Ch	-	10	16	
Fall Time	t_f	V_{DD} = 15 V, R_L = 20 Ω I_D ≅ 0.7 A, V_{GEN} = 4.5 V, R_g = 1 Ω		N-Ch	-	32	46	
		V_{DD} = -15 V, R_L = 20 Ω I_D ≅ -0.5 A, V_{GEN} = -4.5 V, R_g = 1 Ω		P-Ch	-	17	25	

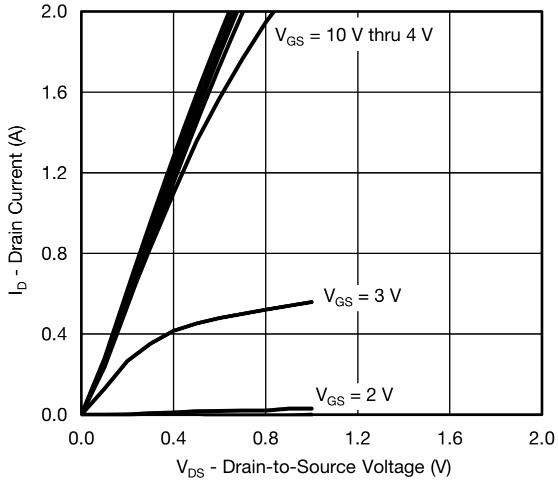
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed Current [a]	I_{SM}	T_C = 25 °C	N-Ch	-	-	3.3	A
			P-Ch	-	-	-3.3	
Forward Voltage	V_{SD}	I_S = 0.5 A	N-Ch	-	0.8	1.2	V
		I_S = -0.4 A	P-Ch	-	-0.8	-1.2	

Notes

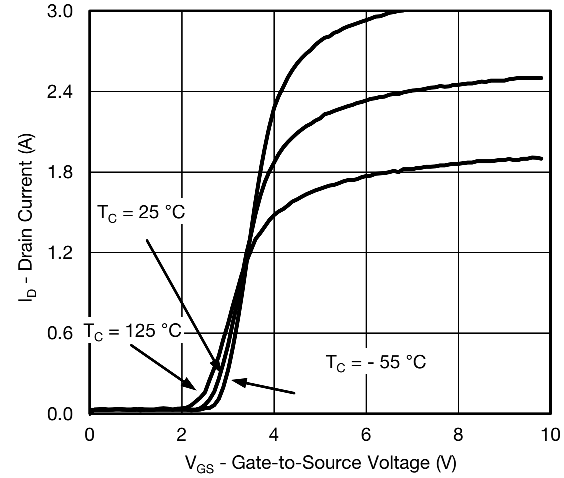
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

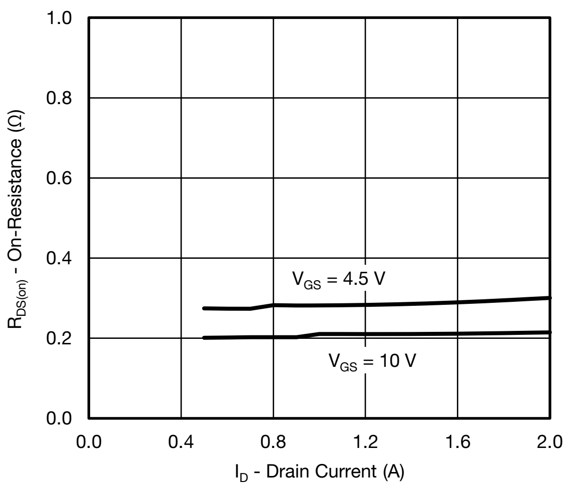
N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



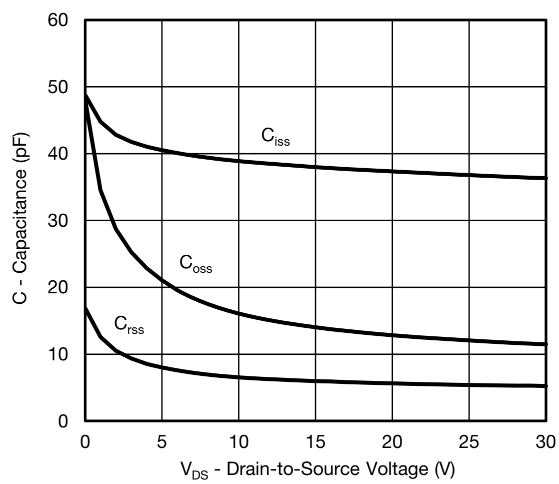
Output Characteristics



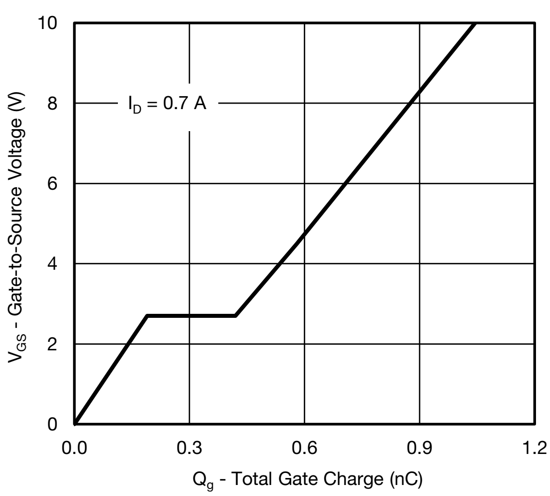
Transfer Characteristics



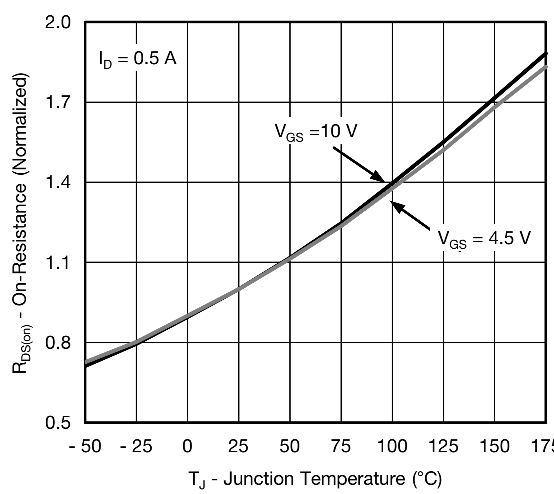
On-Resistance vs. Drain Current



Capacitance

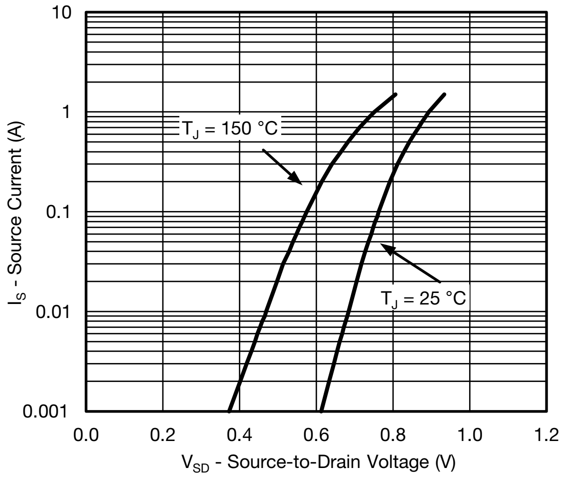


Gate Charge

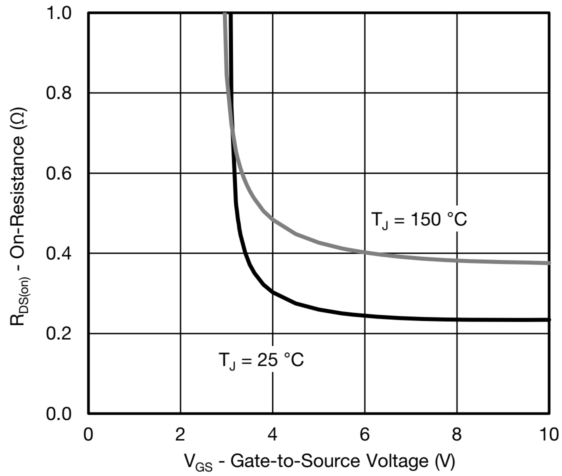


On-Resistance vs. Junction Temperature

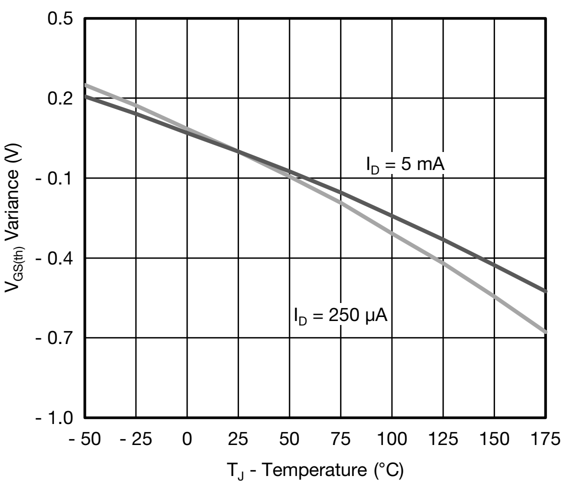
N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



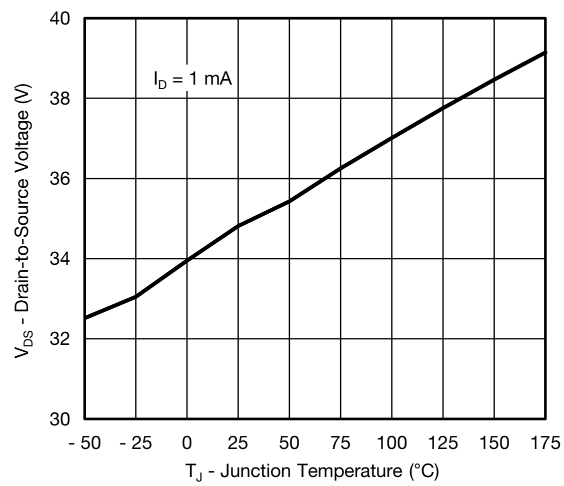
Source Drain Diode Forward Voltage



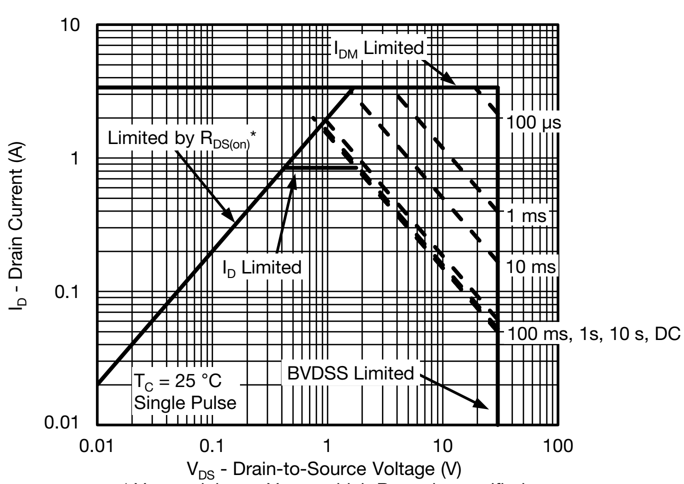
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



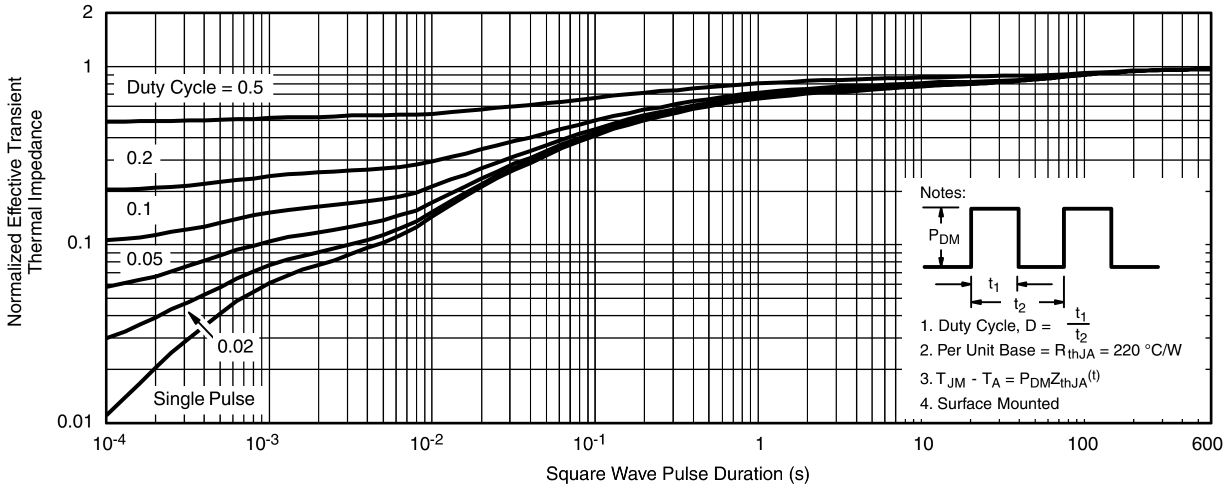
Drain Source Breakdown vs. Junction Temperature



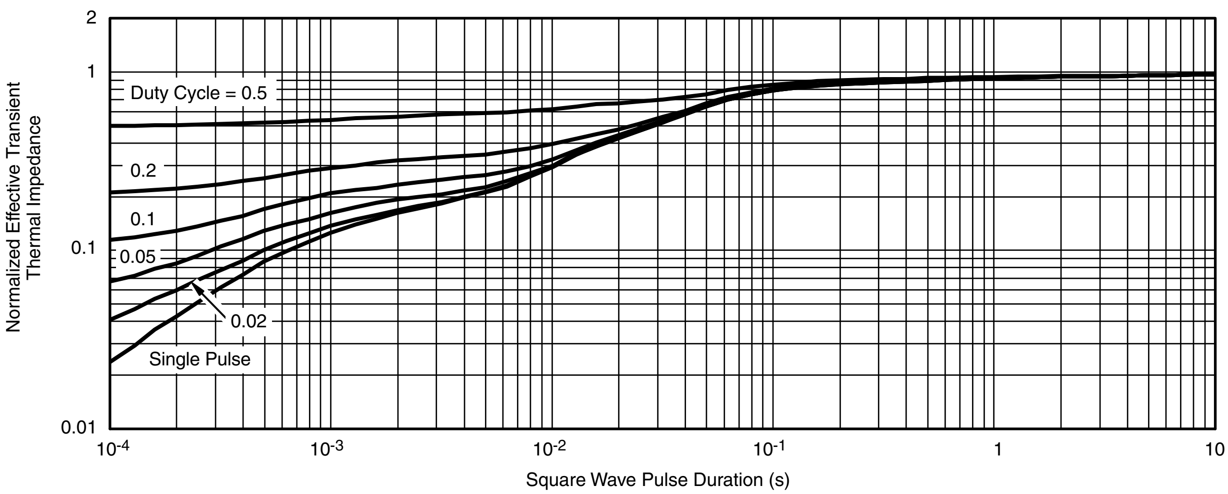
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

N-CHANNEL THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



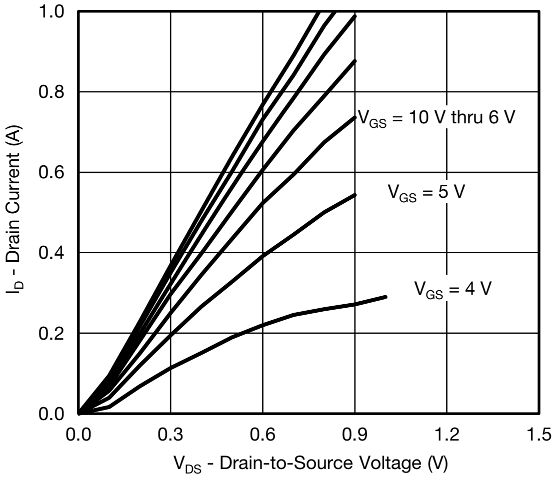
Normalized Thermal Transient Impedance, Junction-to-Foot

Note

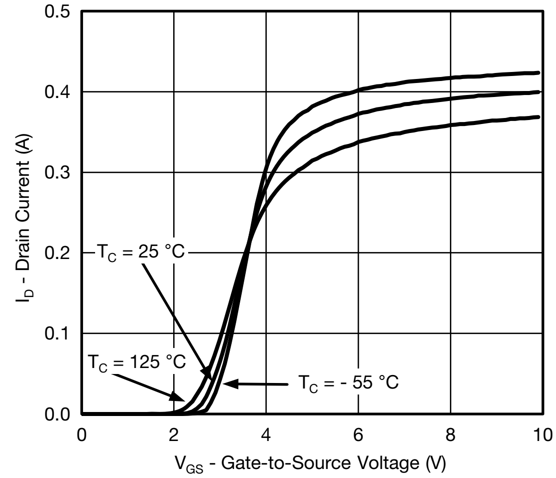
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

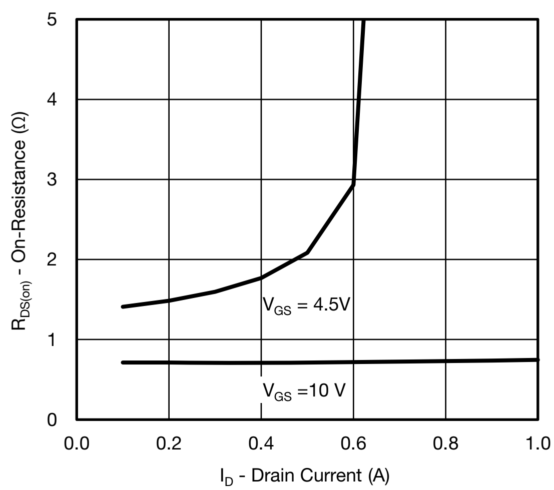
P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



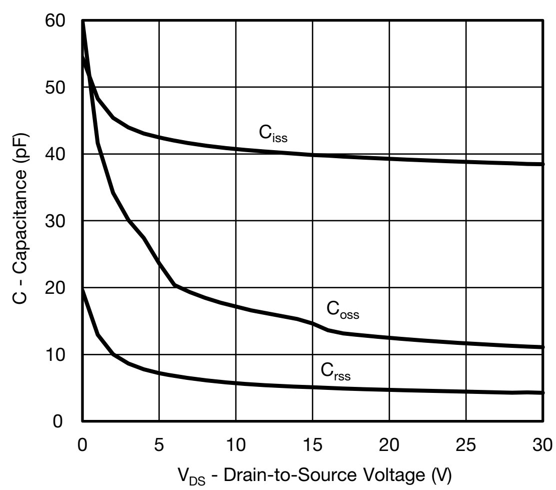
Output Characteristics



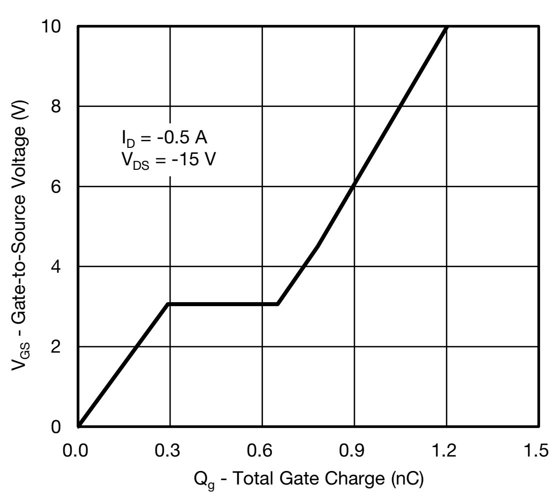
Transfer Characteristics



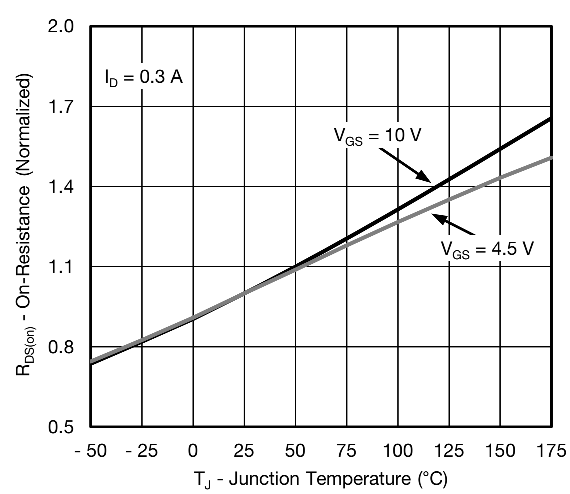
On-Resistance vs. Drain Current



Capacitance

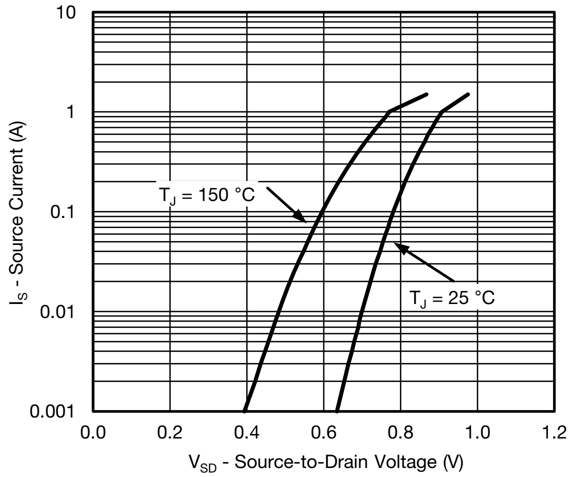


Gate Charge

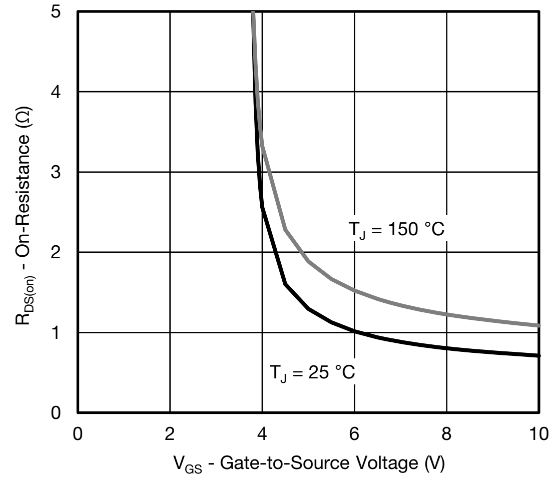


On-Resistance vs. Junction Temperature

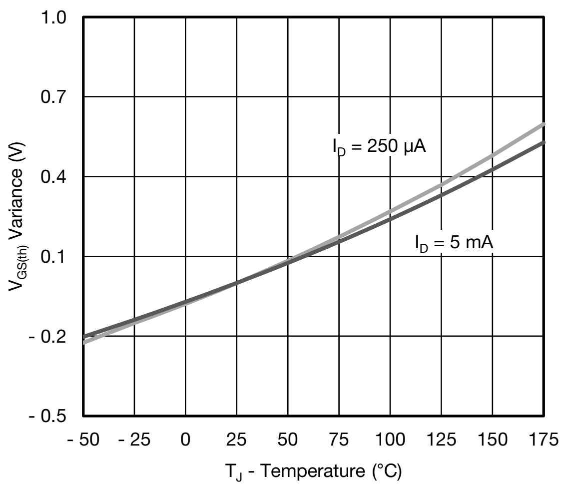
P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



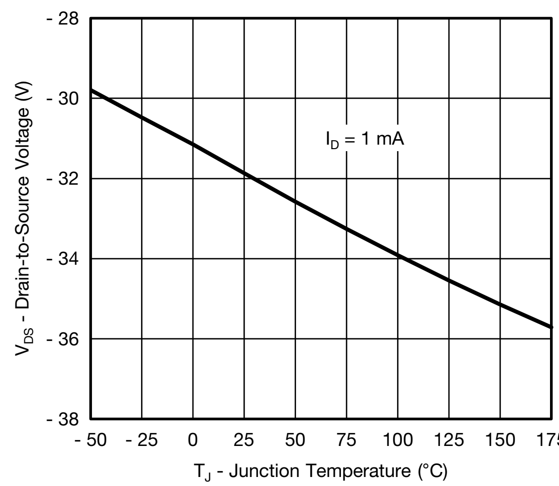
Source Drain Diode Forward Voltage



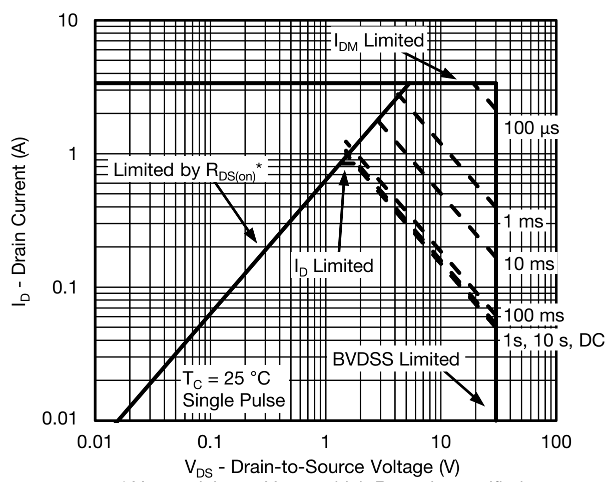
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



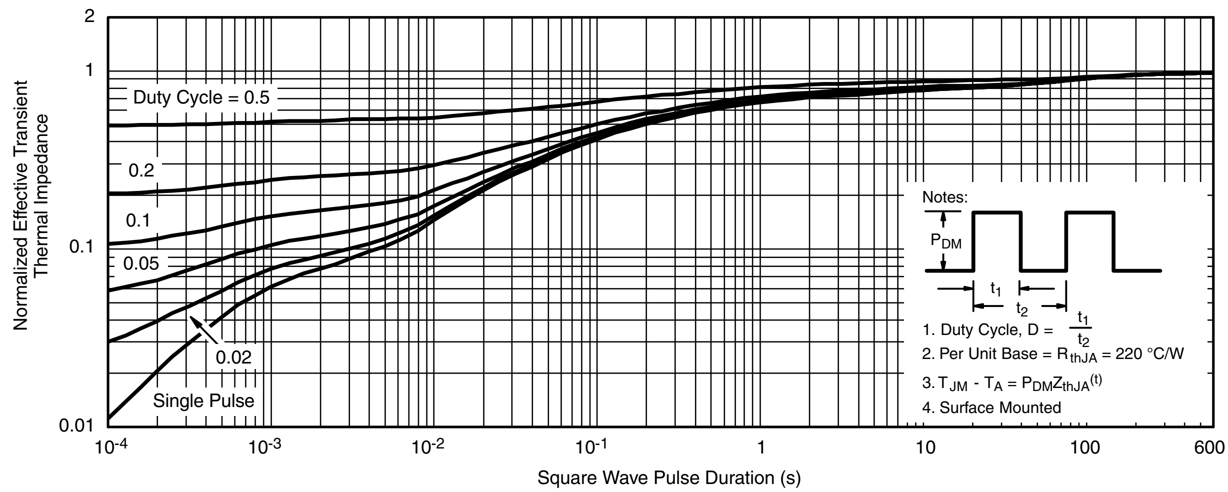
Drain Source Breakdown vs. Junction Temperature



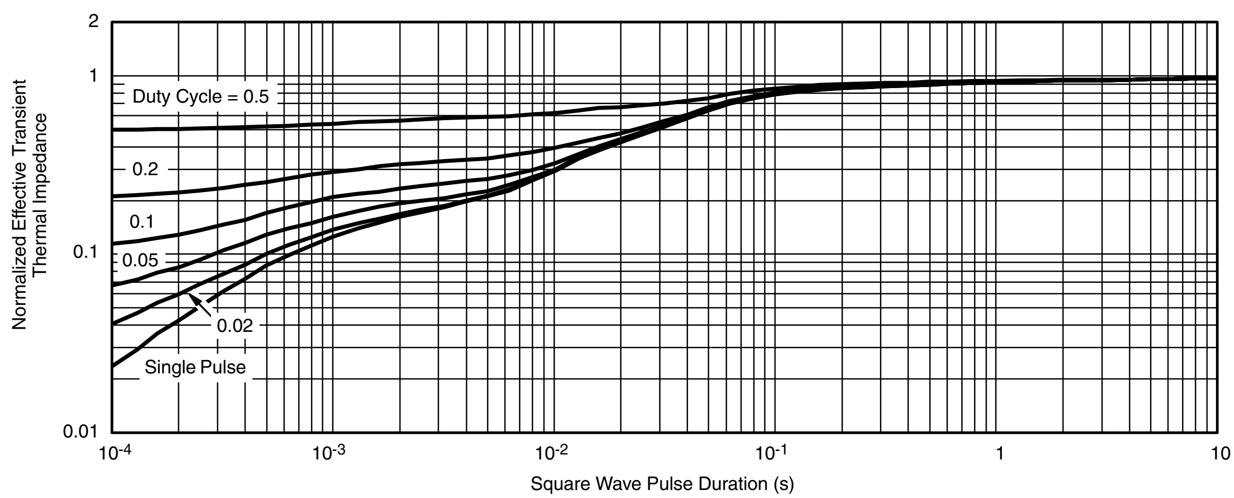
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

P-CHANNEL THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

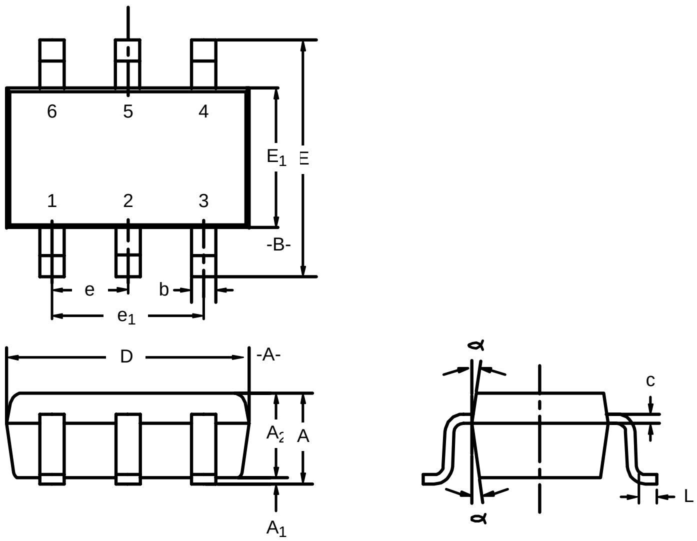
Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62993.

SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

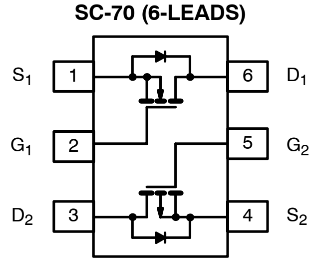
INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.

SOT-363
SC-70 (6-LEADS)



Top View

FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.

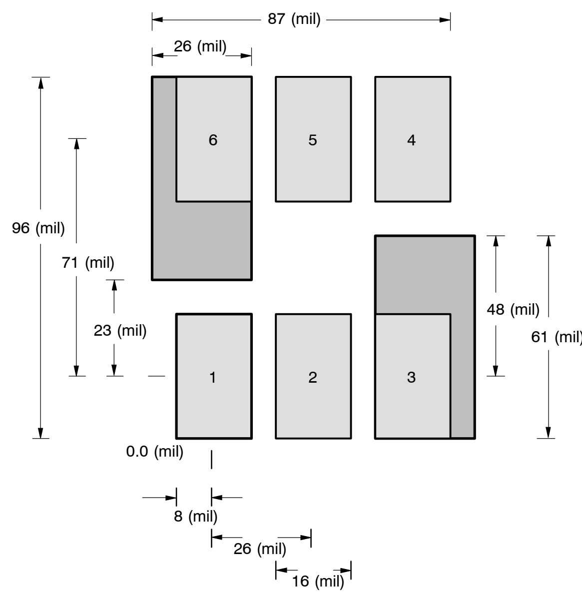


FIGURE 2. SC-70 (6 leads) Dual

EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch^2 PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

Front of Board SC70-6 | Back of Board SC70-6

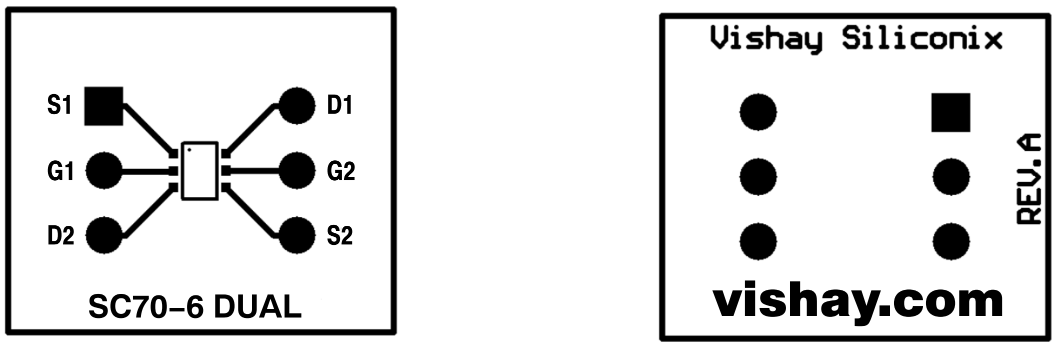


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the “foot” is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

Power Dissipation

The typical $R\theta_{JA}$ for the dual-channel 6-pin SC-70 with a copper leadframe is 224°C/W steady-state, compared to 413°C/W for the Alloy 42 version. All figures are based on the 1-inch^2 FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

Alloy 42 Leadframe

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{413^oC/W}$	$P_D = \frac{150^oC - 60^oC}{413^oC/W}$
$P_D =$ 303 mW	$P_D =$ 218 mW

COOPER LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{224^oC/W}$	$P_D = \frac{150^oC - 60^oC}{224^oC/W}$
$P_D =$ 558 mW	$P_D =$ 402 mW

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of $R\theta_{JA}$ for the dual 6-pin SC-70 with varying leadframes are as follows:

LITTLE FOOT 6-PIN SC-70		
	Alloy 42	Copper
1) Minimum recommended pad pattern on the EVB board (see Figure 3).	518°C/W	344°C/W
2) Industry standard 1-inch^2 PCB with maximum copper both sides.	413°C/W	224°C/W

The results indicate that designers can reduce thermal resistance (θJA) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch^2. PCB area.

The Dual copper leadframe versions have the following suffix:

Dual:	Si19xxEDH
Compl.:	Si15xxEDH

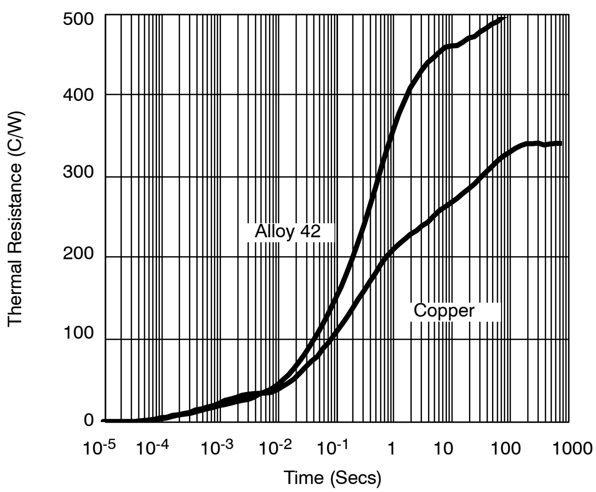


FIGURE 4. Dual SC70-6 Thermal Performance on EVB

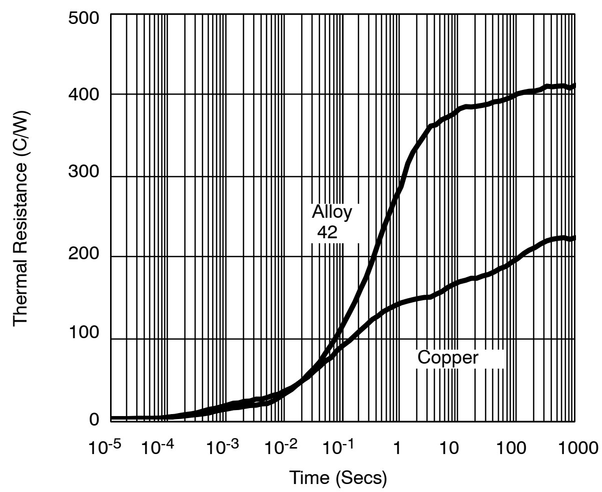
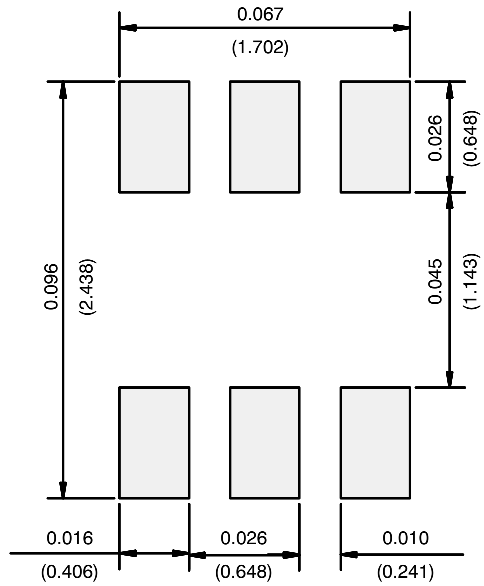


FIGURE 5. Dual SC70-6 Comparison on 1-inch^2 PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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