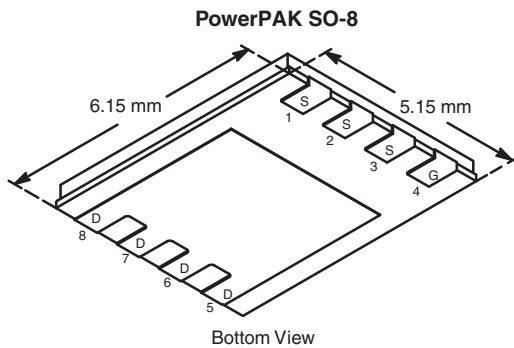




N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, g}	Q_g (Typ.)
25	0.0094 at $V_{GS} = 10$ V	20	8 nC
	0.012 at $V_{GS} = 4.5$ V	20	



Ordering Information: SiR874DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

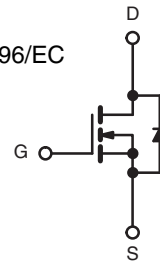
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Gen III Power MOSFET
- Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/96/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook CPU Core
- High-Side Switch
- Game Machine DC/DC High-Side
- Server DC/DC High-Side



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	25	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	20 ^g	A
		$T_C = 70$ °C	20 ^g	
		$T_A = 25$ °C	15 ^{b, c}	
		$T_A = 70$ °C	12 ^{b, c}	
Pulsed Drain Current	I_{DM}	50	A	
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C		20 ^g
		$T_A = 25$ °C	3.2 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	20	mJ	
Avalanche Energy	E_{AS}	20		
Maximum Power Dissipation	P_D	$T_C = 25$ °C	29.8	W
		$T_C = 70$ °C	19.0	
		$T_A = 25$ °C	3.9 ^{b, c}	
		$T_A = 70$ °C	2.5 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	27	32	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	3.5	4.2	

Notes:

a. Base on $T_C = 25$ °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 70 °C/W.

g. Packaged Limited.

SiR874DP

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		34		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-4.7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.1		2.2	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.0075	0.0094	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$		0.010	0.012	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		30		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		985		pF
Output Capacitance	C_{oss}			205		
Reverse Transfer Capacitance	C_{rss}			76		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		18	27	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		8	12	
Gate-Source Charge	Q_{gs}		2.4			
Gate-Drain Charge	Q_{gd}		2.3			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.3	1.3	2.6	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		14	25	ns
Rise Time	t_r			12	24	
Turn-Off Delay Time	$t_{d(off)}$			19	35	
Fall Time	t_f			9	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		8	16	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			16	30	
Fall Time	t_f			9	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			20	A
Pulse Diode Forward Current ^a	I_{SM}				50	
Body Diode Voltage	V_{SD}	$I_S = 3\text{ A}$		0.76	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		14	28	ns
Body Diode Reverse Recovery Charge	Q_{rr}			5	10	nC
Reverse Recovery Fall Time	t_a			8		ns
Reverse Recovery Rise Time	t_b			6		

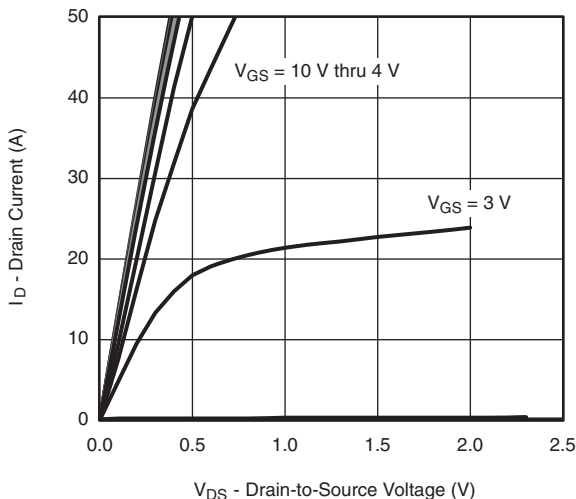
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

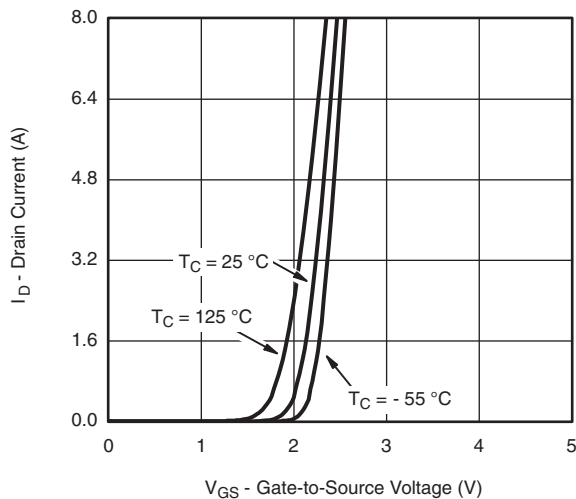
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



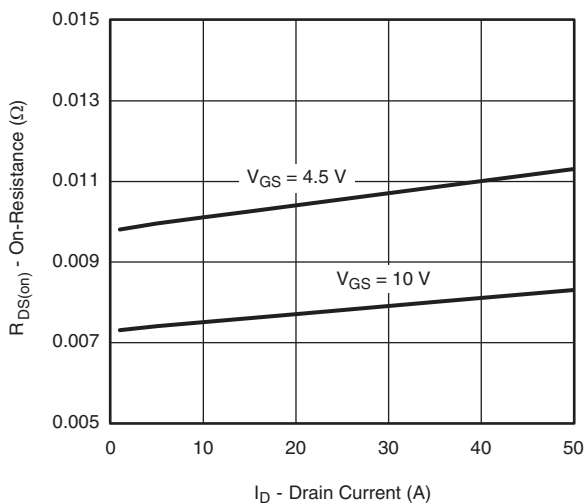
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



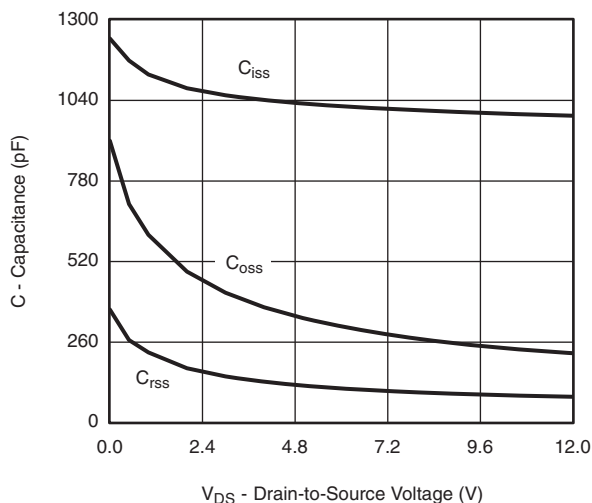
Output Characteristics



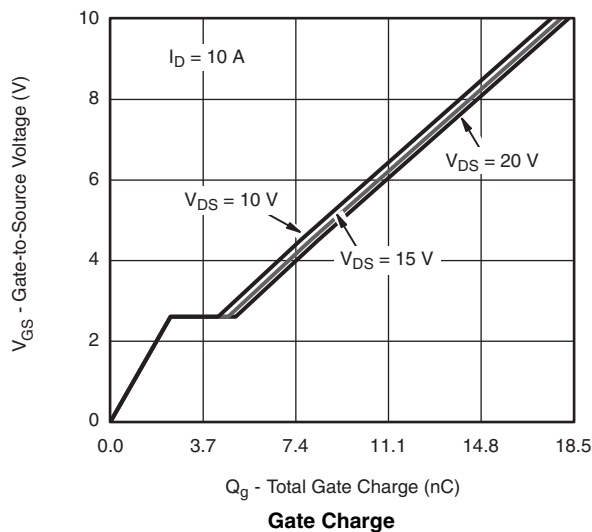
Transfer Characteristics



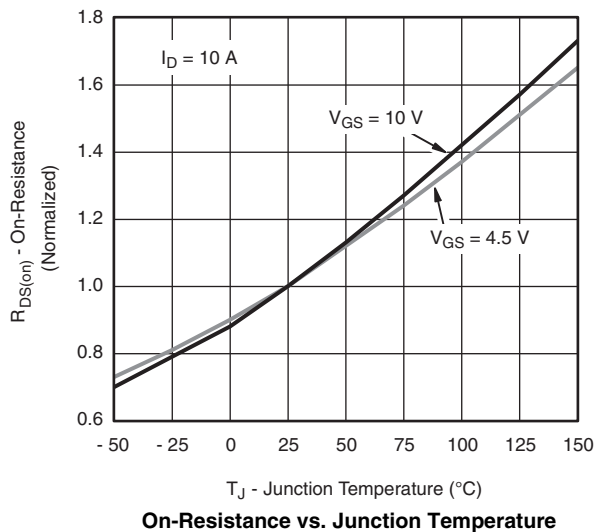
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



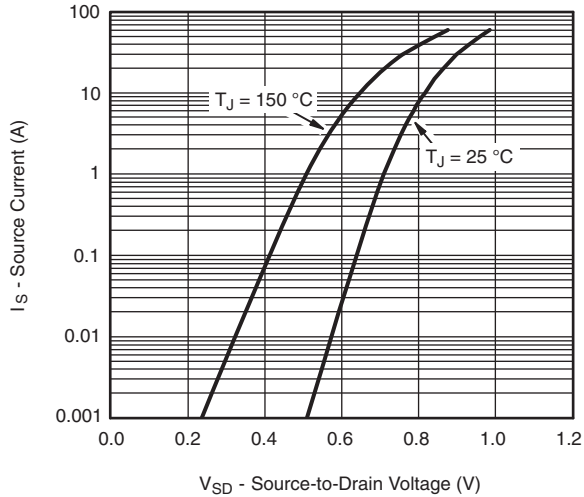
On-Resistance vs. Junction Temperature

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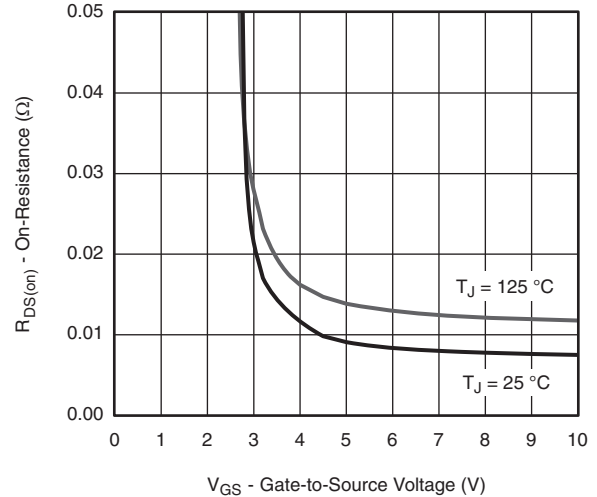
Vishay Siliconix



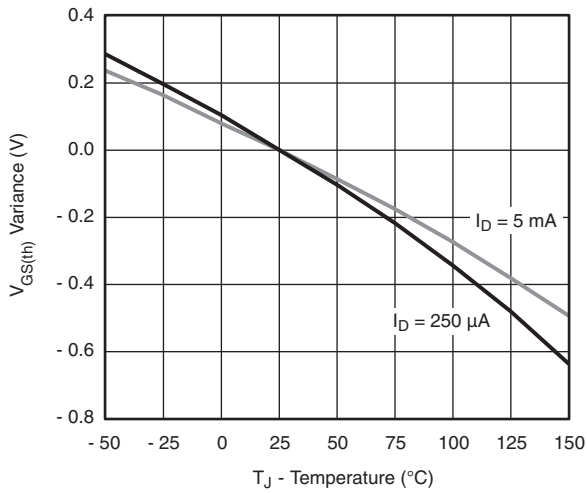
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



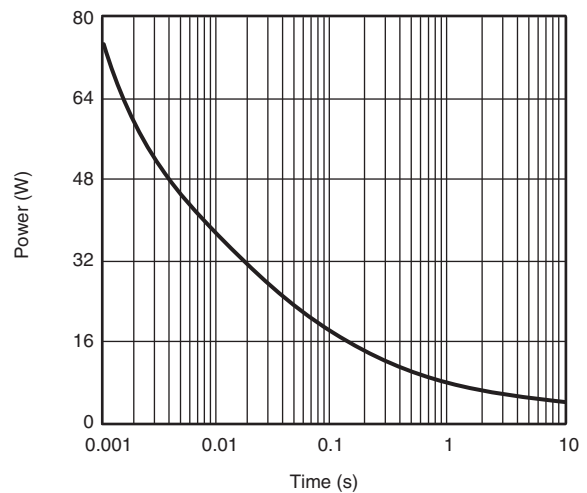
Source-Drain Diode Forward Voltage



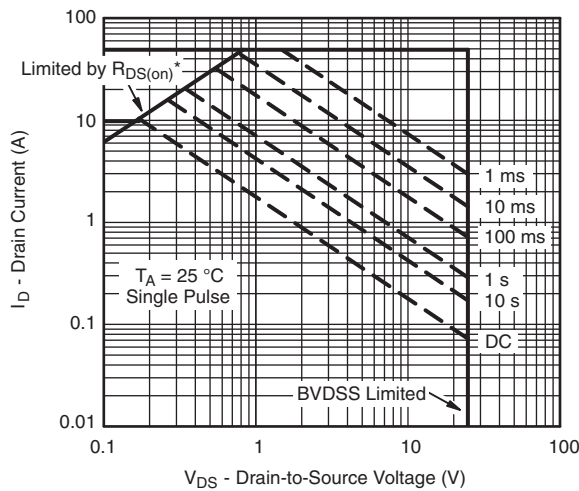
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

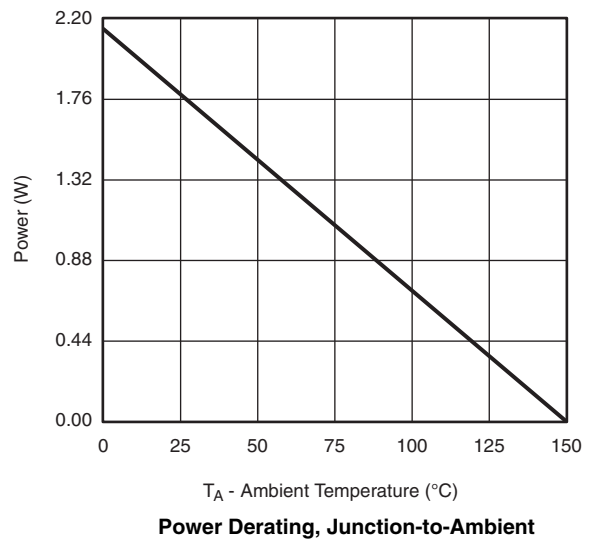
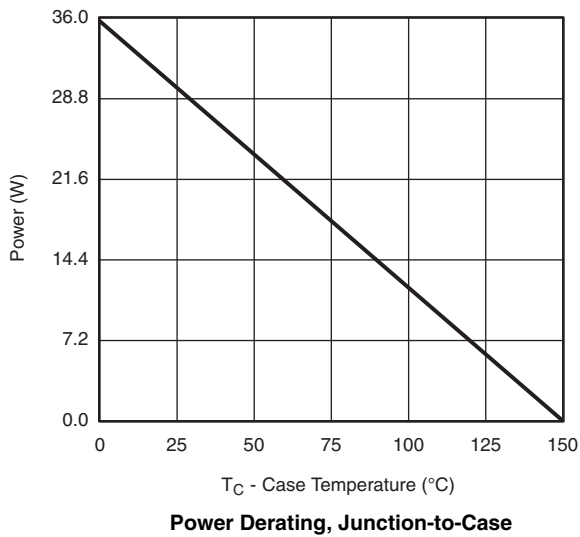
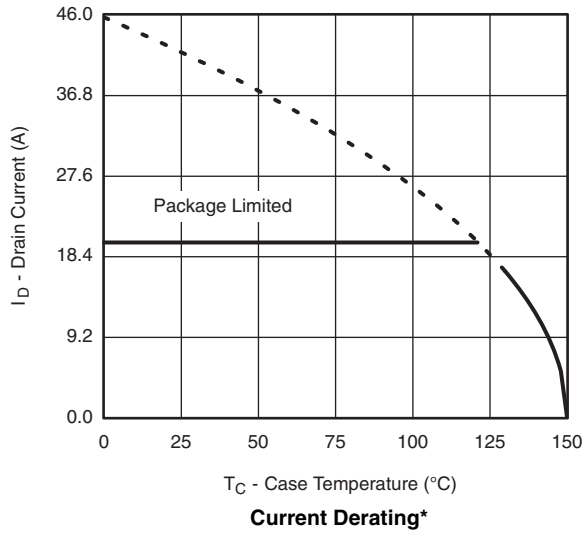


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



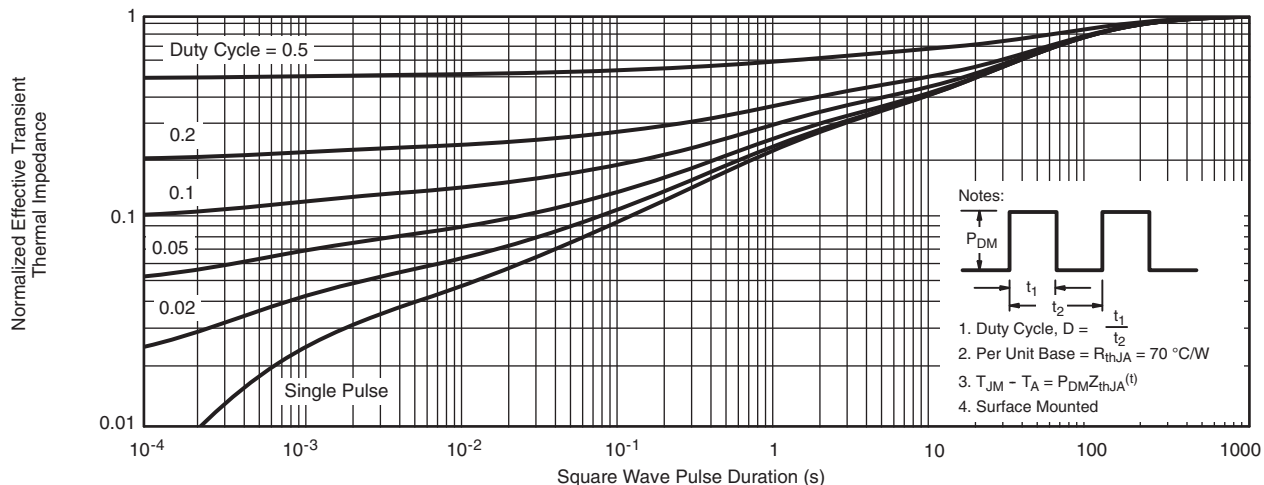
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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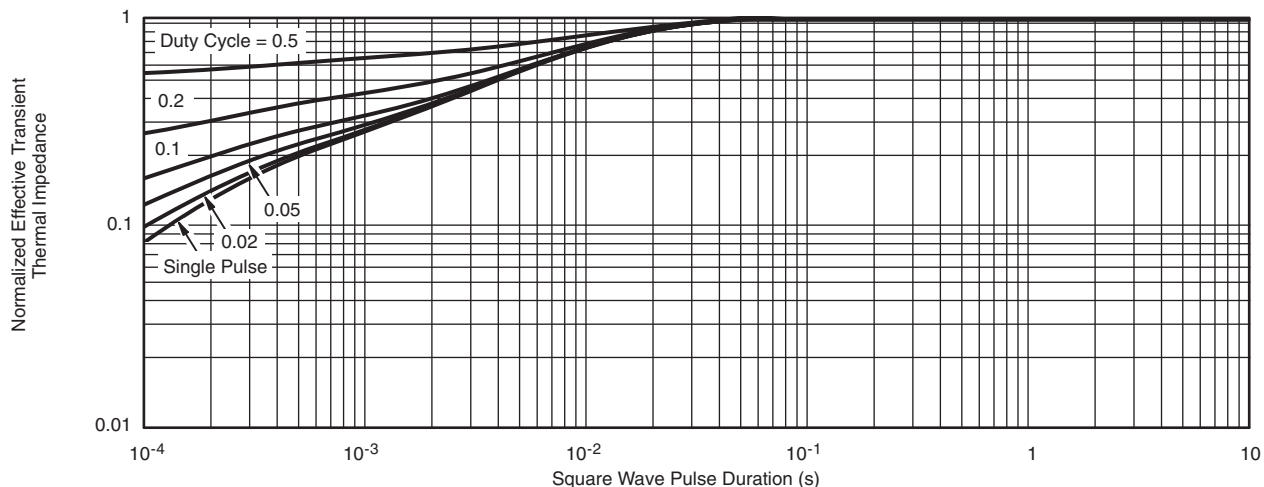
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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