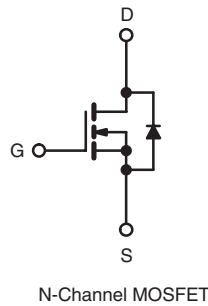
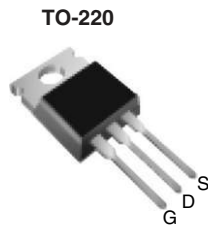


## Power MOSFET

| PRODUCT SUMMARY           |                 |      |
|---------------------------|-----------------|------|
| $V_{DS}$ (V)              | 300             |      |
| $R_{DS(on)}$ ( $\Omega$ ) | $V_{GS} = 10$ V | 0.75 |
| $Q_g$ (Max.) (nC)         | 17              |      |
| $Q_{gs}$ (nC)             | 4.8             |      |
| $Q_{gd}$ (nC)             | 7.6             |      |
| Configuration             | Single          |      |



### FEATURES

- Reduced Gate Drive Requirement
- Enhanced 30 V  $V_{GS}$  Rating
- Reduced  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Lead (Pb)-free Available



RoHS\*  
COMPLIANT

### DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional Power MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge Power MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristics of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

| ORDERING INFORMATION |                             |
|----------------------|-----------------------------|
| Package              | TO-220                      |
| Lead (Pb)-free       | IRF737LCPbF<br>SiHF737LC-E3 |
| SnPb                 | IRF737LC<br>SiHF737LC       |

| ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted |                  |                  |      |          |
|--|------------------|------------------|------|----------|
| PARAMETER  | SYMBOL           | LIMIT            | UNIT |          |
| Drain-Source Voltage   | $V_{DS}$         | 300              | V    |          |
| Gate-Source Voltage  | $V_{GS}$         | $\pm 30$         |      |          |
| Continuous Drain Current                                       | $V_{GS}$ at 10 V | $T_C = 25$ °C    | 6.1  | A        |
|  |                  | $T_C = 100$ °C   | 3.9  |          |
| Pulsed Drain Current <sup>a</sup>                              | $I_{DM}$         | 24               |      |          |
| Linear Derating Factor   |                  | 0.59             | W/°C |          |
| Single Pulse Avalanche Energy <sup>b</sup>                     | $E_{AS}$         | 120              | mJ   |          |
| Avalanche Current <sup>a</sup>                                 | $I_{AR}$         | 6.1              | A    |          |
| Repetitive Avalanche Energy <sup>a</sup>                       | $E_{AR}$         | 7.4              | mJ   |          |
| Maximum Power Dissipation                                      | $T_C = 25$ °C    | $P_D$            | 74   | W        |
| Peak Diode Recovery $dV/dt^c$                                  |                  | $dV/dt$          | 3.4  | V/ns     |
| Operating Junction and Storage Temperature Range               | $T_J, T_{stg}$   | - 55 to + 150    | °C   |          |
| Soldering Recommendations (Peak Temperature)                   | for 10 s         | 300 <sup>d</sup> |      |          |
| Mounting Torque  | 6-32 or M3 screw |                  | 10   | lbf · in |
|  |                  |                  | 1.1  | N · m    |

#### Notes

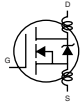

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C,  $L = 5.7$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 6.1$  A (see fig. 12).
- $I_{SD} \leq 6.1$  A,  $dI/dt \leq 270$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS          |            |      |      |      |
|-------------------------------------|------------|------|------|------|
| PARAMETER                           | SYMBOL     | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient         | $R_{thJA}$ | -    | 62   | °C/W |
| Case-to-Sink, Flat, Greased Surface | $R_{thCS}$ | 0.50 | -    |      |
| Maximum Junction-to-Case (Drain)    | $R_{thJC}$ | -    | 1.7  |      |

**Note**

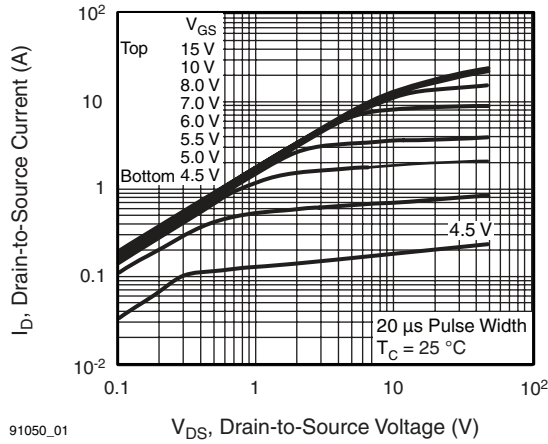
a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS $T_J = 25^\circ\text{C}$ , unless otherwise noted |                     |  |  |      |       |                         |               |
|--|---------------------|--|--|------|-------|-------------------------|---------------|
| PARAMETER  | SYMBOL              | TEST CONDITIONS  |  | MIN. | TYP.  | MAX. UNIT               |               |
| <b>Static</b>  |                     |  |  |      |       |                         |               |
| Drain-Source Breakdown Voltage                                   | $V_{DS}$            | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$  |  | 300  | -     | - V                     |               |
| $V_{DS}$ Temperature Coefficient                                 | $\Delta V_{DS}/T_J$ | Reference to $25^\circ\text{C}$ , $I_D = 1\text{ mA}$  |  | -    | 0.391 | - $^\circ\text{C}^{-1}$ |               |
| Gate-Source Threshold Voltage                                    | $V_{GS(th)}$        | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$  |  | 2.0  | -     | 4.0 V                   |               |
| Gate-Source Leakage  | $I_{GSS}$           | $V_{GS} = \pm 20\text{ V}$   |  | -    | -     | $\pm 100\text{ nA}$     |               |
| Zero Gate Voltage Drain Current                                  | $I_{DSS}$           | $V_{DS} = 300\text{ V}, V_{GS} = 0\text{ V}$   |  | -    | -     | 25 $\mu\text{A}$        |               |
|  |                     | $V_{DS} = 240\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$  |  | -    | -     | 250 $\mu\text{A}$       |               |
| Drain-Source On-State Resistance                                 | $R_{DS(on)}$        | $V_{GS} = 10\text{ V}$   | $I_D = 3.7\text{ A}^b$   | -    | -     | 0.75 $\Omega$           |               |
| Forward Transconductance   | $g_{fs}$            | $V_{DS} = 50\text{ V}, I_D = 3.7\text{ A}^b$   |  | 2.7  | -     | - S                     |               |
| <b>Dynamic</b>   |                     |  |  |      |       |                         |               |
| Input Capacitance  | $C_{iss}$           | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5   |  | -    | 430   | -                       | pF            |
| Output Capacitance   | $C_{oss}$           |  |  | -    | 120   | -                       |               |
| Reverse Transfer Capacitance                                     | $C_{rss}$           |  |  | -    | 9.2   | -                       |               |
| Total Gate Charge  | $Q_g$               | $V_{GS} = 10\text{ V}$   | $I_D = 6.1\text{ A}, V_{DS} = 240\text{ V}$ , see fig. 6 and 13 <sup>b</sup> | -    | -     | 17                      | nC            |
| Gate-Source Charge   | $Q_{gs}$            |  |  | -    | -     | 4.8                     |               |
| Gate-Drain Charge  | $Q_{gd}$            |  |  | -    | -     | 7.6                     |               |
| Turn-On Delay Time   | $t_{d(on)}$         | $V_{DD} = 150\text{ V}, I_D = 6.1\text{ A}, R_G = 12\ \Omega, R_D = 24\ \Omega$ , see fig. 10 <sup>b</sup>   |  | -    | 6.6   | -                       | ns            |
| Rise Time  | $t_r$               |  |  | -    | 21    | -                       |               |
| Turn-Off Delay Time  | $t_{d(off)}$        |  |  | -    | 13    | -                       |               |
| Fall Time  | $t_f$               |  |  | -    | 12    | -                       |               |
| Internal Drain Inductance  | $L_D$               | Between lead, 6 mm (0.25") from package and center of die contact  |  | -    | 4.5   | -                       | nH            |
| Internal Source Inductance                                       | $L_S$               |  |  | -    | 7.5   | -                       |               |
| <b>Drain-Source Body Diode Characteristics</b>                   |                     |  |  |      |       |                         |               |
| Continuous Source-Drain Diode Current                            | $I_S$               | MOSFET symbol showing the integral reverse p-n junction diode      |  | -    | -     | 6.1                     | A             |
| Pulsed Diode Forward Current <sup>a</sup>                        | $I_{SM}$            |  |  | -    | -     | 24                      |               |
| Body Diode Voltage   | $V_{SD}$            | $T_J = 25^\circ\text{C}, I_S = 6.1\text{ A}, V_{GS} = 0\text{ V}^b$  |  | -    | -     | 1.6                     | V             |
| Body Diode Reverse Recovery Time                                 | $t_{rr}$            | $T_J = 25^\circ\text{C}, I_F = 6.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$   |  | -    | 320   | 490                     | ns            |
| Body Diode Reverse Recovery Charge                               | $Q_{rr}$            |  |  | -    | 1.5   | 2.2                     | $\mu\text{C}$ |

**Notes**

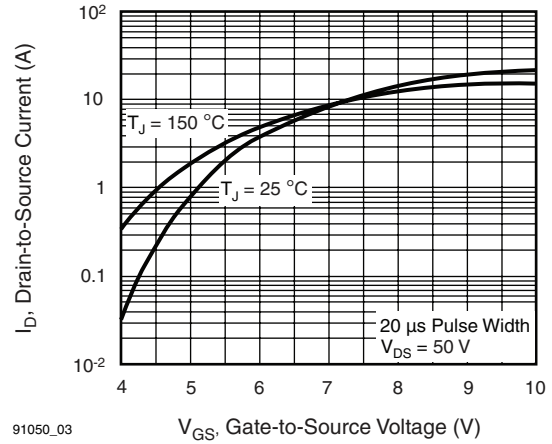
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



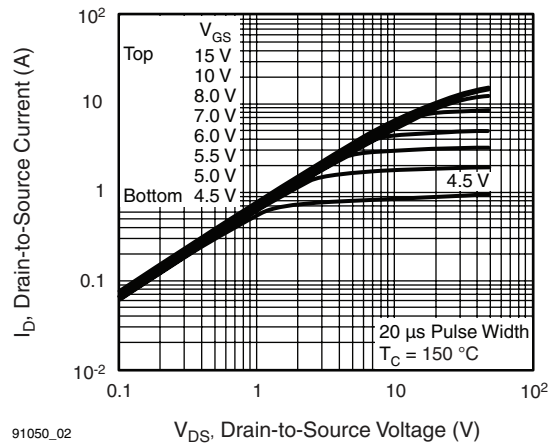
91050\_01

**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ °C}$**



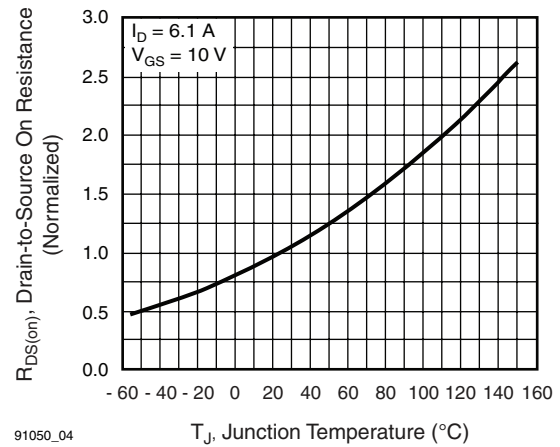
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**Fig. 3 - Typical Transfer Characteristics**



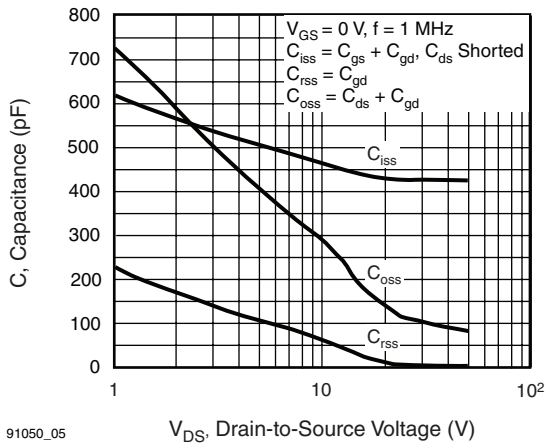
91050\_02

**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ °C}$**



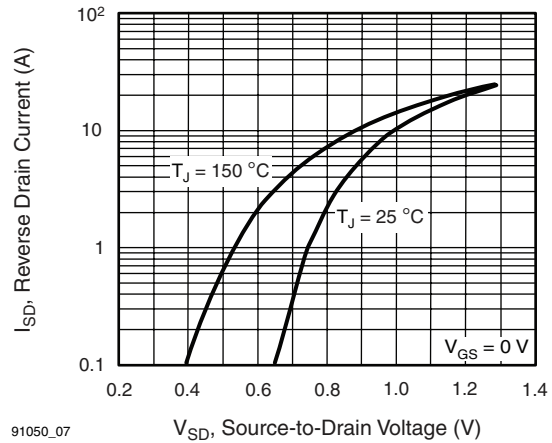
91050\_04

**Fig. 4 - Normalized On-Resistance vs. Temperature**



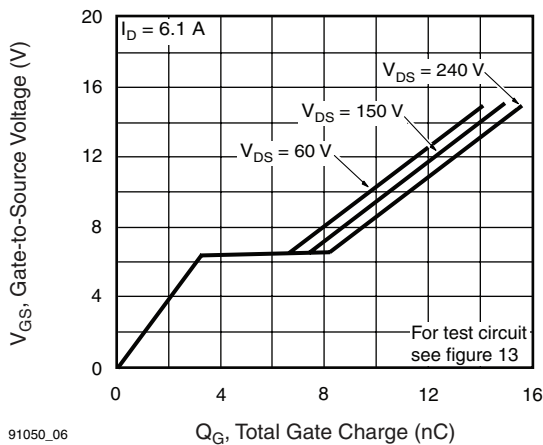
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



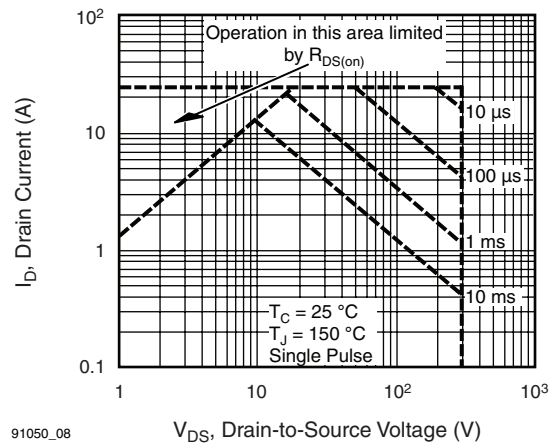
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



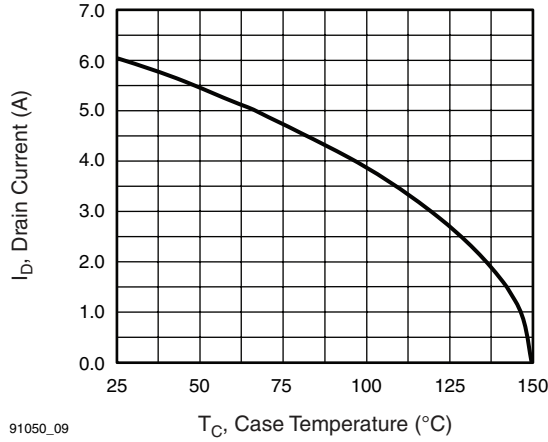
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



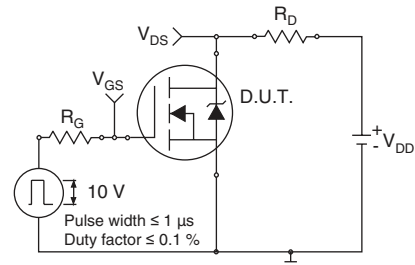
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Fig. 8 - Maximum Safe Operating Area

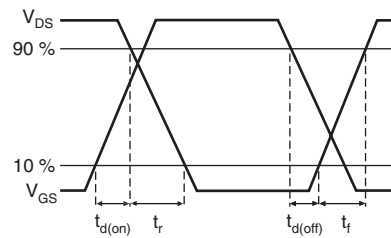


91050\_09

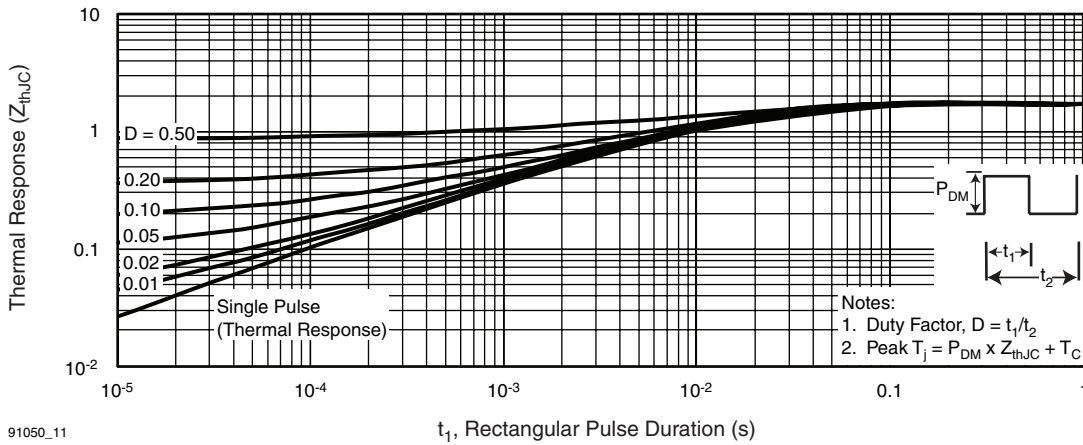
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**

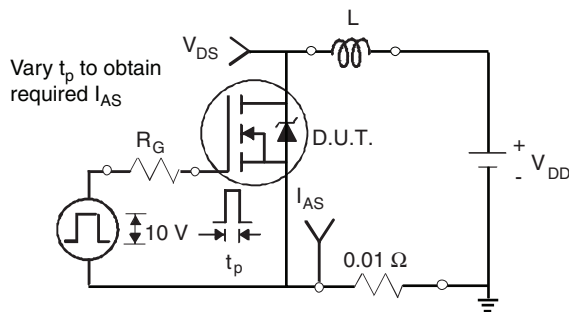


**Fig. 10b - Switching Time Waveforms**

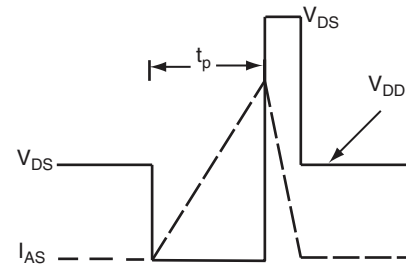


91050\_11

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

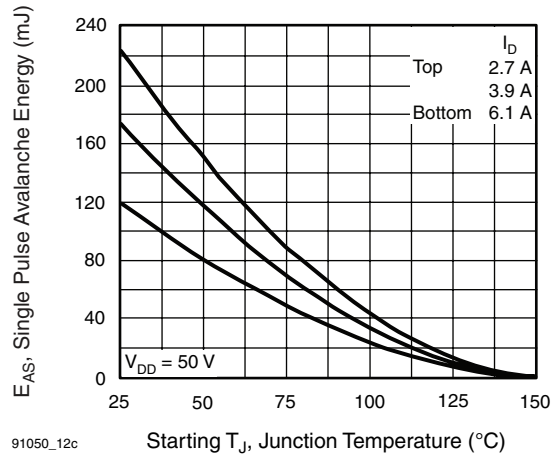


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

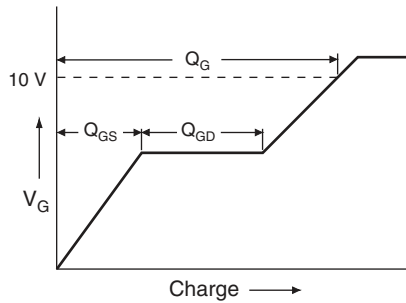


Fig. 13a - Basic Gate Charge Waveform

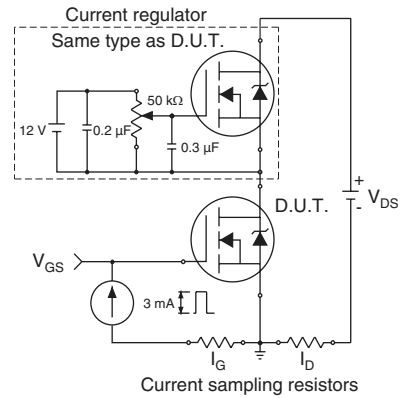


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



Fig. 14 - For N-Channel

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