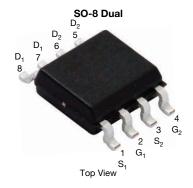
## **SQ4284EY**

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**Vishay Siliconix** 

## Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET



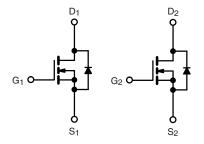
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0135			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.0148			
I <sub>D</sub> (A)	8			
Configuration	Dual			

#### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- AEC-Q101 qualified
- 100 %  $R_q$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



ROHS COMPLIANT HALOGEN FREE



N-Channel MOSFET N-Channel MOSFET

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	SQ4284EY (for detailed order number please see www.vishay.com/doc?79771)

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V <sub>DS</sub>	40	N		
Gate-source voltage		V <sub>GS</sub>	± 20	V		
Continuous drain current	T <sub>C</sub> = 25 °C <sup>a</sup>	1	8			
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	7.4			
Continuous source current (diode conduction)		I <sub>S</sub>	3.5	А		
Pulsed drain current <sup>a</sup>		I <sub>DM</sub>	32			
Single pulse avalanche current		I <sub>AS</sub>	48			
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	115	mJ		
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	D	3.9	W		
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	1.3	vv		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB Mount <sup>b</sup>	R <sub>thJA</sub>	120	°C/W	
Junction-to-foot (drain)		R <sub>thJF</sub>	38	0/10	

#### Notes

a. Pulse test; pulse width  $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%$ 

b. When mounted on 1" square PCB (FR-4 material)

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**SQ4284EY** 

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		1		<u> </u>	1	<u> </u>	1
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$		40	-	-	v
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$		2.0	2.5	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V	-	-	1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	25	-	-	Α
		$V_{GS} = 10 V$	I <sub>D</sub> = 7 A	-	0.0112	0.0135	Ω
Ducia composito de chata una interna a		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 7 A, T <sub>J</sub> = 125 °C	-	-	0.0198	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 7 A, T <sub>J</sub> = 175 °C	-	-	0.0235	
		$V_{GS} = 4.5 V$	I <sub>D</sub> = 5 A	-	0.0123	0.0148	
Forward transconductance b	g <sub>fs</sub>	V <sub>DS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7 A		30	-	S
Dynamic <sup>b</sup>					•		
Input capacitance	C <sub>iss</sub>		V <sub>GS</sub> = 0 V V <sub>DS</sub> = 25 V, f = 1 MHz	-	1760	2200	pF
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$		-	252	315	
Reverse transfer capacitance	C <sub>rss</sub>	1		-	93	116	
Total gate charge <sup>c</sup>	Qg			-	30	45	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	-	5.5	-	nC
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>	1		-	5	-	1
Gate resistance	Rg	f = 1 MHz		2.2	4.53	6.8	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	10	15	
Rise Time <sup>c</sup>	tr	$\label{eq:VDD} \begin{array}{l} V_{\text{DD}} = 20 \ \text{V}, \ R_{\text{L}} = 4 \ \Omega \\ I_{\text{D}} \cong 5 \ \text{A}, \ V_{\text{GEN}} = 10 \ \text{V}, \ R_{\text{g}} = 1 \ \Omega \end{array}$		-	40	60	- ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	32	48	
Fall time <sup>c</sup>	t <sub>f</sub>			-	11	17	
Source-Drain Diode Ratings and Char	acteristics <sup>b</sup>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	32	Α
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 7 A, V <sub>GS</sub> = 0 V		-	0.76	1.2	V

Notes

a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing

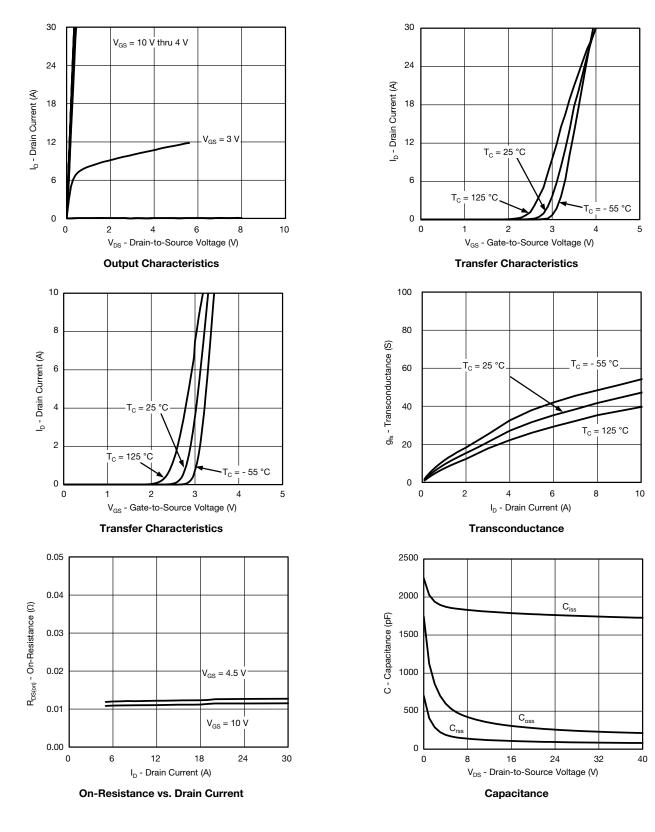
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

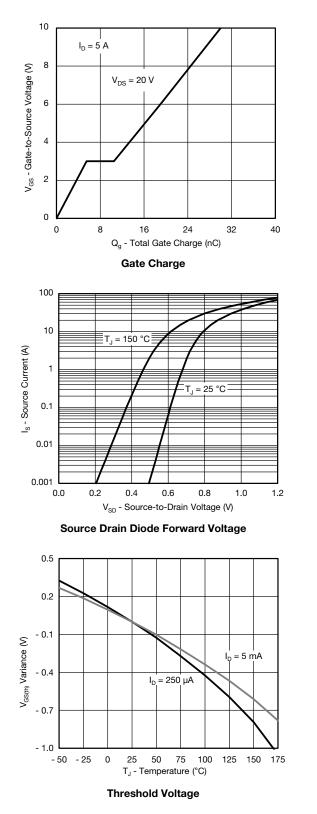


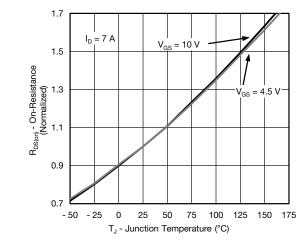
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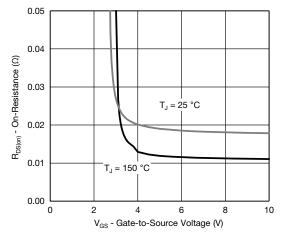


### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

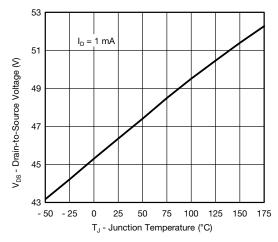




**On-Resistance vs. Junction Temperature** 







Drain Source Breakdown vs. Junction Temperature

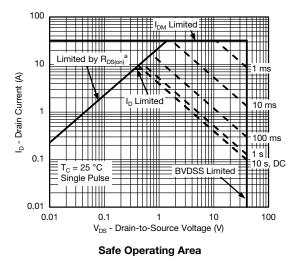
S21-0375-Rev. E, 23-Apr-2021

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## **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

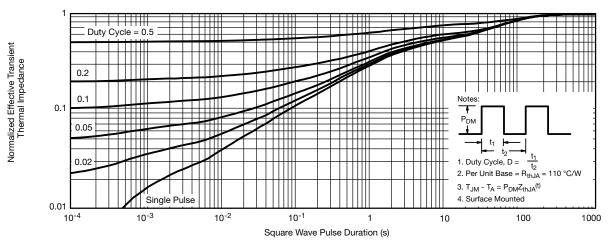


#### Note

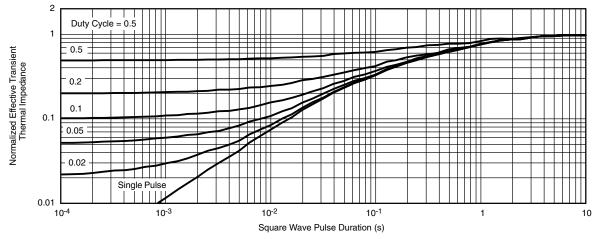
a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(\text{on})}$  is specified



### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67334.

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# Package Information

Vishay Siliconix

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

# **Application Note 826**

Vishay Siliconix



**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

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