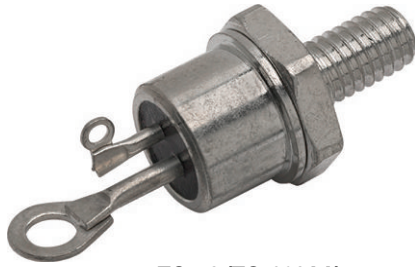




## Phase Control Thyristor RMS SCRs, 25 A, 35 A



TO-48 (TO-208AA)

### FEATURES

- General purpose stud mounted
- Broad forward and reverse voltage range - through 1200 V
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS COMPLIANT

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	16 A, 22 A
$I_{T(RMS)}$	25 A, 35 A
$V_{DRM}/V_{RRM}$	25 V, 50 V, 100 V, 150 V, 200 V, 250 V, 300 V, 400 V, 500 V, 600 V, 700 V, 800 V, 1000 V 1200 V
$V_{TM}$	2.3 V
$I_{GT}$	60 mA
$T_J$	-40 °C to +125 °C
Package	TO-48 (TO-208AA)
Circuit configuration	Single SCR

MAJOR RATINGS AND CHARACTERISTICS				
PARAMETER	TEST CONDITIONS	VALUES 2N681-92	VALUES 2N5205-07	UNITS
$I_{T(AV)}$		16 <sup>(1)</sup>	22 <sup>(1)</sup>	A
	$T_C$	-65 to +65 <sup>(1)</sup>	-40 to +40	°C
$I_{T(RMS)}$		25	35	A
$I_{TSM}$	50 Hz	145	285	A
	60 Hz	150 <sup>(1)</sup>	300 <sup>(1)</sup>	
$I^2t$	50 Hz	103	410	A <sup>2</sup> s
	60 Hz	94	375	
$I_{GT}$		40	40	mA
$dV/dt$		-	100 <sup>(1)</sup>	V/ $\mu$ s
$dl/dt$		75 to 100	100	A/ $\mu$ s
$V_{DRM}$	Range	25 to 800	600 to 1200	V
$V_{RRM}$	Range	25 to 800	600 to 1200	V
$T_J$		-65 to +125 <sup>(1)</sup>	-40 to +125 <sup>(1)</sup>	°C

**Note**

<sup>(1)</sup> JEDEC® registered value



## ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS (APPLIED GATE VOLTAGE ZERO OR NEGATIVE)			
TYPE NUMBER	$V_{RRM}/V_{DRM}$ , MAXIMUM REPETITIVE PEAK REVERSE AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE ( $t_p < 5$ ms) V	$T_J$
VS-2N681	25	35	-65 °C to +125 °C
VS-2N682	50	75	
VS-2N683	100	150	
VS-2N684	150	200	
VS-2N685	200	300	
VS-2N686	250	350	
VS-2N687	300	400	
VS-2N688	400	500	
VS-2N689	500	600	
VS-2N690	600	720	
VS-2N691	700	840	
VS-2N692	800	960	
VS-2N5205	800	960	-40 °C to +125 °C
VS-2N5206	1000	1200	
VS-2N5207	1200	1440	

## Note

- JEDEC registered values

ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES 2N681-92	VALUES 2N5205-07	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° half sine wave conduction		16 <sup>(1)</sup>	22 <sup>(1)</sup>	A
				-65 to +65 <sup>(1)</sup>	-40 to +40 <sup>(1)</sup>	°C
Maximum RMS on-state current	$I_{T(RMS)}$			25	35	A
Maximum peak, one-cycle non-repetitive surge current	$I_{TSM}$	50 Hz half cycle sine wave or 6 ms rectangular pulse	Following any rated load condition, and with rated $V_{RRM}$ applied following surge	145	285	A
		60 Hz half cycle sine wave or 5 ms rectangular pulse		150 <sup>(1)</sup>	300 <sup>(1)</sup>	
		50 Hz half cycle sine wave or 6 ms rectangular pulse	Same conditions as above except with $V_{RRM}$ applied following surge = 0	170	340	
		60 Hz half cycle sine wave or 5 ms rectangular pulse		180	355	
Maximum $I^2t$ capability for fusing	$I^2t$	t = 10 ms	Rated $V_{RRM}$ applied following surge, initial $T_J = 125$ °C	103	410	A <sup>2</sup> s
		t = 8.3 ms		94	375	
Maximum $I^2t$ capability for individual device fusing	$I^2t$	t = 10 ms	$V_{RRM} = 0$ following surge, initial $T_J = 125$ °C	145	580	
		t = 8.3 ms		135	530	
Maximum $I^2\sqrt{t}$ capability for individual device fusing	$I^2\sqrt{t}$ <sup>(2)</sup>	t = 0.1 ms to 10 ms, initial $T_J < 125$ °C $V_{RRM}$ applied following surge = 0		1450	5800	A <sup>2</sup> √s
Maximum peak on-state voltage	$V_{TM}$	$T_J = 25$ °C, $I_{T(AV)} = 16$ A (50 A peak) 2N681, $I_{T(AV)} = 22$ A (70 A peak) 2N5204		2 <sup>(1)</sup>	2.3 <sup>(1)</sup>	V
Maximum holding current	$I_H$	Anode supply 24 V, initial $I_T = 1.0$ A		20 at 25 °C (typical)	200 <sup>(1)</sup> at -40 °C	mA

## Notes

- <sup>(1)</sup> JEDEC registered value  
<sup>(2)</sup>  $I^2t$  for time  $t_x = I^2\sqrt{t} \cdot \sqrt{t_x}$



SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES 2N681-92	VALUES 2N5205-07	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	$T_C = 125\text{ }^\circ\text{C}$ , $V_{DM} = \text{Rated } V_{DRM}$ , $I_{TM} = 2 \times di/dt$ , gate pulse = 20 V, 15 $\Omega$ , $t_p = 6\text{ }\mu\text{s}$ , $t_r = 0.1\text{ }\mu\text{s}$ maximum Per JEDEC standard RS-397, 5.2.2.6	100	-	A/ $\mu\text{s}$
			75	-	
			-	100	
Typical delay time	$t_d$	$T_C = 25\text{ }^\circ\text{C}$ , $V_{DM} = \text{Rated } V_{DRM}$ , $I_{TM} = 10\text{ A}$ DC resistive circuit, gate pulse = 10 V, 40 $\Omega$ source, $t_p = 6\text{ }\mu\text{s}$ , $t_r = 0.1\text{ }\mu\text{s}$	1	1	$\mu\text{s}$

BLOCKING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES 2N681-92	VALUES 2N5205-07	UNITS	
Minimum critical rate of rise of off-state voltage	dV/dt	$T_J = 125\text{ }^\circ\text{C}$ , exponential to 100 % rated $V_{DRM}$	100 (typical)	100 <sup>(1)</sup>	V/ $\mu\text{s}$	
		$T_J = 125\text{ }^\circ\text{C}$ , exponential to 67 % rated $V_{DRM}$	250 (typical)	250		
Maximum reverse leakage current	$I_{DRM}$ , $I_{RRM}$	$T_J = 125\text{ }^\circ\text{C}$	$V_{RRM}$ , $V_{DRM} = 400\text{ V}$	3.5	-	mA
			$V_{RRM}$ , $V_{DRM} = 500\text{ V}$	3.5	-	
			$V_{RRM}$ , $V_{DRM} = 600\text{ V}$	2.5	3.3	
			$V_{RRM}$ , $V_{DRM} = 700\text{ V}$	2.2	-	
			$V_{RRM}$ , $V_{DRM} = 800\text{ V}$	2	2.5	
			$V_{RRM}$ , $V_{DRM} = 1000\text{ V}$	-	2	
			$V_{RRM}$ , $V_{DRM} = 1200\text{ V}$	-	1.7	

**Note**

(1) JEDEC registered value

TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES 2N681-92	VALUES 2N5205-07	UNITS
Maximum peak gate power	$P_{GM}$	$t_p < 5\text{ ms}$ for 2N681 series; $t_p < 500\text{ }\mu\text{s}$ for 2N5204 series	5 <sup>(1)</sup>	60 <sup>(1)</sup>	W
Maximum average gate power	$P_{G(AV)}$		0.5 <sup>(1)</sup>	0.5 <sup>(1)</sup>	
Maximum peak positive gate current	$+I_{GM}$		2 <sup>(1)</sup>	2	A
Maximum peak positive gate voltage	$+V_{GM}$		10 <sup>(1)</sup>	-	V
Maximum peak negative gate voltage	$-V_{GM}$		5 <sup>(1)</sup>	5 <sup>(1)</sup>	
Maximum required DC gate current to trigger	$I_{GT}$	$T_C = \text{min. rated value}$ Maximum required gate trigger current is the lowest value which will trigger all units with +6 V anode to cathode	80 <sup>(1)</sup>	80 <sup>(1)</sup>	mA
		$T_C = 25\text{ }^\circ\text{C}$	40	40	
		$T_C = 125\text{ }^\circ\text{C}$	18.5	20	
Typical DC gate current to trigger		$T_C = 25\text{ }^\circ\text{C}$ , +6 V anode to cathode	30	30	
Maximum required DC gate voltage to trigger	$V_{GT}$	$T_C = -65\text{ }^\circ\text{C}$ Maximum required gate trigger voltage is the lowest value which will trigger all units with +6 V anode to cathode	3 <sup>(1)</sup>	3 <sup>(1)</sup>	V
		$T_C = 25\text{ }^\circ\text{C}$	2	2	
Typical DC gate voltage to trigger		$T_C = 25\text{ }^\circ\text{C}$ , +6 V anode to cathode	1.5	1.5	
Maximum DC gate voltage not to trigger	$V_{GD}$	$T_C = 125\text{ }^\circ\text{C}$ Maximum gate voltage not to trigger is the maximum value which will not trigger any unit with rated $V_{DRM}$ anode to cathode	0.25 <sup>(1)</sup>	0.25 <sup>(1)</sup>	V

**Note**

(1) JEDEC registered value



THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES 2N681-92	VALUES 2N5205-07	UNITS
Operating junction and storage temperature range	$T_J, T_{Stg}$		-65 to 125 <sup>(1)</sup>	-40 to 125 <sup>(1)</sup>	°C
Maximum internal thermal resistance, junction to case	$R_{thJC}$	DC operation	1.5	1.5 <sup>(1)</sup>	°C/W
Typical thermal resistance, case to sink	$R_{thCS}$	Mounting surface, smooth, flat and greased	0.35	0.35	
Mounting torque ± 10 %	to nut	Lubricated threads (Non-lubricated threads)	20 (27.5)		lbf · in
			0.23 (0.32)		kgf · cm
			2.3 (3.1)		N · m
	to device	Lubricated threads	25		lbf · in
			0.29		kgf · cm
			2.8		N · m
Approximate weight			14	14	g
			0.49	0.5	oz.
Case style			TO-48 (TO-208AA)		

**Note**

<sup>(1)</sup> JEDEC registered value

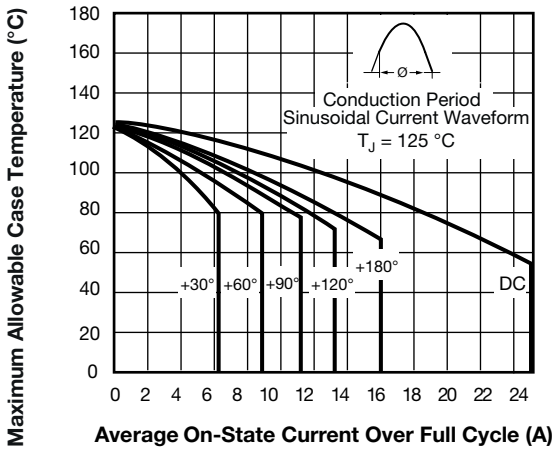


Fig. 1 - Maximum Allowable Case Temperature vs. Average On-State Current, 2N681 Series

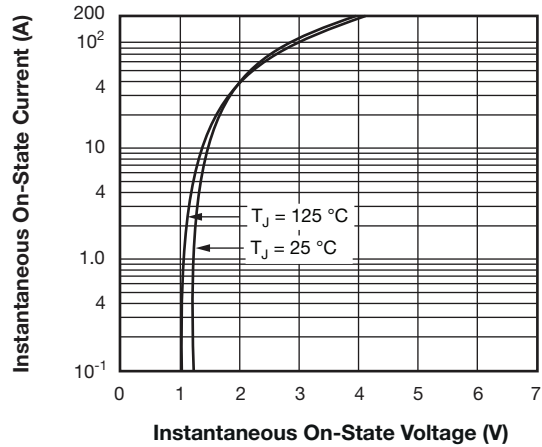


Fig. 2 - Maximum On-State Voltage vs. Current, 2N681 Series

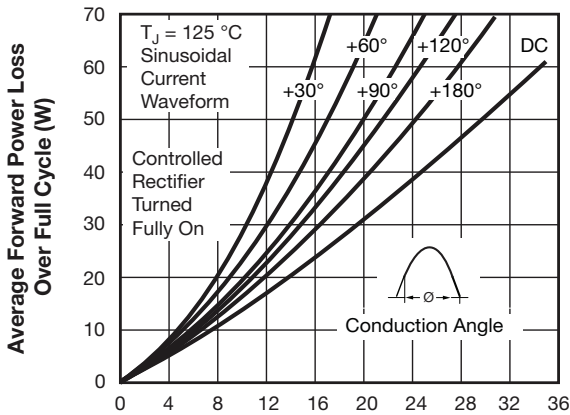


Fig. 3 - Maximum Low Level On-State Power Loss vs. Current (Sinusoidal Current Waveform), 2N681 Series

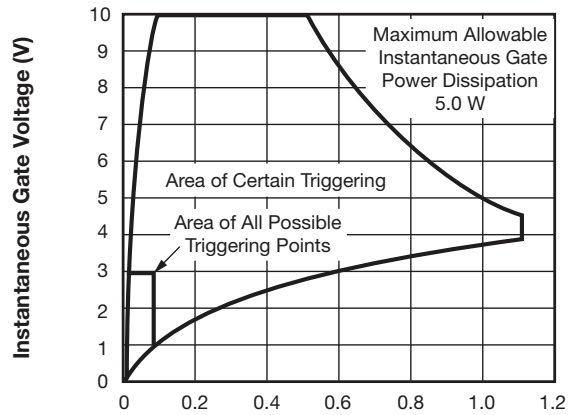


Fig. 5 - Gate Characteristics, 2N681 Series

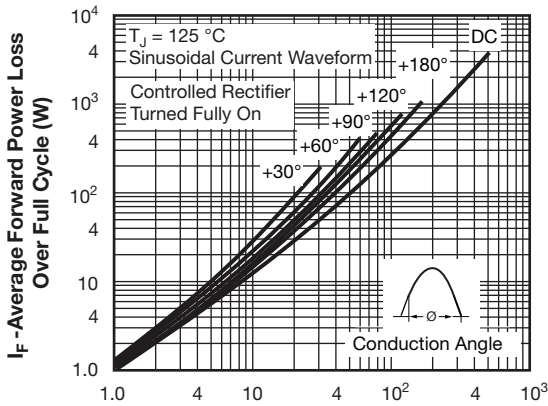


Fig. 4 - Maximum High Level On-State Power Loss vs. Current (Sinusoidal Current Waveform), 2N681 Series

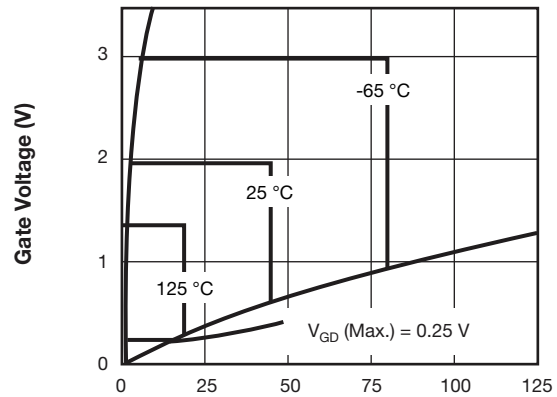


Fig. 5a - Area of All Possible Triggering Points vs. Temperature, 2N681 Series

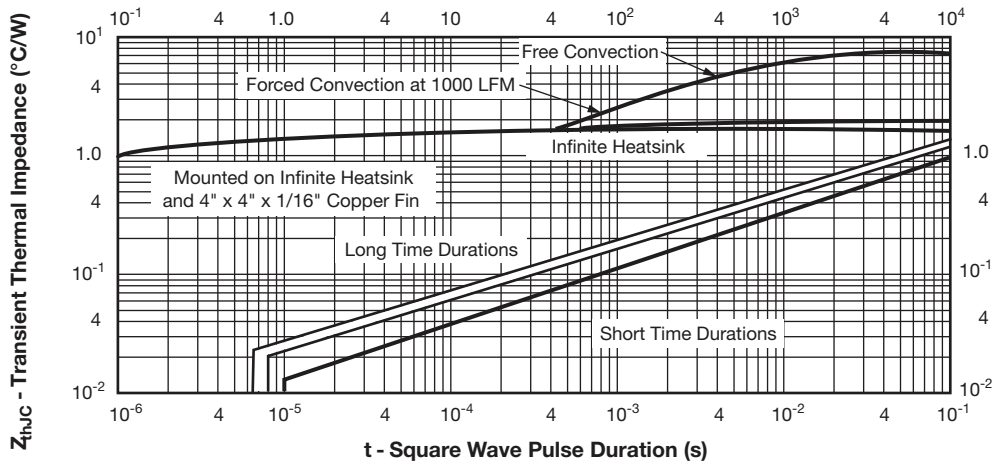


Fig. 6 - Maximum Transient Thermal Impedance, Junction to Case, vs. Pulse Duration, 2N681 Series

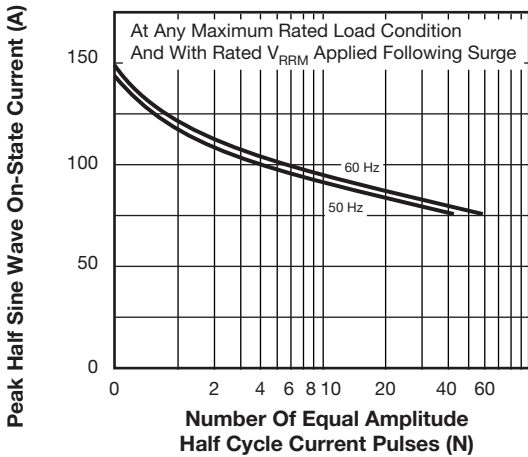


Fig. 7 - Maximum Non-Repetitive Surge Current vs. Number of Current Pulses, 2N681 Series

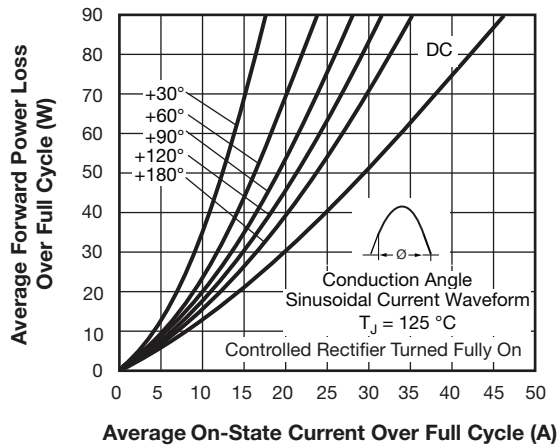


Fig. 10 - Maximum Low-Level On-State Power Loss vs. Average On-State Current (Sinusoidal Current Waveform), 2N5205 Series

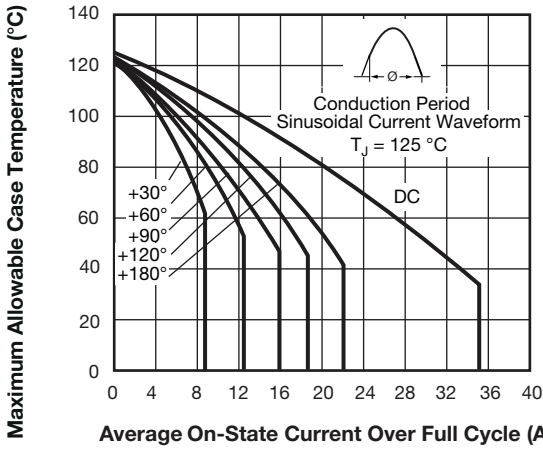


Fig. 8 - Maximum Allowable Case Temperature vs. Average On-State Current (Sinusoidal Current Waveform), 2N5205 Series

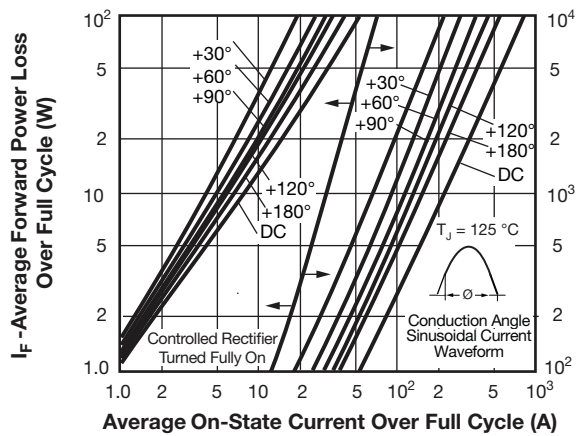


Fig. 11 - Maximum High-Level On-State Power Loss vs. Average On-State Current (Sinusoidal Current Waveform), 2N5205 Series

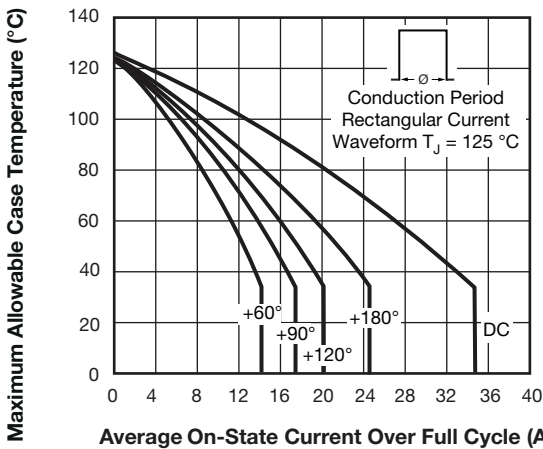


Fig. 9 - Maximum Allowable Case Temperature vs. Average On-State Current (Rectangular Current Waveform), 2N5205 Series

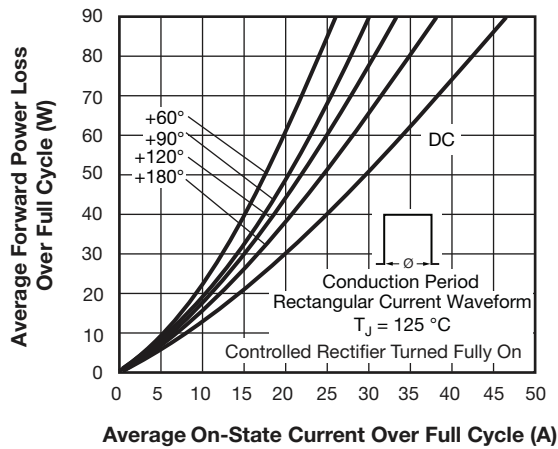


Fig. 12 - Maximum Low-Level On-State Power Loss vs. Average On-State Current (Rectangular Current Waveform), 2N5205 Series



Fig. 13 - Maximum High-Level On-State Power Loss vs. Average On-State Current (Rectangular Current Waveform), 2N5205 Series



Fig. 14 - Maximum Instantaneous On-State Voltage vs. Instantaneous On-State Current, 2N5205 Series

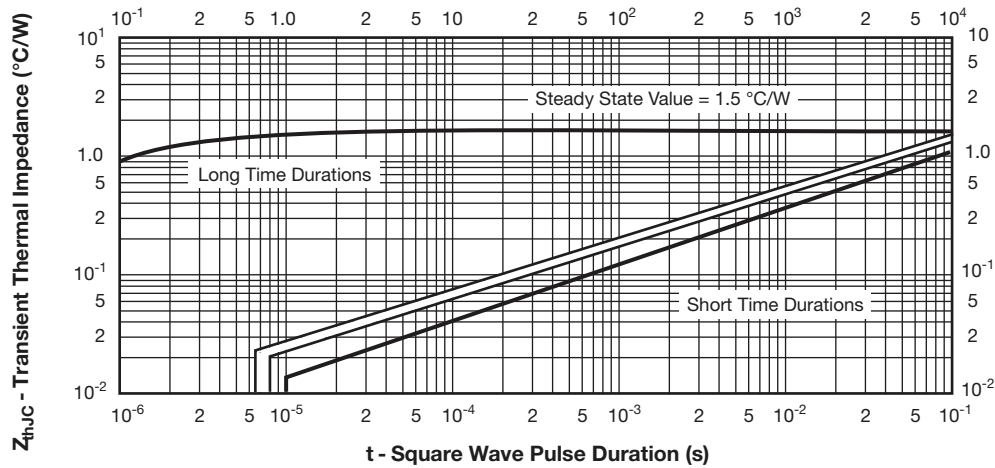


Fig. 15 - Maximum Transient Thermal Resistance, Junction to Case vs. Pulse Duration, 2N5205 Series

LINKS TO RELATED DOCUMENTS

Dimensions

[www.vishay.com/doc?95333](http://www.vishay.com/doc?95333)





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